A Combined Anti-Aliasing Filter and 2-tap FFE in 65-nm CMOS for 2x Blind 2-10 Gb/s ADC-Based Receivers

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Abstract- This paper presents a combined anti-aliasing filter and 2-tap feed-forward equalizer (AAF/FFE) as an analog front-end (AFE) for 2x blind ADC-based receivers. The front-end optimizes the channel/filter characteristics for data-rates of 2-10 Gb/s. The AAF bandwidth scales with the data-rate and the 2-tap FFE is designed without the need for noise-sensitive analog delay cells. The AAF/FFE is implemented in 65-nm CMOS, occupies 0.013 mm^2, and consumes 2.4 mW at 10 Gb/s.

I. Introduction

High definition television, voice over Internet, and even gaming systems are creating a large demand for faster data transmission from chip-to-chip to over continental distances. Established industry standards such as high-definition multi-media interface (HDMI), Peripheral Component Interconnect Express (PCIe), Universal Serial Bus (USB), and Serial Advanced Technology Attachment (SATA) have driven this market for decades. New receiver architectures are sought everyday to carve out a path for multi-gigabits per second (Gb/s) data transmission.

Binary receivers use a flip-flop at the front-end to sample the incoming signal. A binary receiver effectively detects the signs of each sample while discarding their magnitudes. As a result, all equalization for these receivers must be performed at the front-end, prior to the sampling. Usually, an analog equalizer that precedes the binary sampler takes care of this compensation. ADC-based receivers [1, 2], however, sample the received signal with an ADC. Each sample is now represented by more than one bit, preserving both the sign and the magnitude information. The extra information about the received signal enables the ADC-based receivers to employ more complex equalization in the digital domain in addition to the analog equalization. As the advancement in wireline channels lags the rapid increase in the data-rate, the need for intensive compensation of the channel impairments grows. Accordingly, ADC-based receivers which allow for a higher degree of equalization are suitable candidates for wireline multi-Gb/s transceivers above 20 Gb/s [3].

Current 2x blind ADC-based receivers rely on interpolation between digital samples taken at 2x the baud rate in order to estimate the center and edge of the received signal for timing recovery [4, 5]. This interpolation leads to erroneous estimation of the zero crossings and reduced jitter tolerance if the received signal contains sharp transitions or, equivalently, if the received signal contains frequencies beyond the baud rate. This phenomenon, known as aliasing, occurs either due to shorter-than-target channel length or due to smaller-than-target data-rates, especially in systems that support standards with various data-rates.

To date, 2x blind ADC-based receivers [4, 5] rely on the communication channel to perform the necessary anti-aliasing. To show the significance of the anti-aliasing filter (AAF), we simulated the CDR presented in [5] with and without the AAF at 2 Gb/s, when the channel was unable to band-limit the input signal. Fig. 1 shows the jitter tolerance results. Without the AAF, the CDR is not able to lock. Turning on the AAF, on the other hand, restores the jitter tolerance to the expected values.

To support channels of different length, the receiver needs to provide equalization with adjustable parameters. Equalization can be performed in the analog domain (before the ADC) or in the digital domain (after the ADC). The former boosts noise at high frequency while the latter boosts the quantization noise from the ADC.

This paper presents an analog front-end (AFE) that consists of an AAF combined with an analog FFE, targeting a data-rate in the range of 2-10 Gb/s. The AAF suppresses the high-frequency noise. The anti-aliasing function is implemented using integrating-sampler (IS) circuits, allowing the overall bandwidth of the channel to be adjusted in proportion to the data-rate. The analog FFE, also implemented in IS circuits, provides up to 14 dB of boost at the Nyquist frequency (half the data-rate).

The remainder of the paper is organized as follows. Section II presents the receiver architecture we have targeted for the proposed AFE. Section III describes the circuit implementation of the AAF/FFE and the required clock generation.

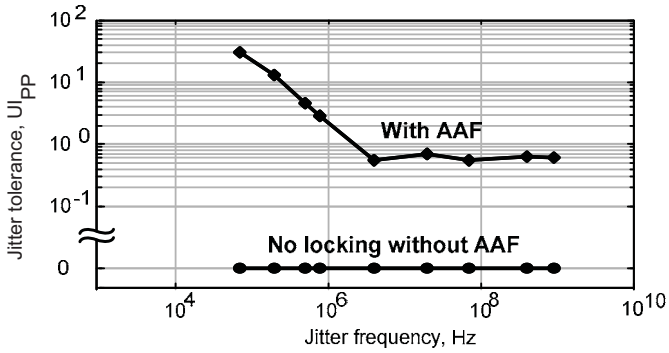

Fig. 1. Simulated Jitter Tolerance of the CDR in [5] with/without AAF

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Experimental results from a test-chip fabricated in a 65-nm CMOS process are included in Section IV. Conclusions are provided in Section V.

II. Receiver Architecture

Fig. 2 presents the overall architecture of a conventional ADC-based receiver (RX) and highlights the contribution of this work: a combined AAF and FFE analog front-end. The AAF/FFE takes the received signal (2-10 Gb/s) and produces four band-limited, equalized signals at half the data-rate to feed the four time-interleaved half-rate 4-bit ADC's. As illustrated in Fig. 2, the target bandwidth of the analog front-end (e.g. with 50% FFE tap coefficient) must scale linearly with the data-rate; otherwise aliasing occurs. The 4 interleaved ADCs quantize the data at twice the baud rate; this data is DeMUXed and sent to the 2x blind ADC-based CDR.

To ensure that the AAF bandwidth scales with the data-rate, we employ an integration and dump (I&D) architecture, which integrates the input for a period of time (T_i). The I&D is an LTI system with a rectangular impulse response, whose pulse-width is equal to T_i [6, 7]. Therefore, if T_i is a function of the data-rate, the resulting filter bandwidth will be controlled by the data-rate.

III. Circuit Implementation

Fig. 3 shows a detailed block diagram of the AAF/FFE front-end. The overall system has a differential input (V_i) and produces 4 interleaved differential outputs (V_{o1} to V_{o4}). The 4 clocks driving this system, SC_0 to SC_3, define the 4 phases of post-cursor tap integration (PI), main tap integration (MI), hold (Hld), and reset (Rst) for each output node. V_i is converted to current via two G_m cells and is integrated on the input capacitance of the ADC (C_L) first by CK_{PI} (enabling post-cursor tap integration) and second by CK_{MI} (enabling main tap integration). The final result is held constant during the Hld phase and reset during the Rst phase.

Anti-aliasing is realized by integration and dump of a current on C_L which is produced by a 2-tap FFE. The tap coefficients are controlled via the gains of two resettable integrators. Delaying the input signal to achieve equalization is effectively performed through 4 phases of operations (PI, MI, Hld, Rst). This avoids the use of analog delay cells which often exhibit delay sensitivity to PVT variation and require delay calibration.

The schematic of the AAF/FFE front-end is presented in Fig. 4. Each tap uses a differential pair with resistive degeneration and produces an output current that is steered into one of the 4 interleaved branches depending on $SC_{0\text{-}3}$. The FFE tap-coefficient is adjusted by setting the bias currents of the differential pair (I_{b1} for the main tap and I_{b2} for the post-cursor tap). The reset operation is performed by three PMOS transistors as shown in Fig 4. Two dummy transistors are added to the reset cell to eliminate charge-injection effects.

Fig. 5 depicts the circuitry used for the clock generation of the AAF/FFE system. A full-rate clock is divided by a current-mode logic (CML) divider, generating 4-phase half-rate clocks. For power/area savings, the CML half-rate clocks are further converted to CMOS-style rail-to-rail levels by CML-to-CMOS converters. The duty cycles of these converters are corrected by back-to-back inverters [8]. Finally, the generated 4-phase CMOS clocks pass through logic NOR-gates to create the desired SC_n and $\overline{SC_n}$ signals.

The four ADCs are required to sample the AAF/FFE output when it is valid (i.e. during Hld phase). Therefore, the ADC clock, $(f_b/2)_\Delta$, is required to be phase-aligned to the AAF/FFE clock, $SC_{0\text{-}3}$. Fig. 6 shows a timing diagram of the nodes in Fig. 5. A 2-phase full-rate external clock is used to generate the pulses driving the AAF/FFE. The same external clock is used to generate ADC clocks. For accurate sampling, the external clock is shifted by 25% UI prior to the divider. This phase is adjusted manually in measurements.

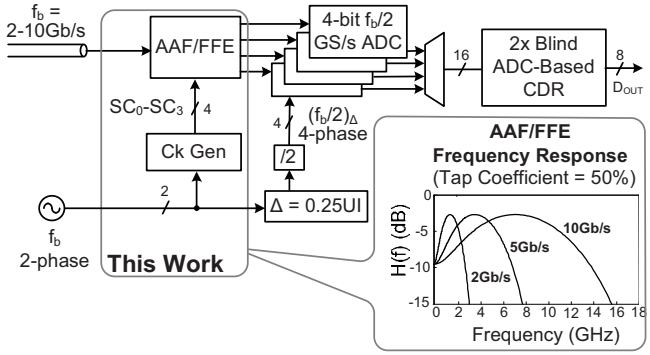


Fig. 2. Proposed analog front-end for a 2x blind ADC-Based RX.

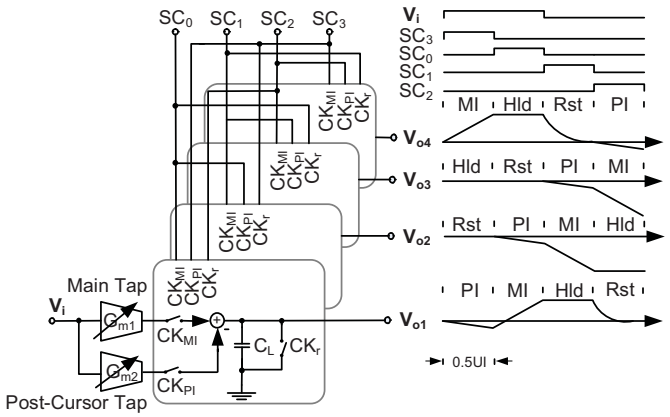


Fig. 3. The overall AAF/FFE system block diagram.

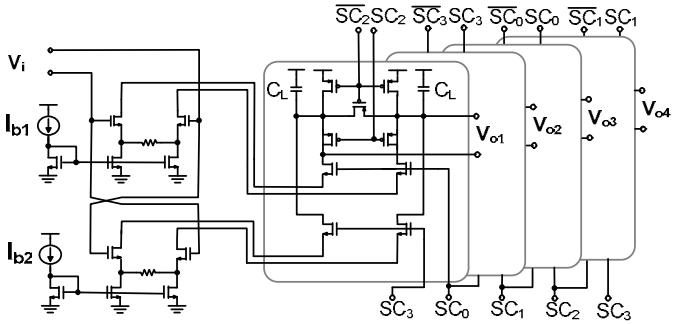


Fig. 4. AAF/FFE circuit implementation.

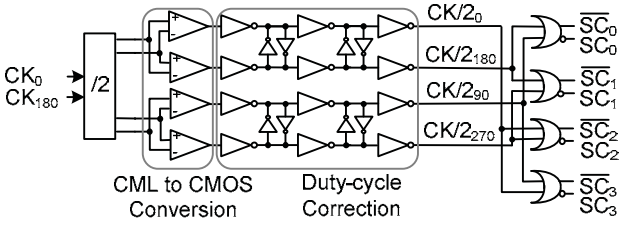


Fig. 5. The clock generation circuitry.

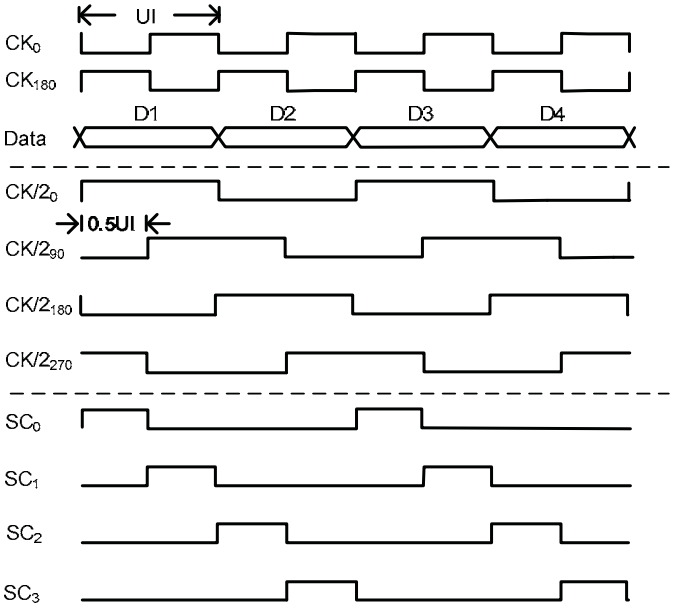


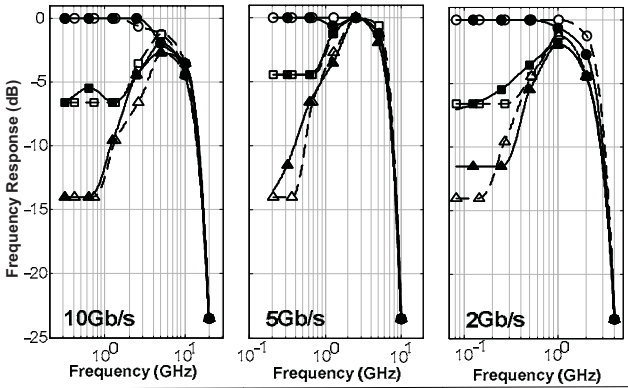
Fig.6. Clock timing diagram.

IV. Experimental Results

A test-chip was fabricated in a 65-nm CMOS process and measured to validate the proposed design. Fig. 7 shows the measured and simulated frequency responses of the AAF/FFE front-end for data-rates of 2, 5, and 10 Gb/s. At each data-rate, three sets of bias currents (I_{b1} & I_{b2}) were used to achieve 0, 5, and 14 dB of boost. For each setting, 6 input tones were applied and the output digital eye-diagrams were constructed. The digital eye-diagrams correspond to the ADC samples taken at one DeMUX output. This data is imported to Matlab where it is rearranged in time to construct the eye. The frequency of the ADC sampling clock is set to have an offset with respect to the input data-rate so that the eye can be scanned in the same way as the sampling head of the digital oscilloscope. This frequency offset is chosen such that the entire eye is swept with 0.64%UI resolution. The amplitudes of the eye-diagrams were converted to dB values and plotted versus their corresponding frequencies. Frequency response plots in Fig. 7 confirm that the combined frequency response of the AAF and FFE scales with the data-rate. The slight discrepancies in the low-frequency portion of the response at 2 Gb/s (and partially at 5 Gb/s) are artifacts of the measurement equipment as these frequencies were outside the operating range of the power splitter used.

The need for anti-aliasing filter arises at the lower range of the data-rate (i.e. 2 Gb/s) when the interconnect is unable to band-limit the input signal. To demonstrate this, we used a total of 44" SMA cable in the data-path. The resulting attenuation of this channel was measured to be 0.9 dB at 1 GHz. Next, we observed the output eye with and without the AAF. To measure the case without the AAF, we used a test-chip which directly connects the input to the ADCs (i.e. no AAF). Fig. 8 shows the output eyes when the AAF is on and off. In both cases, a 2^7-1 PRBS data is transmitted at 2.0004 Gb/s while the receiver sampling frequency is 2 GHz. It is clear from the figures that the slopes of the eye opening are reduced when the AAF is on. Quantitatively, the slope is reduced by a factor of 2.4. Fig. 1, presented previously, showed that excluding the AAF prevents the CDR from locking.

A 2^7-1 PRBS sequence at 10.0005, 5.0005, and 2.0004 Gb/s was employed to verify the FFE at 10, 5, and 2 Gb/s, respectively. To ensure that the FFE can open an otherwise closed eye, an external FR4 backplane was used to impose 13.3, 13, and 11.7 dB of attenuation at the corresponding Nyquist frequencies. Fig. 9 shows that when the FFE is off, the three output eyes are closed. However, by turning on the FFE, we obtain vertical eye-openings of 5LSBs (223mV), 5LSBs (281.5mV), and 6LSBs (380.4mV) at 10, 5, and 2 Gb/s, respectively.



	I_{b1}/I_{b2}	I_{b1}/I_{b2}	I_{b1}/I_{b2}
--o--	1.3/0 mA	724/0 µA	404/0 µA
--□--	600/170 µA	436/161 µA	317/152 µA
--△--	320/210 µA	272/204 µA	247/211 µA

Fig. 7. Measured (solid) vs simulated (dashed) frequency response.

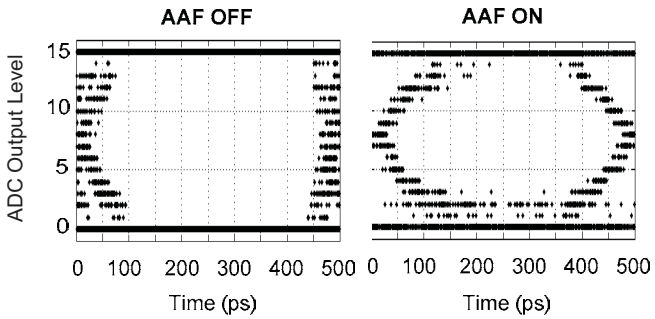


Fig. 8. Digital eye-diagrams with AAF OFF/ON.

Fig. 10 shows the test-chip die-photo, which includes the AAF/FFE front-end, the clock generation, the four 4-bit ADCs, and the DeMUX. Table I summarizes the measurement results. The AAF/FFE consumes a total of 2.4 mW at 10 Gb/s and occupies 0.013 mm^2 of the chip area. The clock generation circuitry consumes 97.2 mW at 10 Gb/s and occupies an area of 0.034 mm^2. The role of the clock generation circuitry was to generate clean pulses for preliminary verification of the AAF/FFE functionality. The power of the clock generation can be reduced in future designs by optimizing the buffer sizes and the back-to-back inverters shown in Fig. 5.

V. Conclusions

This paper presents an AFE targeting 2x blind ADC-based receivers. The AFE consists of a combined AAF and 2-tap FFE, 4 time-interleaved ADCs, the clock generation circuitry, and the DeMUXes. This design overcomes the limited data-rate coverage of 2x blind ADC-based receivers and extends it to cover 2-10 Gb/s. A test-chip was fabricated in a 65-nm CMOS process and the measurement results were presented. The AAF/FFE consumes a total of 2.4 mW at 10 Gb/s and occupies 0.013 mm^2 of the chip area.

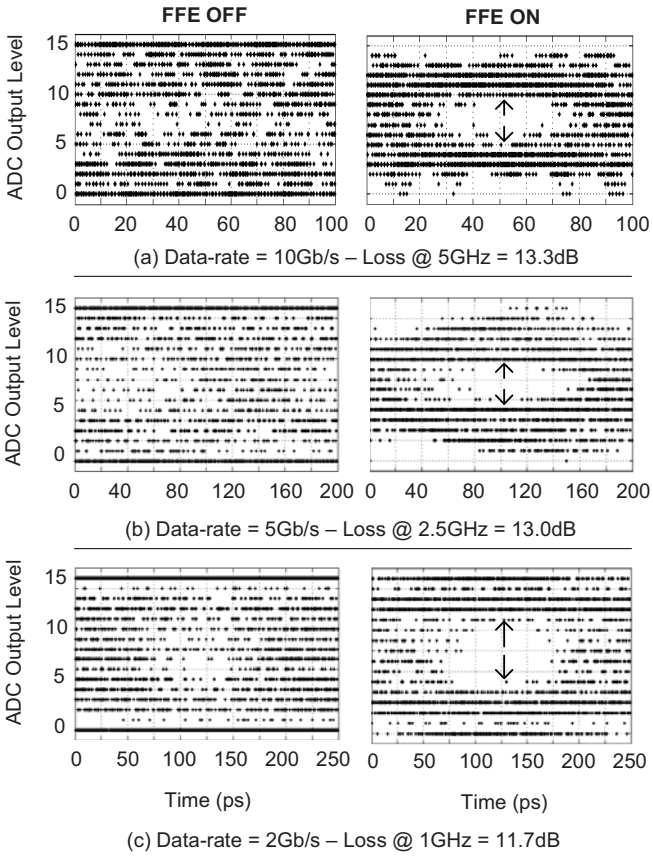


Fig. 9. Digital eye-diagrams with FFE OFF/ON.

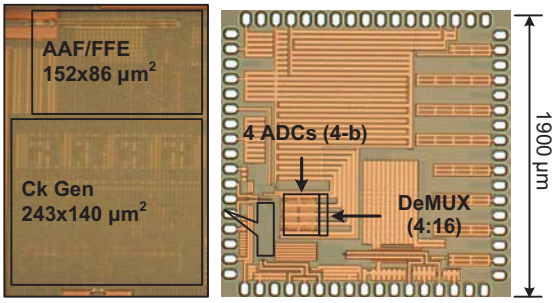


Fig. 10. Die micrograph.

TABLE I

Performance Summary

Technology	65-nm CMOS	
Data Rate	2 – 10 Gb/s	
Supply	1.2 V	
	AAF/FFE	Ck Gen
Power @ 10 Gb/s	2.4 mW	97.2 mW
Power @ 5 Gb/s	2.2 mW	66 mW
Power @ 2 Gb/s	1.6 mW	42 mW
Area	152 x 86 µm²	243 x 140 µm²

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