18.5 A 3.2Gb/s Semi-Blind-Oversampling CDR

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A blind-oversampling CDR tracks the high-frequency jitter of the input data stream, but is limited at low-frequencies by the size of its FIFO [1]. A phase-tracking CDR, on the other hand, tracks jitter at frequencies below f_{3dB} of its loop filter, but performs poorly beyond this frequency [2]. In this paper, a semi-blind-oversampling technique is presented. The proposed technique produces a jitter tolerance equal to the product of the jitter tolerances of a phase-tracking CDR and a blind-oversampling CDR (see Fig. 18.5.1), thereby increasing the low-frequency jitter tolerance by a factor of 32 (limited by the FIFO size). This enhancement in low-frequency jitter tolerance is essential to applications such as spread-spectrum clocking [3] where the clock edge can deviate from its nominal location by as many as a few hundred UIs.

The block diagram of the proposed hybrid CDR is shown in Fig. 18.5.2. A 20-phase 800MHz VCO is used to 5× oversample a 3.2Gb/s sequence. Therefore, in one period of the 800MHz clock, a total of 20 samples are collected which corresponds to 4UI of the received data. These 20 samples are then retimed and passed to the next block where data transitions are found by XORing adjacent samples. This block also estimates the expected value of the transition phase (fine-phase) and sends this information to the down-sampler to pick the data bits among the 20 samples. Since a $^2/_5$UI of peak jitter per 4UI window is tolerated, the downsampled data size from a 20-sample window can be between 3 and 5 bits, as explained later. This data is then written into an 8×4 elastic FIFO where up to a total of 16UI peak jitter (half the FIFO size) is absorbed.

The FIFO write pointer is also passed to a 5b DAC, then low-pass filtered to provide the control voltage for the VCO. This closes the loop, creating a hybrid CDR that is no longer blind, but tracks low-frequency jitter with enhanced tolerance. This can be intuitively described as follows: in a phase-tracking CDR, the phase difference between the received data and the *recovered clock* can never exceed ±0.5UI; otherwise an error occurs. In contrast, the blind oversampling system allows its *blind clock* to drift from the data by as many as ±16UI (in this implementation). In the hybrid system, the *recovered clock* of the phase-tracking component is fed to the *blind clock* of the oversampling component, producing a jitter tolerance that is the product of the two tolerances.

Figure 18.5.3 shows the circuit implementation of the 20-phase VCO using a 10-stage ring oscillator. Extra buffers cut halfway through the ring to increase the VCO frequency [4]. The samplers are integrated with the VCO, eliminating the need to distribute a multi-phase clock.

The expected location of the data transitions within the 5-sample nominal bit-period (fine-phase) is calculated by observing a window of 20 samples. In general, the transitions can occur at any of the five fine-phases (0 to 4) with an estimated probability of T_n/T, where T_n is the number of transitions at phase n, and T is the total number of transitions. Thus, to estimate the expected value of n, one must sum nT_n/T over all n. This however requires division and multiplication, and hence cannot be completed within one clock cycle. To simplify, it is observed that the partial sums of nT_n are equal around the expected phase. By checking this at each of the five possible phases and choosing the closest match, the expected phase can be found, eliminating the need for division. Further, by replacing n with 2^n, multiplication is reduced to simple binary shifts, without causing error in the final results.

Figure 18.5.4 shows the implementation of this scheme along with one example for transition totals at each phase. Partial sums are passed from one side to the other in both directions, manipulated at each stage, then compared (subtracted) to see whether the result is positive or negative by observing its MSB. The stage at which the MSB flips indicates the expected phase. In the example shown, the previous phase is assumed to be ϕ_2, and the current phase is calculated also as ϕ_2 (encoded in one-hot binary). In case of no transition in a window, the previous phase is simply retained. Simulation results confirm that the entire operation of fine-phase detection completes in less than 1.14ns, below one period of the 800MHz clock.

The fine-phase guides the selection of the data bits amongst the 20 samples. Under typical conditions, 4 bits are picked among 20 samples. But depending on the relation between the sampling phases of two adjacent windows, there exists 6 cases (among a total of 25) for which an additional bit must be picked or a bit to be dropped, ending up with 3 or 5 bits. These cases are shown in Fig. 18.5.5 along with an illustration for three examples.

Figure 18.5.6 shows measured results for the jitter tolerance of the proposed CDR, fabricated in a 0.11µm CMOS process, and compares them against the behavioral-simulation results and analytical predictions, all in close agreement. The measured results are obtained by first modulating the clock frequency of an off-the-shelf VCO (Minicircuit's ZX95-2650-S) and passing it to a 2^{31}-1 PRBS generator, then measuring the modulation amplitude at which the BER becomes 6×10^{-5}. The behavioral simulations are performed in Verilog, repeated at each frequency for 10^5 cycles with increasing jitter amplitude until an error is observed. The analytical prediction is based on an allowable phase change of $^2/_5$UI over a run length of 32 (2^{31}-1 PRBS), a FIFO of 32b, and a loop filter with an RC time constant of 300ns. With these parameters, the corner frequency of the jitter tolerance of the phase-tracking CDR exceeds that of the oversampling counterpart, producing a -60dB/dec overlap. Below and above this frequency range, the tolerance slope is due only to the phase-tracking CDR and the oversampling CDR, respectively. All results are measured at 2.4Gb/s due to the limited tuning bandwidth of the VCO used to frequency-modulate the clock. The CDR, however, is fully operational from 1.9 to 3.5Gb/s. At 2.4Gb/s, the design consumes 180mW from a 1.2V supply.

To compare the jitter tolerance of the hybrid CDR against that of a purely phase-tracking CDR, the latter is simulated by effectively reducing the FIFO size to 1b. The result confirms that the hybrid CDR has a low-frequency jitter tolerance that is 32 times that of the phase-tracking CDR, as shown in Fig. 18.5.6. The die micrograph of the fabricated testchip, measuring 440µm×340µm excluding pads, is shown in Fig. 18.5.7.

References

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[3] M. Kokubo, et al., "Spread-Spectrum Clock Generator for Serial ATA Using Fractional PLL Controlled by ΔΣ Modulator with Level Shifter," *ISSCC Dig. Tech. Papers*, pp. 160-161, Feb., 2005.
[4] L. Sun, et al., "A 1.25-GHz 0.35-µm Monolithic CMOS PLL Based on a Multiphase Ring Oscillator," *IEEE J. Solid-State Circuits*, pp. 910-916, June, 2001.

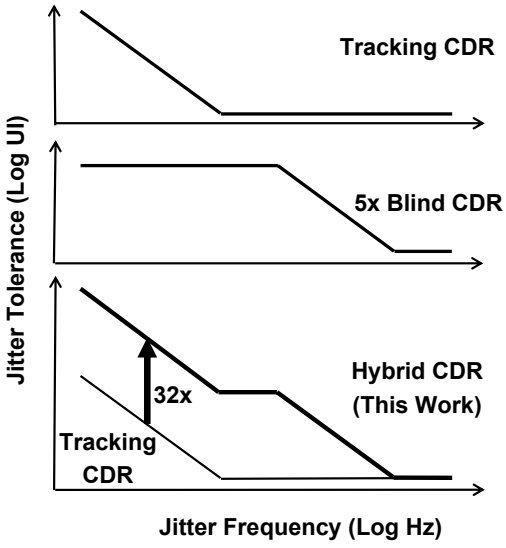

Figure 18.5.1: Increased jitter tolerance in a hybrid CDR.

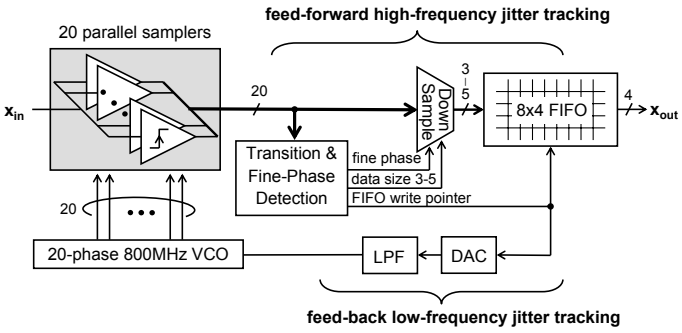

Figure 18.5.2: Block diagram of the hybrid CDR.

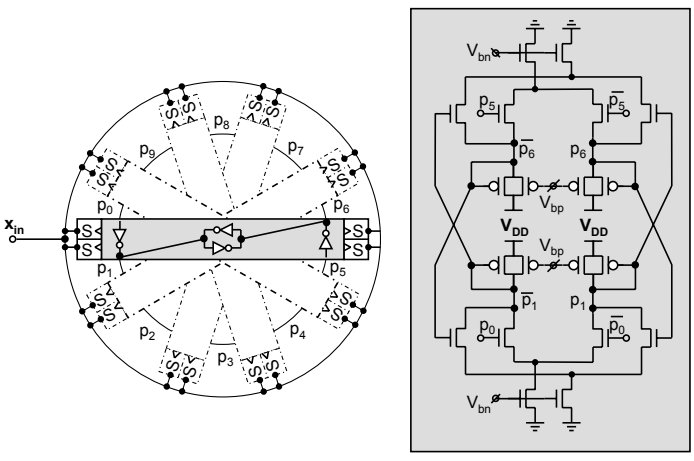

Figure 18.5.3: 20-phase VCO with samplers.

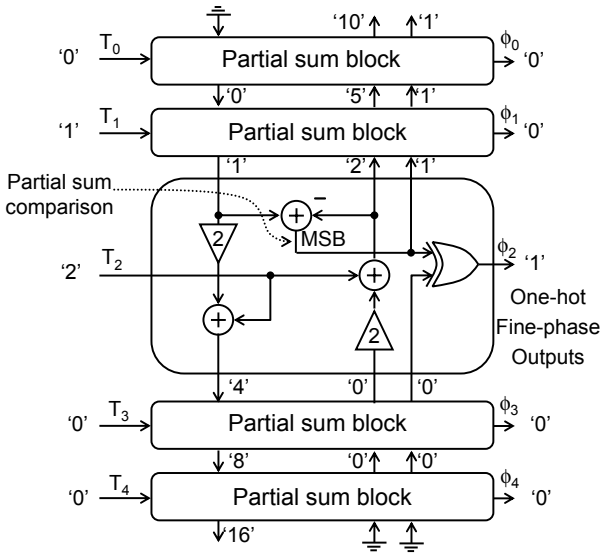

Figure 18.5.4: Implementation of fine-phase detection.

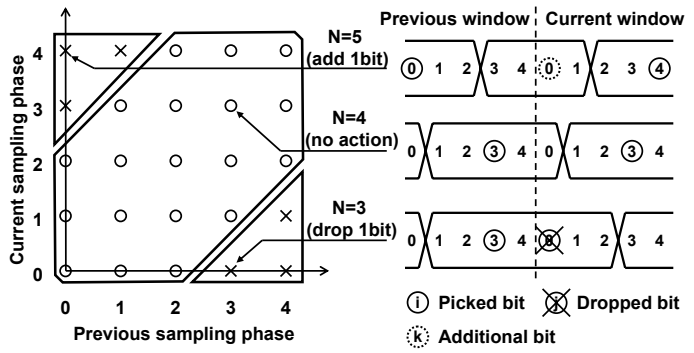

Figure 18.5.5: Data-selection implementation.

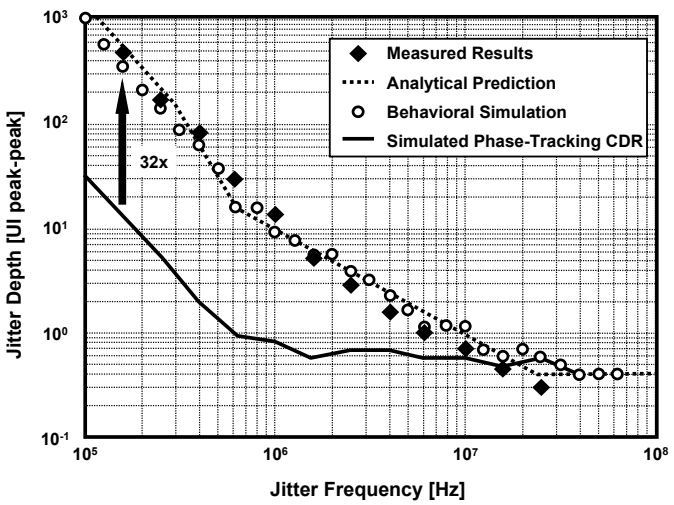

Figure 18.5.6: Measurement results.

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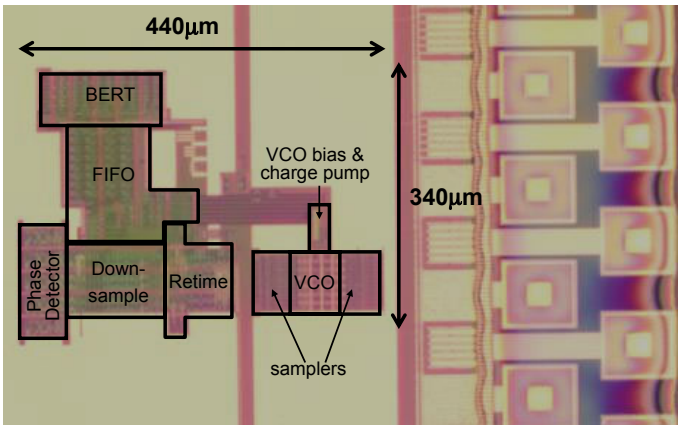

Figure 18.5.7: Chip micrograph.

