25.1 A 5Gb/s Adaptive DFE for 2× Blind ADC-Based CDR in 65nm CMOS

Behrooz Abiri[1], Ali Sheikholeslami[1], Hirotaka Tamura[2], Masaya Kibune[2]

[1]University of Toronto, Toronto, Canada
[2]Fujitsu Laboratories, Kawasaki, Japan

ADC-based receivers allow for extensive equalization in the digital domain and therefore can easily compensate for channel loss at higher data rates [1]. Digital equalization can be implemented as an FFE [2] or DFE [3]. An adaptive FFE is straight forward to implement [2], as it relies on magnitudes only (not phases) of the blind samples, however, it enhances the quantization noise of the ADC. A DFE has better noise immunity [3], but challenges remain in designing an adaptive DFE for receivers with blind clocks. A typical adaptive engine for a DFE compares the equalized center samples against a desired level to calculate error in each sample. The power of this error is then minimized to guide equalization. In a blind receiver, however, the center samples are not known; the blind samples may deviate from the eye's center and move closer to the zero crossings. As a result, one cannot use a single desired level independent of the blind sampling phase; the desired level must change according to the sampling phase. In this paper, we use a *desired waveform*, instead of a *desired level*, to perform the adaptation. Our measurement results confirm that this approach adapts the coefficients within 80µs and opens an otherwise closed eye for a channel attenuation of 13.3dB at 2.5GHz.

A simplified block diagram of a 2× blind ADC-based receiver with an adaptive DFE is demonstrated in Fig. 25.1.1. The received 5Gb/s signal is blindly sampled at 10GS/s using four interleaved 5b flash ADCs. The ADC uses a 4-phase 2.5GHz clock that is generated from an external 5GHz reference clock. The 5-bit samples are DMUXed further to produce 16 samples of 5-bit each (corresponding to a total of 8 UIs). All other blocks in this diagram operate at the reduced clock rate of 625MHz. The 5-bit samples are then passed to a 1-tap speculative DFE, where the contribution of the previous bit is subtracted (or added) from each sample. This contribution, which defines the DFE coefficient (α), depends on the sampling phase of the blind clock (which is not fixed). Accordingly, we define eight such coefficients (α_1 to α_8) corresponding to eight phase bins in one UI [3] and choose one for each blind sample based on the sampling phase extracted in the digital CDR. The task of the adaptive engine is to determine these eight coefficients automatically while the link is in full operation (i.e., no training sequence). The equalized samples (S^+_{EQ} and S^-_{EQ}) are then passed to the digital CDR [4] where the average phase of the zero crossings (Φ_{AVE}) is extracted and the data is recovered.

The detailed implementation of the adaptive engine is presented in Fig. 25.1.2. The speculative DFE produces two sets of 16 equalized samples corresponding to 8 UIs. For adaptation, 2 samples from each set ($S^+_{EQ-8,9}$ and $S^-_{EQ-8,9}$) corresponding to 1 UI out of 8 UIs are used. A 2:1 MUX selects either $S^+_{EQ-8,9}$ or $S^-_{EQ-8,9}$ based on the previous recovered bit and denotes these by $S_{EQ-8,9}$, which are the equalized signals corresponding to two blind samples in 1 UI. These equalized signals should be compared against their corresponding reference levels ($d_{ref-1,2}$) which are provided by the desired waveform generator block (discussed later). The result of subtracting $d_{ref-1,2}$ from $S_{EQ-8,9}$ is 2 equalization error signals whose values depend on the remaining inter-symbol interference (ISI) in the equalized samples. The goal of adaptation engine is to find coefficients α_1 to α_8 such that these errors are minimized regardless of the sampling phase of blind clock. To this end, we multiply the error by the previous bit to obtain the residual 1st post-cursor ISI. We then accumulate these residual ISI to obtain the ISI, or equivalently the DFE coefficient.

The desired waveform generator produces valid desired references whenever there is a data transition. If no transition occurs, the error values are incorrect and are discarded. This transition filtering, implemented by 2:1 MUX after the multiplication in Fig. 25.1.2, reduces the adaptation speed but makes the design of desired waveform generator simpler. The 1:8 DMUX selects the accumulators that correspond to the current sampling phase of the blind clock. The outputs of accumulators (α_1 to α_8) are the DFE coefficients corresponding to 8-phase bins of 1 UI. Depending on the sampling phase of the clock, two of these coefficients (α_i, α_{i+4}) are provided to the DFE to be subtracted from the two adjacent samples of ADC, which are ½ UI apart.

The PD in the digital CDR uses linear interpolation to recover zero-crossings [4]. For this PD, a triangular waveform is the ideal waveform as its interpolated zero-crossings coincide with the actual zero-crossings. Figure 25.1.3 shows how the amplitude of the desired waveform is generated. Two adjacent ADC samples (S_8 and S_9) are fed to a 2:1 MUX which selects one of the two based on proximity to eye's center. Ideally the value at the center of the eye should be interpolated to provide an estimate of the eye height, however, this increases hardware complexity. The absolute value of the selected sample is averaged using a first-order digital lowpass filter to produce S_{AVE}. Desired references are then generated from S_{AVE} and Φ_{AVE} in a dynamic lookup table with the stored shape of the triangular waveform. We use two different dynamic look up tables so that $d_{ref-1,2}$ correspond to 2 blind samples of ½ UI apart, corresponding to two different reference levels.

We use two Tyco FR4 channels with 9.9 and 13.3dB attenuation at 2.5GHz (26-inch and 34-inch channels) for measurement. Figure 25.1.4 shows the measured learning curves of adaptation engine for these channels. The adaptation converges in less than 80µs. As expected, the DFE coefficients are higher for the channel with higher attenuation.

Figure 25.1.5 shows the measured eye diagrams at the ADC input (analog), ADC output (prior to equalization), and the equalized output for two distinct channels described earlier. The first row shows the eye diagram at the output of the channels. The second row shows the eye diagram at the output of the ADC and prior to the DFE. The third row shows the eye diagram after equalization with adaptive 1-tap DFE (S_{EQ-8} in Fig. 25.1.2). For the 13.3dB channel, the adaptation engine is capable of creating a 320mV opening from a completely closed eye. To generate these eye diagrams, a frequency offset is added to the blind clock. This offset causes the sampling clock to scan the entire input eye once every period of the offset. ADC samples are then overlapped accordingly to reconstruct the eye diagrams.

Figure 25.1.6 shows the jitter tolerance of receiver for PRBS7 with BER<10^{-12} and adapted coefficients for two mentioned channels. Sinusoidal jitter frequencies below 80kHz and above 8MHz could not be applied due to equipment limitations.

The chip micrograph as well as the power and area breakdowns is shown in Fig. 25.1.7. The chip is fabricated in a 65nm CMOS and occupies 0.4mm^2. The receiver operates from 1.2V supply and consumes 192mW, of which 114mW is consumed by the flash ADC and 78mW by the digital CDR and equalization/adaptation.

Acknowledgement:
The authors would like to thank Ravi Shivnaraine for his help with the measurements.

References:
[1] M. Harwood, N. Warke, R. Simpson, et al., "A 12.5Gb/s SerDes in 65nm CMOS Using a Baud-Rate ADC with Digital Receiver Equalization and Clock Recovery," *ISSCC Digest of Tech. Papers*, pp. 436-591, Feb., 2007.
[2] H. Yamaguchi, H. Tamura, Y. Doi, et al., "A 5Gb/s transceiver with an ADC-based feedforward CDR and CMA adaptive equalizer in 65nm CMOS," *ISSCC Digest of Tech. Papers*, pp. 168-169, Feb., 2010.
[3] S. Sarvari, T. Tahmouresadeh, A. Sheikholeslami, et al., "A 5Gb/s Speculative DFE for 2x Blind ADC-based Receivers in 65-nm CMOS," *IEEE Symposium on VLSI Circuits,* pp. 69-70, June, 2010.
[4] O. Tyshchenko, A. Sheikholeslami, H. Tamura, et al., "A 5Gb/s ADC-Based Feed-Forward CDR in 65nm CMOS," *IEEE J. Solid-State Circuits,* vol. 45, no. 6, pp. 1091-1098, June, 2010.

 978-1-61284-302-5/11/$26.00

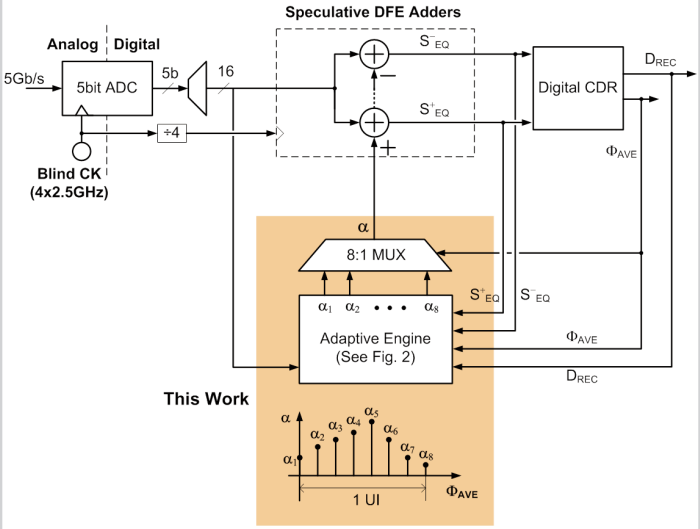


Figure 25.1.1: Adaptive DFE for 2× blind ADC-based receiver.

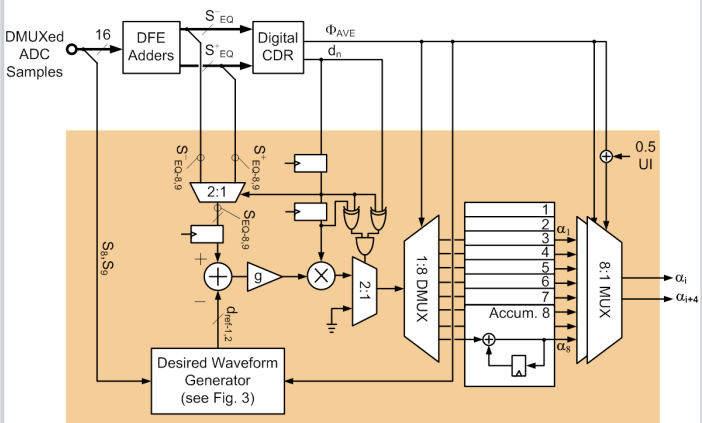


Figure 25.1.2: Adaptation engine implementation.

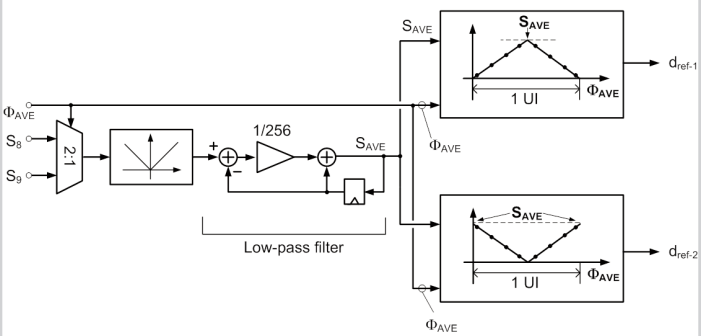


Figure 25.1.3: Desired waveform generator: desired levels produced based on average phase.

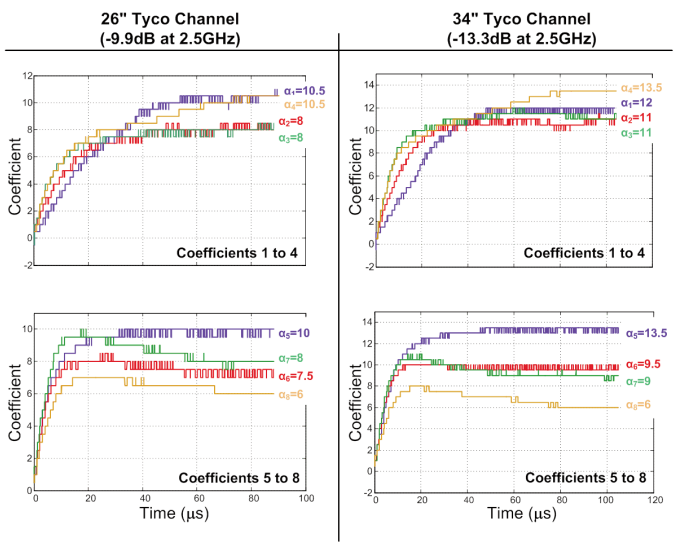


Figure 25.1.4: Measured learning curves for 26” and 34” Tyco channels.

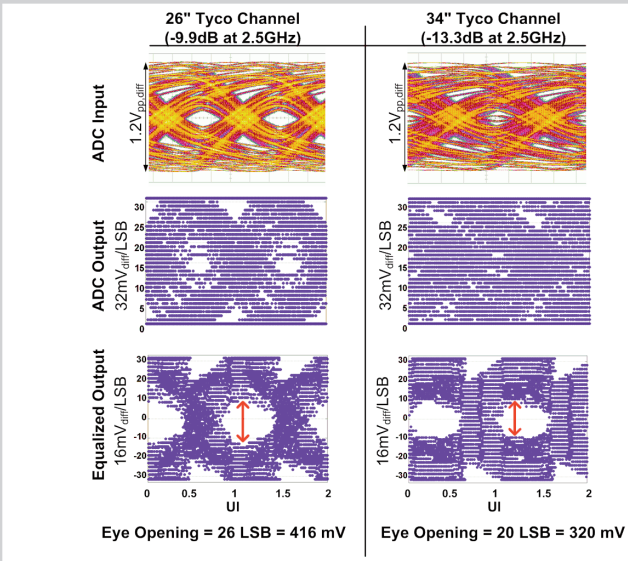


Figure 25.1.5: Measured eye diagrams for a 26” and 34” Tyco channels.

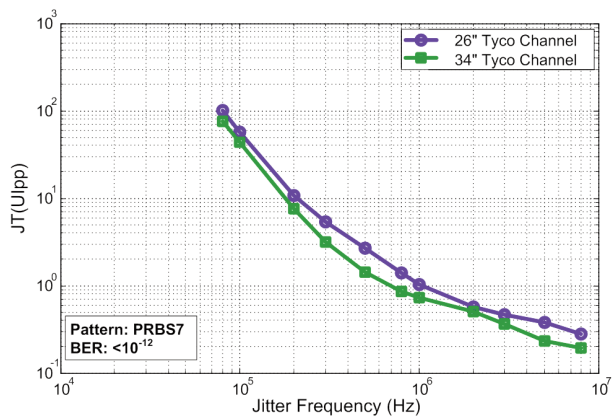
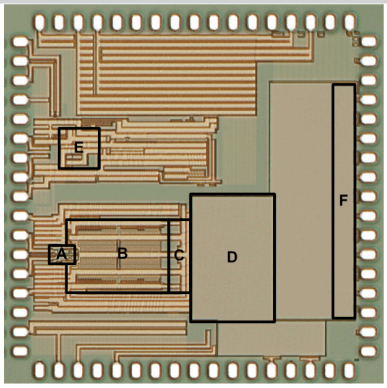


Figure 25.1.6: Measured jitter tolerance for 26” and 34” Tyco channels.



Process	65-nm CMOS
Data Rate	5 Gb/s
Supply	1.2V
ADC Power	114mW
Digital Power	78mW
Total Power	192mW

A	Input Buffers	$50\times60\mu m^2$
B	4 × 2.5GSa/s ADC	$400\times490\mu m^2$
C	4:16 DeMUX	$60\times490\mu m^2$
D	Digital CDR/DFE + Test Structures	$420\times640\mu m^2$
E	BGR and Bias Gen.	$170\times140\mu m^2$
F	Pad Drivers	$60\times1200\mu m^2$

Figure 25.1.7: Die micrograph.

978-1-61284-302-5/11/$26.00