Special Issue Papers

A Pulse-Based, Parallel-Element Macromodel for Ferroelectric Capacitors

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***Abstract*—A pulse-based behavioral model is proposed and implemented in HSPICE. Hysteresis-loop and pulse measurement results are used to extract the model parameters. The model accurately predicts the bitline voltage of a ferroelectric memory testchip.**

I. Introduction

A UNIVERSAL, physically based model is essential in designing any integrated circuit using ferroelectric capacitors. Such a model does not exist to date mainly due to the complexity of FE capacitor characteristics. As a result, researchers have focused on behavioral modeling of FE capacitors as a short-term solution to ferroelectric circuit simulations [1]–[6]. A behavioral model can be implemented as a macromodel using elements such as voltage-controlled capacitors, switches, and resistors.

Behavioral models of ferroelectric capacitors can be classified as either pulse-based models or hysteresis-based models [2]. This classification relies on the observation that the FE capacitor behaves differently in response to high-frequency and low-frequency voltage waveforms. Pulse-based models are appropriate for higher-frequency voltage waveforms with pulse widths on the order of 100 ns. These are the types of waveforms observed in a typical ferroelectric memory read/write access. Hysteresis-based models, however, are appropriate for sinusoidal steady-state analysis of ferroelectric capacitors with voltage waveforms in the 1 kHz range. From the implementation point of view, pulse-based models require a more complicated measurement scheme compared to the hysteresis-based models. In this paper, we propose a unified approach that takes advantage of the simplicity of the hysteresis-based models and the accuracy of the pulse-based models for ferroelectric memory circuit simulations.

One example of a pulse-based model is the Zero Switching-Time Transient model [4]. This model provides good accuracy for large-signal circuit simulations of ferroelectric memories. However, it is relatively complicated to implement. In fact, the control circuitry that implements switches in the model consumes a substantial fraction of the simulation time.

One example of a hysteresis-based model is the parallel-element model proposed by Jiang *et al.* [1]. Unlike other hysteresis-based models, the parallel-element model employs measurement data from both major and minor hysteresis loops. This results in a more accurate behavioral model but at the cost of higher complexity (more components) and longer simulation time. In addition, the model could overestimate the capacitor charge in pulse-based simulations [4].

We propose a unified approach based on these two examples. We offer a methodology that reduces the complexity of the parallel-element model (i.e., reduces the number of parallel elements) while increasing the model accuracy for pulse-based simulations. We implemented the proposed model in HSPICE [7] and demonstrated its accuracy in predicting the bitline voltage in a ferroelectric memory array testchip.

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II. Methodology

The parallel-element model is based on hysteresis-loop measurements and refined using pulse-based measurements of an FE capacitor. We briefly explain the measurement procedure here to introduce our notations, and we refer the readers to [1] for an extended version of the procedure.

A. Data Collection

A major hysteresis loop and a set of minor hysteresis loops are generated using a triangular voltage waveform across the FE capacitor as shown in Fig. 1. The loop corresponding to the first period of the applied waveform is

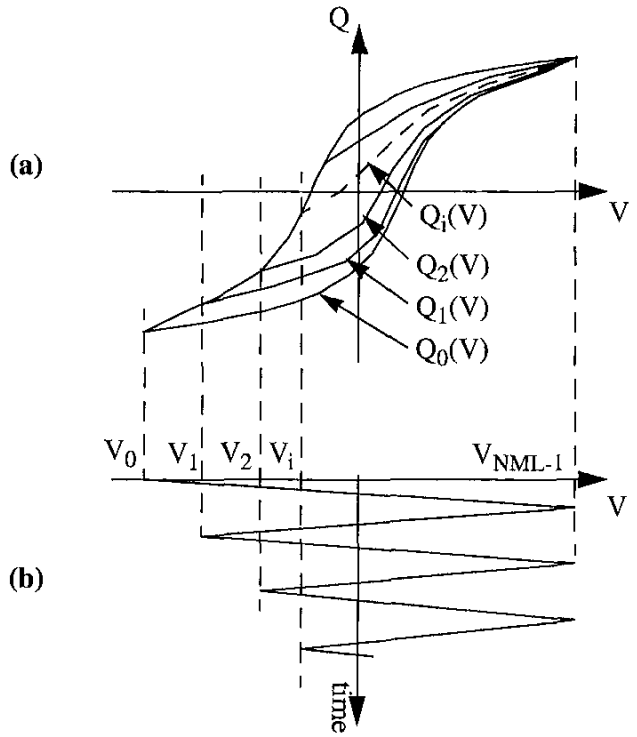

Fig. 1. (a) Major and minor hysteresis loops, (b) voltage waveform applied to the ferroelectric capacitor.

$Q_0(V)$:	Q_{00}	Q_{01}	Q_{02}	.	Q_{0j}	.	$Q_{0(NML-1)}$
$Q_1(V)$:	0	Q_{11}	Q_{12}	.	Q_{1j}	.	$Q_{1(NML-1)}$
$Q_2(V)$:	0	0	Q_{22}	.	Q_{2j}	.	$Q_{2(NML-1)}$
.....	0	0	0	.	.	.	.
$Q_i(V)$:	0	0	0	0	Q_{ij}	.	$Q_{i(NML-1)}$
.....	0	0	.	.	.	.	.
$Q_{NML-1}(V)$:	0	0	0	0	0	0	$Q_{(NML-1)(NML-1)}$

Fig. 2. Matrix Q: each row corresponds to a minor curve of Fig. 1.

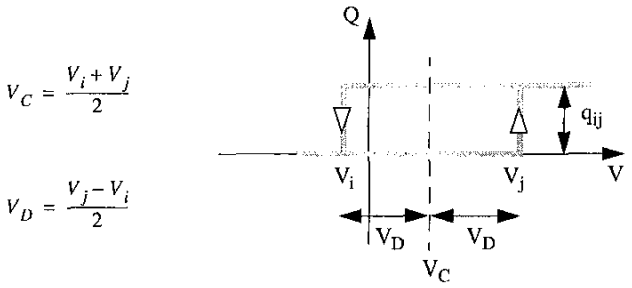

Fig. 3. Q-V characteristic of a switching component C_{ij}.

called the major hysteresis loop, and the loops corresponding to the subsequent periods are called minor loops. Each loop consists of two curves—a top curve and a bottom curve—each represents charge (Q) on the FE capacitor as a function of applied voltage (V). The top curve corresponds to the descending portion of the input voltage; the bottom curve corresponds to the ascending portion of the input voltage. With the voltage pattern of Fig. 1, the top curves of all loops coincide. The bottom curves, however, are different and are numbered from 0 to NML−1; NML denotes the number of minor loops. The i-th curve, denoted by $Q_i(V)$, begins at V_i and ends at V_{NML-1}. The last minor curve, $Q_{NML-1}(V)$, consists of a single point (V_{NML-1}, Q_{NML-1}).

Using samples of $Q_i(V)$ $(0 \leq i \leq \text{NML}-1)$ at discreet voltage values $V = V_j$ $(i \leq j \leq \text{NML}-1)$, we formed a matrix that represents all the minor curves. The samples of $Q_i(V)$ form the i-th row of the matrix as shown in Fig. 2. Note that the matrix rows are numbered from 0 to NML−1. Also note that zero is assigned to all the elements below the diagonal.

Matrix ΔQ is formed by taking the difference between two adjacent elements in the same row of matrix Q. Mathematically:

$$\Delta Q_{ij} = Q_{ij} - Q_{i(j-1)} \qquad i+1 \leq j \leq \text{NML}-1. \tag{1}$$

All the elements on the diagonal and below it are zero. ΔQ_{ij} represents the amount of charge that switches at $V = V_j$, if the initial voltage is V_i; $\Delta Q_{(i+1)j}$ represents the amount of charge that switches at $V = V_j$, if the initial voltage is V_{i+1}. Therefore, the difference between the two represents a charge increment at $V = V_j$ and an equal charge decrement at $V = V_i$. This is equivalent to a small hysteresis loop, shown in Fig. 3, with sharp transitions at V_i and V_j and a switching charge of q_{ij} defined by:

$$q_{ij} = \Delta Q_{ij} - \Delta Q_{(i+1)j}. \tag{2}$$

We define C_{ij} to be a capacitor element (or a switching component) with the Q-V characteristic of Fig. 3. A parallel combination of all C_{ij} elements [a total of NML (NML−1)/2 elements] form a parallel element model. When the voltage across the FE capacitor changes from V_{initial} to V_{final} $(> V_{\text{initial}})$, all the switching components C_{ij} with $V_{\text{initial}} < V_j < V_{\text{final}}$ contribute to the charge increment of the FE capacitor. Similarly, when the voltage across the FE capacitor changes from V_{final} to V_{initial}, all switching components C_{ij} with $V_{\text{initial}} < V_i < V_{\text{final}}$ contribute to the charge decrement of the FE capacitor.

B. Minor Loop Selection

The accuracy of the parallel-element model in reconstructing the original hysteresis loops depends on the NML selected to characterize the FE capacitor. A larger NML results in higher accuracy and higher complexity in terms of the number of elements. For a fixed NML, the model accuracy is affected by the distribution of the starting points of the minor curves. We distinguish two general distributions here, namely, the uniform voltage distribution (UVD) and the uniform charge distribution (UCD).

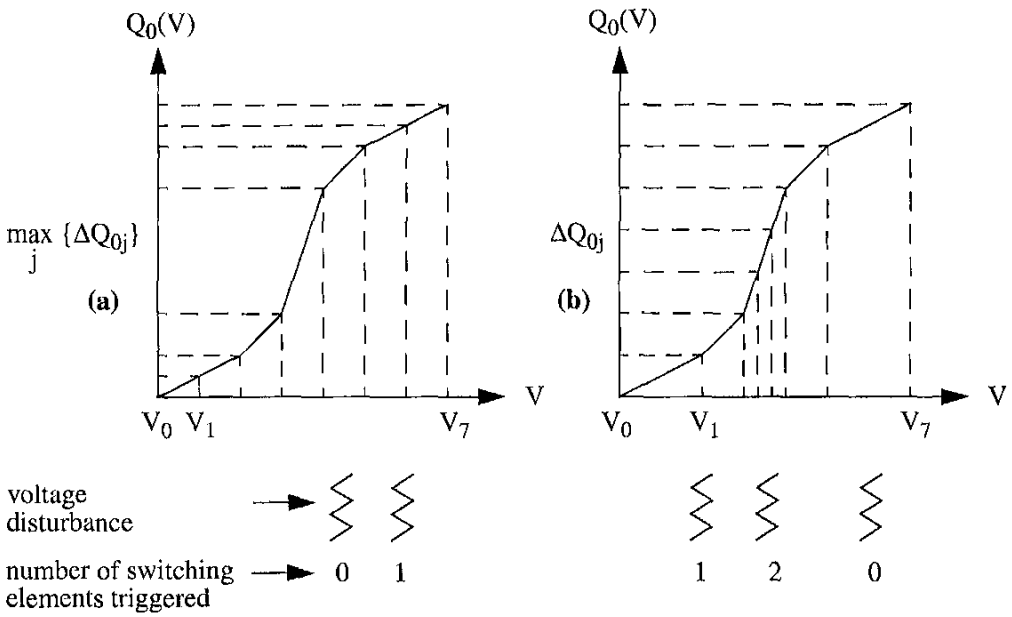

Fig. 4. (a) Uniform voltage distribution generates nonuniform charge intervals on the charge axis; a maximum of one switching element is triggered by a voltage disturbance less than 1V. (b) Uniform charge distribution, a maximum of 2 switching elements are triggered by the voltage disturbance.

In UVD, the starting voltages of the minor curves are uniformly distributed along the voltage axis. In UCD, the starting charges of the minor curves are uniformly distributed along the charge axis. For example, if the major loops extends from -5V to 5V and NML = 11, UVD collects data points on minor curves that begin at -5V, -4V, -3V, ..., 5V.

In UCD, data collection is performed in two steps. In step 1, only a major hysteresis loop is measured. The charge axis is then partitioned uniformly and mapped to the voltage axis to find a nonuniform voltage distribution. In step 2, this nonuniform voltage distribution is used as the starting points of a set of minor curves.

The UCD approach guarantees a maximum charge error that is less than a charge interval on the charge axis. This is independent of where the voltage disturbance falls. The UVD approach, however, is sensitive to where the voltage disturbance occurs, and the simulated charge can differ from the measured charge by as large as the maximum charge interval on the charge axis. Fig. 4 compares the two approaches using a voltage disturbance of less than 1 V. In the UVD approach with a 1 V step, no switching element is triggered if the voltage disturbance falls inside a 1 V interval. Only one switching element is triggered in the best case.

In the UCD approach, the number of switching elements triggered depends on the interval of the voltage disturbance. If the voltage disturbance occurs at a point with high slope, then more than one switching element is triggered. This happens when the voltage disturbance is close to the coercive voltage of the FE capacitor. No switching element is triggered at low-slope points.

The UCD approach provides higher accuracy for the same number of elements in the model. Or, to state it differently, the UCD approach requires fewer elements for the same error tolerance.

C. Small-Signal Capacitance

The parallel element model does not respond to any voltage disturbance that is smaller than a minimum voltage step. This is because there is one-to-one correspondence between the voltage step and the voltage width of the Q-V characteristic of a switching component. This effect is apparent during reconstruction of a major hysteresis loop using the model. As the voltage across the capacitor increases to reach its peak, so does the number of elements that contribute to the total charge increment. When the voltage reaches its peak and begins to fall off, there is a time period for which the capacitor charge stays constant. This is until the voltage falls off by at least one voltage step. The reason is that a switching element would switch back only if the voltage across it falls by at least 2 V_D (refer to Fig. 3). The hysteresis loop reconstructed in this manner looks flat at both ends. In fact, this phenomenon is observed at any point in which the applied voltage changes course.

To investigate this further, let us construct a parallel-element model for a linear capacitor with $C = 1$fF. Using (1) and (2), and assuming a voltage step of 1 V, one can verify that q_{ij} is equal to 1fC for $j = i + 1$ and 0 otherwise. That is, only the subdiagonal elements of the C matrix are nonzero. Fig. 5 compares the original capacitor characteristic with the simulated characteristic of the capacitor based on the parallel-element model. The simu-

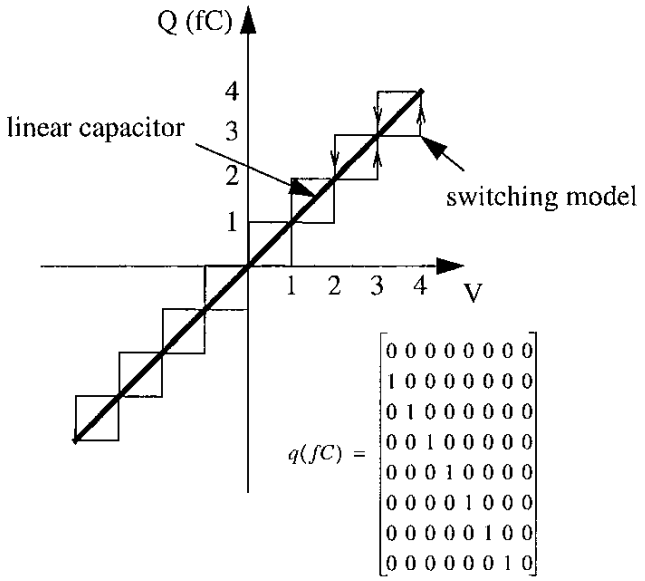

Fig. 5. Approximating a linear capacitor by a parallel combination of switching elements. Charge is expressed in units of femto-Coulombs.

lated characteristic of the capacitor has an echelon form that translates into a small-signal capacitance of zero at nontransitional points. This is expected due to the hysteresis nature of each parallel element in the model.

To remedy the situation, we observe that both switching and nonswitching elements can contribute to the subdiagonal elements of the C matrix. There is little contribution from the switching elements if the voltage steps in characterizing the capacitor are small. Therefore, we introduce little error by treating the subdiagonal elements as nonswitching elements only. However, we obtained a nonzero small-signal capacitance that is very close to the actual small-signal capacitance of the FE capacitor.

D. Pulse-Based Modeling

The methodology explained so far is based entirely on the hysteresis loop measurements, using a Sawyer-Tower circuit with a 100 Hz sinusoidal or triangular input waveform as shown in Fig. 6. Hysteresis-loop measurements tend to overestimate the switching charge of a ferroelectric capacitor for a ferroelectric memory [4]. This is attributed to the low frequency of the applied voltage and its low slew rate, in the order of 2 V/ms. To determine the overestimation factor by the hysteresis loop, we performed two series of measurements: the hysteresis-based measurements and pulse measurements, both using the Sawyer-Tower circuit.

The hysteresis loop uses a 100 Hz triangular waveform, shown in Fig. 6(b), whereas the pulse-measurement uses a PUND sequence [8] with 5 μs pulse-width and 5V/100 ns slew rate, shown in Fig. 6(c). In each case, the switching and the nonswitching charge of the capacitor is plotted against the peak value of the applied voltage in Fig. 7. The hysteresis-based nonswitching charge closely follows the pulse-based nonswitching charge. The hysteresis-based

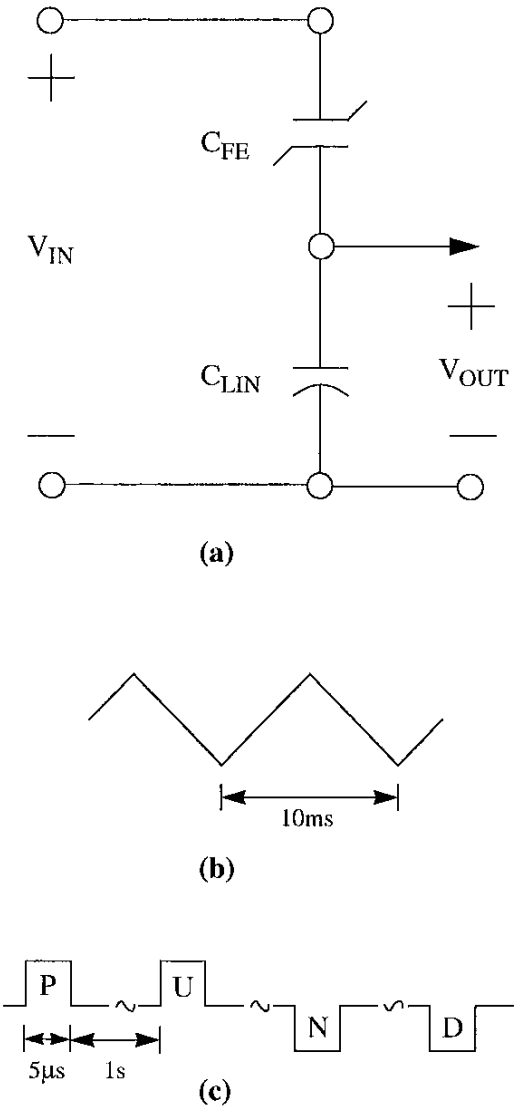

Fig. 6. (a) Sawyer-Tower circuit (b) input voltage waveform for hysteresis-loop measurement, (c) input voltage waveform for pulse measurement.

switching charge, however, overestimates the pulse-based switching charge by 30%. In other words, if we were to design a ferroelectric memory based on the hysteresis loop only, we would estimate the capacitor area to be 75% $(1/1.3 * 100\%)$ of its optimum value. Based on this result, we decided to include a heuristically determined reduction factor of 0.7 for the switching components derived from the hysteresis loop. We incorporate this factor into the model in Section IV to accurately predict the capacitor behavior in a ferroelectric memory array.

III. Model Implementation

The parallel-element model consists of the parallel combination of switching components, each having a Q-V characteristic shown in Fig. 3. In this section, we develop a

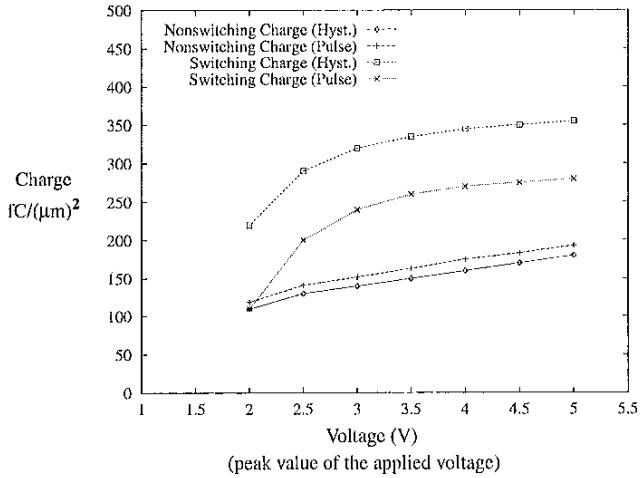

Fig. 7. The hysteresis-based nonswitching charge closely follows its pulse-based counterpart; the hysteresis-based switching charge overestimates its pulse-based counterpart by 30%.

macromodel for a switching component using predefined elements in HSPICE.

We modeled a switching component by a series combination of a voltage controlled resistor (VCR) and a voltage-controlled capacitor (VCC) as shown in Fig. 8. The VCR characteristic is centered around 0V with a width of V_D on each side [Fig. 8(b)]. Ideally, the VCR must act as an open circuit in the center region and as a short circuit on the side region. The VCC characteristic is centered around V_C and must ideally have zero width [Fig. 8(c)]. We explain the operation of this series combination under these ideal conditions.

Assume that both VCC and VCR experience 0 V initially, which means the VCR acts as an open circuit and conducts zero current. If the applied voltage increases gradually, but less than V_D, all this voltage appears across the VCR because it acts as an open circuit. When the applied voltage increases beyond V_D, the VCR acts as a short circuit and allows the VCC to experience the remaining voltage. The remaining voltage, however, has to exceed V_C in order to see a nonzero capacitance, which happens when the applied voltage reaches $V_D + V_C$. At this voltage, the total charge on the capacitor changes from 0 to q_{ij}. Beyond $V_D + V_C$, there is no change in the capacitor charge as the capacitance is reduced to zero. This verifies the transition of q_{ij} at $V = V_j$ in Fig. 8(d).

Assume now that the applied voltage changes course and gradually reduces to zero. As soon as the applied voltage begins to decrease, the voltage across the VCR becomes less than V_D and the VCR turns off because the voltage across the VCC cannot change unless the current flows in the opposite direction. When the applied voltage reduces by 2 V_D from its peak, the VCR turns on and allows current to flow in the opposite direction. When the applied voltage reaches $V_C - V_D$, the negative charge transition occurs. This corresponds to $V = V_i$ of Fig. 8(d).

A. VCC Implementation

The voltage-controlled capacitance $C(V)$ [refer to Fig. 8(c)] must satisfy the following condition:

$$\int_{(V_C-\varepsilon)}^{(V_C+\varepsilon)} C(V)\,dV = q_{ij} \tag{3}$$

where ε is a small positive voltage. Moreover, $C(V)$ must be zero outside the integral range. In other words, the total charge increment due to the voltage increment across the VCR should be equal to q_{ij}. Also, for the feasibility of implementation in HSPICE, the function must be smooth with as many continuous higher-order derivatives as possible. This provides a convergent solution in shorter simulation time. We have chosen the following function as $C(V)$:

$$C(V) = \frac{C_{\max}}{1 + \left(\frac{V - V_C}{\alpha V_D}\right)^2} \tag{4}$$

where α is a positive number that determines the width of the capacitor characteristics. $C(V)$ has a maximum of $C_{\max}$ at $V = V_C$ and reduces to half of its maximum at $V = V_C \pm \alpha V_D$. Applying the constraint expressed in (3) to this function, we have:

$$q_{ij} = \pi \alpha V_D C_{\max} \tag{5}$$

This equation states that, for fixed q_{ij} and V_D, $\alpha C_{\max}$ must be kept constant. A capacitor with larger α results in a smaller $C_{\max}$ or, equivalently, smaller slopes of transitions at V_i and V_j.

B. VCR Implementation

Fig. 9 shows a VCR implementation in HSPICE using a voltage-controlled current source (VCCS). In the center region, the current is zero, hence providing an infinite resistance. In the side regions, the current jumps to a value beyond the current level consumed by the peripheral circuitry. In other words, the VCCS provides as much current as the peripheral circuitry requires. This guarantees the voltage across the VCR to be fixed at $-V_D$ or $+V_D$ when the voltage across the series combination of Fig. 8(a) is below $-V_D$ or above V_D, respectively. This characteristic is symbolized by two back-to-back diodes in Fig. 8(a) in which each diode has a forward voltage of V_D. A direct implementation of the VCR, instead of using a VCCS, is possible but less attractive due to nonconvergent HSPICE simulation results.

IV. Simulation Results

The macromodel implementation of the parallel element model as described in this paper accurately reconstructs the original hysteresis loop as shown in Fig. 10. Both the measured and the simulated hysteresis loops are obtained

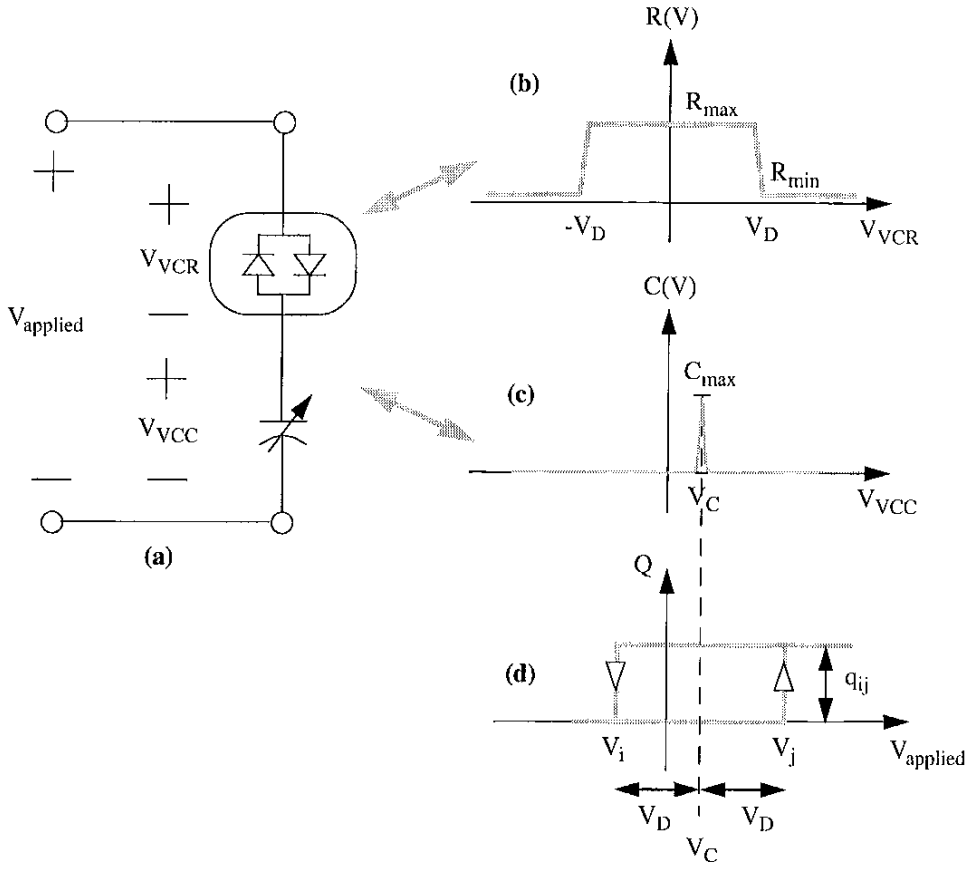

Fig. 8. (a) A series combination of a voltage-controlled resistor (VCR) and a voltage-controlled capacitor (VCC) forms a switching component q_{ij}. (b) VCR characteristic is centered around 0 V and has a width of V_D. (c) VCC characteristic is centered around V_C and ideally has a width of 0 V. (d) The combined characteristic of the VCR and the VCC in series is equivalent to the characteristic of the switching component q_{ij}.

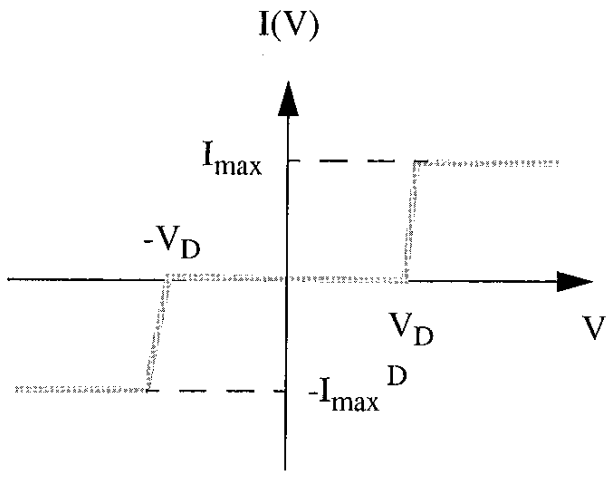

Fig. 9. An HSPICE implementation of the VCR of Fig. 8(b).

using the same Sawyer-Tower circuit. The frequency of the applied waveform is 100 Hz.

Next, we refined the model by inserting a reduction factor of 0.7 for all C_{ij} with $i+2 \leq j \leq \text{NML}-1$. This factor is determined heuristically, as explained earlier in this paper, to account for the overestimation of the switching charge by hysteresis-loop measurements. The refined model is then used to predict the bitline voltage of a ferroelectric memory array, shown in Fig. 11(a). The bitline voltage is observed through a PMOS transistor after a low-precharged bitline is shorted to a memory cell storing a digital 1 or a digital 0. This experiment is repeated over a range of power supply voltage, V_{DD}, with the wordline driven by $V_{DD}+2V$. The final simulation results and measurement results are compared on Fig. 11(b). The simulation results for both digital 1 and digital 0 are within 10% of the measurement results.

V. Conclusions

A unified approach that combines the simplicity of a hysteresis-based modeling with the accuracy of pulse-based modeling was presented in this paper. The unified approach was used to implement a macromodel for HSPICE in which a 90% accuracy was obtained in simulating a ferroelectric memory array testchip.

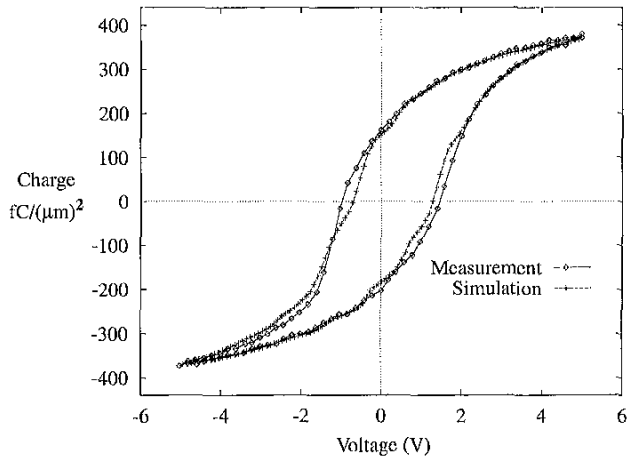

Fig. 10. Reconstruction of the hysteresis loop using the parallel-element model.

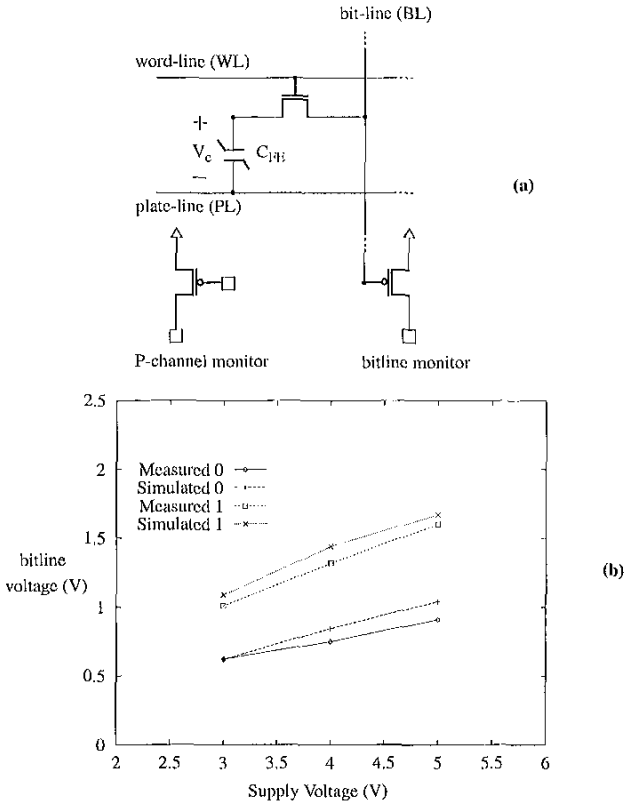

Fig. 11. (a) Ferroelectric test array architecture, (b) simulation results versus the measurement results for the bitline voltage.

Acknowledgements

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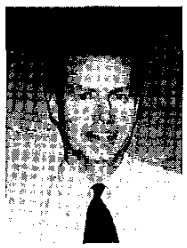
Dr. Sheikholeslami is a co-author for several journal and conference papers on ferroelectic memory design and modeling as well as multiple-valued memories. He was granted two U.S. patents in the area of content-addressable memories in 1998 and 1999.



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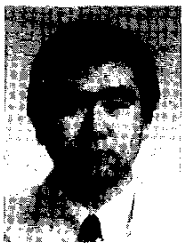

Hideki Takauchi was born in Tokyo, Japan, on January 15, 1966. He received the B.S. and M.S. degrees from Waseda University, Tokyo, in 1988 and 1990, respectively. In 1990, he joined Fujitsu Laboratories Ltd., where he was engaged in research on high-temperature superconductor devices and other oxide devices, including ferroelectric nonvolatile memories. Since 1996, he has been working on CMOS circuit design. His current research interests include high-speed I/O interface design and chip-to-chip communication. He is a member of the Japan Society of Applied Physics.

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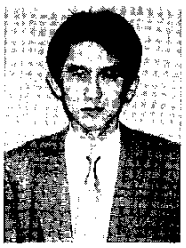

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