A 5Gb/s Speculative DFE for 2x Blind ADC-based Receivers in 65-nm CMOS

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Abstract

This paper presents the design of a DFE for a 2x blind ADC-based RX. The DFE is implemented in 65-nm CMOS along with a 2x blind CDR and ADC. Our measured results confirm 5Gb/s data recovery with BER less than 10^{-12} with a channel introducing 13.3dB of attenuation at the Nyquist frequency of 2.5GHz. Without the DFE, the BER exceeds 10^{-8}.

Keywords: speculative DFE, blind sampling, ADC-based receiver and CMOS

Introduction

An ADC-based receiver converts the incoming analog signal to its digital counterpart in order to enable significant equalization in the digital domain, especially at higher data rates where the channel loss is severe [1][2]. The architecture proposed in [1] uses a *blind* clock (at twice the baud rate) for the ADC to sample the incoming signal and feeds these digital samples to a feed-forward equalizer (FFE) to remove the inter-symbol interference (ISI). An FFE, however, is known to suffer from noise enhancement and, as such, is inferior to a non-linear equalizer such as a decision-feedback equalizer (DFE). This paper presents for the first time a DFE for 2x blind ADC-based receivers.

Fig. 1 compares a DFE in a *phase-tracking* receiver (RX) with a DFE in a *blind* RX. In a phase-tracking RX, the DFE relies on the recovered clock from the incoming signal for its operation [2]. In a blind ADC-based RX, however, there is no recovered clock [1]; the sampling clock is totally blind. This makes the task of DFE design nontrivial as the samples of the incoming signal no longer correspond to the centre of the eye or to any specific data phase. Moreover, the locations of the samples change during the operation of the receiver (e.g. due to low-frequency jitter) necessitating variable DFE coefficients.

Proposed DFE Scheme

Fig. 2 illustrates the proposed DFE scheme. Fig. 2 (left) shows the *actual* pulse response of the channel corresponding to UI_{n-1}; the tail of this signal stretches over the next UI (UI_n) due to the limited bandwidth of the channel. The *desired* pulse response is derived such that the sum of two consecutive pulses results in an approximately constant value. The shaded area depicts the ISI; the amount of this ISI is a function of the sampling time. Therefore, as shown in Fig. 2 (right), the proposed DFE divides the nominal UI into 8 equal intervals, $I_{[0:7]}$, and assigns one coefficient to each interval. These coefficients, $\alpha_{[0:7]}$, represent the interference from b_{n-1} in $I_{[0:7]}$. During the operation of the RX, the DFE uses the average transition phase, Φ_{AVG}, recovered by the clock and data recovery (CDR) [1] to select two coefficients among 8, which correspond to the sampling time. Φ_{AVG1}, the modulo-1UI version of Φ_{AVG}, indicates the distance between the second sample of the current UI, S_2, and the next nominal UI boundary. As an example, Fig. 2 (right) illustrates the case where S_2 falls in I_2, hence α_6 and α_2 will be used for S_1 and S_2, respectively.

Fig. 3 depicts the full-rate implementation of the proposed RX in a simplified block diagram. Two ADC samples of the current UI, $S_{[1:2]}$, along with one delayed sample of the previous UI, S_0, form the 3 consecutive samples, $S_{[0:2]}$, needed by the CDR to recover b_n [1]. The DFE Coefficient Selector (DCS) uses the current value of Φ_{AVG} to select the two coefficients, $c_{[1:2]}$, which correspond to the location of $S_{[1:2]}$ from $\alpha_{[0:7]}$. These coefficients are multiplied by the sign of b_{n-1} to generate the correction terms (ISI replica) $\delta_{[1:2]}$ for $S_{[1:2]}$. The correction term for S_0, δ_0, is generated by multiplying c_2 (ignoring the change of Φ_{AVG} in 1UI) by the sign of b_{n-2}. $\delta_{[0:2]}$ are subtracted from $S_{[0:2]}$ to remove the post cursor ISI, and the resulting ISI-free samples, $d_{[0:2]}$, are used by the CDR to recover b_n and update Φ_{AVG}.

Receiver Architecture

To accommodate 5Gb/s operation, the proposed DFE employs loop-unrolling (*speculative*) architecture in a *deMUXed-by-8* RX. Fig. 4 shows the block diagram of the entire receiver. The received signal is sampled by four time-interleaved 2.5GS/s 5-bit ADCs to generate 10GS/s corresponding to 2 samples per UI. A 4:16 demultiplexer (deMUX) feeds 16 samples of an 8-UI frame, $S_{[1:16]}$, to the digital DFE/CDR. These 16 samples along with one delayed sample from the previous frame form $S_{[0:16]}$. Since Φ_{AVG} is constant throughout the entire 8-UI frame, c_1 and c_2 are used as the selected DFE coefficients respectively for all odd- and even-numbered ADC samples. The ISI Subtractor adds/subtracts $c_{[1:2]}$ to/from $S_{[0:16]}$ to produce the raw speculative data, $d_{[0:16]}^0$ and $d_{[0:16]}^1$, which are later used by 8 parallel Phase Detection and Data Decision arrays (PD/DD). Each PD/DD array processes the information of one UI in a 4 PD/DD Unit structure (shown in the inset) and generates the 4 possible values of instantaneous phase and recovered bit, $(\Phi_X, b)^{[1:4]}$. Eight 4:1 multiplexers (MUXes) follow the PD/DD arrays to select the final recovered bits, $b_{[1:8]}$, and final recovered instantaneous phases, $\Phi_{X[1:8]}$. This MUX operation requires the last two bits of the previous frame as shown. Finally, $\Phi_{X[1:8]}$ are fed to the average phase recovery block to update Φ_{AVG} for the next 8-UI frame.

Experimental Results

To experimentally verify the DFE performance, we fabricated the RX in Fujitsu's 65-nm CMOS. We used 2^7-1 PRBS generated by a Centellax board at 5Gb/s. This data is boosted by a broadband amplifier to use the entire $1V_{PP,diff}$ input range of the ADCs. In one test setting, the PRBS data after 4dB of boost is fed to the test-chip through a probe card. Fig. 5 (left-top) shows the eye diagram of the signal at the probe card input. To verify the ADC functionality we set the RX sampling clock at 5.001GHz and saved 500,000 deMUXed ADC samples at one deMUX output using a logic analyzer. Fig. 5 (left-bottom) shows the eye diagram generated by rearranging these samples according to the 1MHz frequency offset, verifying ADC functionality. For BER and jitter

tolerance measurements, our test channel included a 5"-24"-5" FR4 backplane with an aggregate attenuation of 13.3dB at 2.5GHz. Fig. 5 (middle) shows the measured S_{21} of the channel. The PRBS data is passed through this channel after 7dB of boost and fed to the test-chip through the probe card. Fig. 5 (right) shows the measured eye diagrams at the probe card input and the deMUX output, confirming that the received eye at the output of the ADC is completely closed. It is from this closed eye that we successfully recover the data.

Fig. 6 presents the simulation and measurement results of the RX. We calculate the DFE coefficients according to the proposed DFE scheme using the measured s-parameters of the test channel; we then quantize them to 5 bits (LSB = 31.3mV) to obtain $\alpha_{[0:7]}$ for simulations and measurements. Fig. 6 (left) depicts the simulated and measured jitter tolerance of the RX with DFE around the bandwidth of the phase recovery loop; without the DFE, the RX fails to achieve the target BER values, thus jitter tolerance is *zero*. For the simulations, we used an event-driven model [3] in Simulink. The BER of 10^{-6} is used for simulations due to simulation time limitations, and no random jitter is added to the TX and RX clocks. In measurements, the BER of 10^{-12} is used, and the total jitter introduced by the setup is 16ps (0.08UI); we added sinusoidal jitter (SJ) up to the frequency of 8MHz (limited by the equipment). Measurements confirm that the RX with DFE recovers data in the presence of up to $0.24UI_{PP}$ of high-frequency SJ. To determine the sensitivity of the receiver BER to DFE coefficients, we scaled the coefficients (before quantizing) by a factor of K and measured the BER. Fig. 6 (right) shows the results of simulations and measurements in which we change K from 0 (no DFE) to 1.6, where K = 1 denotes the optimal DFE coefficients. The simulations were performed for 10^7 bits, thus the minimum measurable BER was 10^{-7}. Measurements confirmed that the BER remains better than 10^{-12} for $0.9 \le K \le 1.1$ but increases above 10^{-11} for K = 0.8. Outside this range, the BER is worse than 10^{-8} (the accurate BER could not be found due to saturation of error counters).

Fig. 7 shows the performance summary and die photo. The synthesized logic and deMUX together consume 57.6mW. The entire receiver consumes 211.2mW and, excluding the test structures, occupies $0.3741mm^2$.

References

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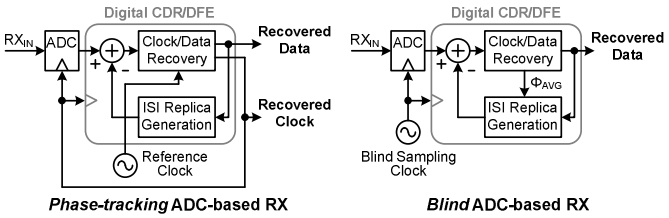

Fig. 1. Phase-tracking and blind ADC-based receivers using DFE.

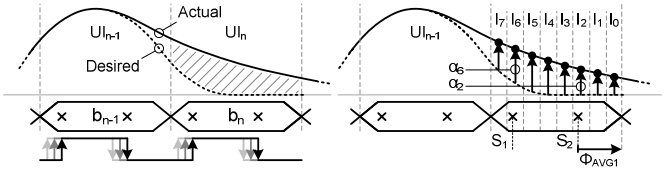

Fig. 2. Sampling intervals determine DFE coefficients.

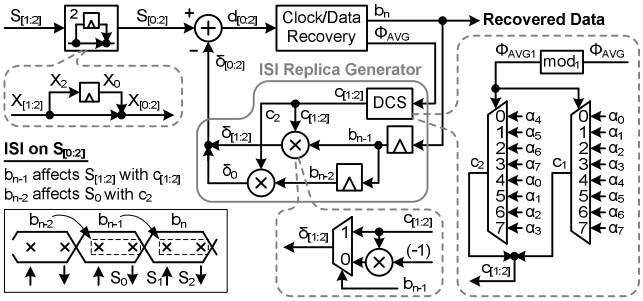

Fig. 3. Simplified block diagram of the RX with the proposed DFE.

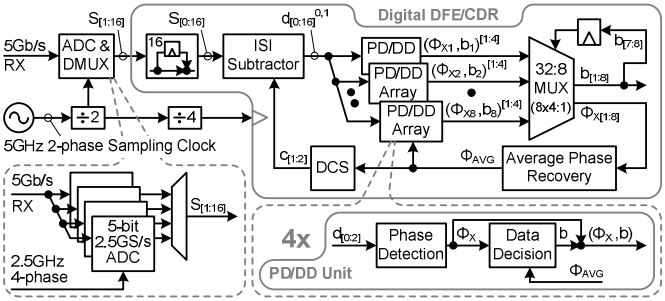

Fig. 4. The entire *deMUXed-by-8* RX with the *speculative* DFE.

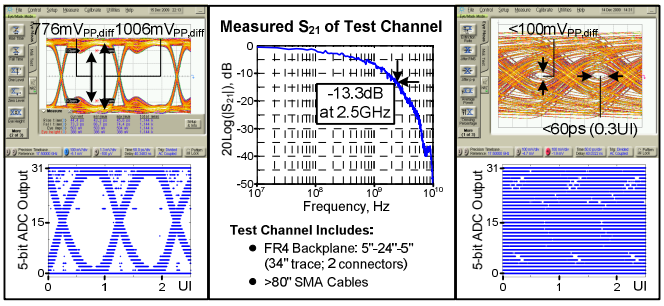

Fig. 5. Measured eye diagrams and S_{21} of the test channel.

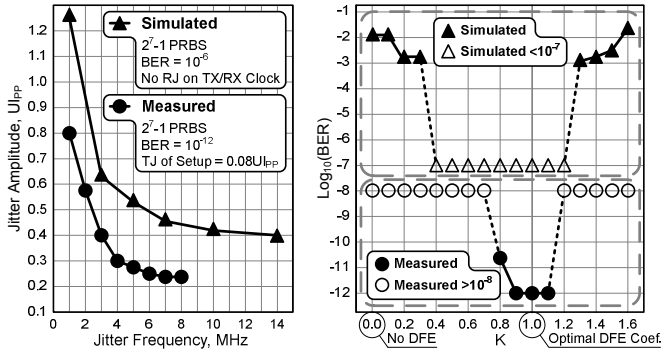

Fig. 6. Simulated and measured jitter tolerance and BER of the RX.

Process	CMOS65	Receiver	Total Power (Incl. Test Structures)	211.2 mW	
Data Rate	5 Gb/s		Total Area (Excl. Test Structures)	0.3741mm²	
Supply	1.2 V				
Analog Front-End (Customized Layout)		A	BGR & Bias Gen.	170x140μm²	
		B	Input Buffers	50x60μm²	
		C	4x 2.5GS/s ADCs	400x490μm²	
		D	4:16 DeMUX	60x490μm²	
Digital Cells (Synthesized)		E	Test Structures	0.0510mm²	
		F	Digital DFE/CDR	0.1219mm²	

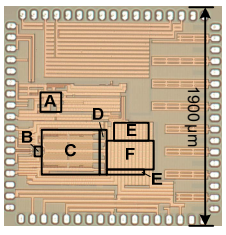

Fig. 7. Performance summary and die photograph.