Project 2 ECE1371S

1) Charge injection

Your task is to investigate charge injections effects in a fully-differential switched-capacitor integrator. For your simulations, all elements can be ideal except for switches and clock waveforms. Simulate using the 0.18um technology in the typical process and 1.6V power supply and 80 degrees C. Assume each differential sampling capacitor is 1pF and clock-rate is 1MHz. Choose switch sizes so it settles to 12 bit accuracy. The diff input signal level should be 1.0V pp with a common mode voltage of 0.8V. The input common-mode of the opamp should be set to 0.4V.

Compare ...

a) A parasitic sensitive delaying integrator

b) A parasitic insensitive delaying integrator where the input switch is advanced

c) A parasitic insensitive delaying integrator where the ground switch is advanced

d) A parasitic insensitive non-delaying integrator where the virtual ground switch is advanced.

You need to develop a test bench so you can look at the distortion due to charge injection in these designs. You can choose the integrator capacitor value as your goal is to look at the input stage.

2) Pipeline ADC

Your task is to compare 2 approaches for designing a 10-bit pipeline ADC.
- Approach 1: 1 bit resolved per stage
- Approach 2: 2 bits resolved per stage
(both approaches use digital error correction so they should resolve more than the number of bits per stage than those shown above)

- Assume no calibrations are required and design for 50MS/s and minimize power consumption

The design is in a 0.18um CMOS process with a 1.8 V (nominal) power supply.

Simulate only the first 2 stages. The load of the second stage should be the expected input load of the third stage (you do not need to design the entire third stage)

- Simulate the first 2 stages in spice and take the digital and residue outputs and put them into matlab to determine the performance of the first 2 stages.

- Assume a constant bias current of 50uA is available.

- Design over typical, fast and slow process corners and +/- 10% power supply variation at a fixed temperature of 80 degrees C. For typical, use 1.8V, for fast, use 2.0V, for slow, use 1.6V (3 design corners).

- Assume capacitor absolute values do not vary but add 10% parasitic capacitance on each side of any capacitor you use. Assume resistor absolute values vary by 20% but they match perfectly.

- Assume a high impedance differential reference voltage is available (in other words, you need to buffer the reference voltage). You can decide on the voltage levels.