Project 3 Oversampling ADC ECE1371S

1a. Use the DS (Delta-Sigma) Toolbox to compare 4th and 5th-order DS ADCs meeting the following requirements: OSR = 16, M = 8 comparators, peak SQNR >= 96 dB, CRFB topology. In each case, select the minimum Hinf needed to achieve the desired SQNR. Construct a table which lists Hinf, the maximum stable input and the -3dB STF bandwidth.

1b. For the fifth-order design, use the DS Toolbox to plot the NTF & STF, example input and output waveforms, example spectrum and the SQNR vs Input level graph. For the example spectrum, be sure to state NBW and also include the theoretical noise spectral density on your plot. (Hint: Use dsexample1.m.)

2a. Draw a block diagram of your fifth-order design and write out its difference equations. Construct a matlab function which simulates those difference equations and verify that your function is correct by i) comparing the open-loop impulse response of the loop filter obtained with the DS Toolbox's impL1 function with the open-loop response produced by your function, and ii) running a closed-loop simulation with a -3dBFS sine-wave input and comparing the resulting spectrum with what you obtained in 1b. Also verify that when you do dynamic-range scaling, the integrator swings are limited to ±1. (Suggestion: For your first pass on this problem, skip dynamic-range scaling and debug your code with these simplified coefficients.)

2b. Construct a fully-differential switched-capacitor implementation of the modulator using a 1-V reference voltage plus ideal switches and amplifiers. Scale the coefficients such that the full-scale input level and the integrator differential output is 2Vpp. Verify your design using both open-loop and closed-loop simulations in SPICE/Spectre. Compute the first-stage capacitor sizes that result in -83dBFS in-band thermal noise assuming the only noise source is kT/C noise from each switched capacitor. (For the ideal switches and amps, it may be beneficial to use small resistors in the switches and bandwidth limited amplifiers since SPICE/Spectre may have a difficult time with extremely small time-constants).

2c. Leaving everything else ideal, replace the first stage opamp with a transistor opamp using the 0.18um CMOS process, a 1.6V power supply, a fixed temperature of 80 degrees C and a clock frequency of 50 MHz. Design for minimum power consumption. Assume a constant bias current of 50uA is available and check your design over process corners. Describe techniques that you used to keep your simulation times short/ reasonable.