Continuous-Time Filters

David Johns and Ken Martin
University of Toronto
(johns@eecg.toronto.edu)
(martin@eecg.toronto.edu)

Motivation

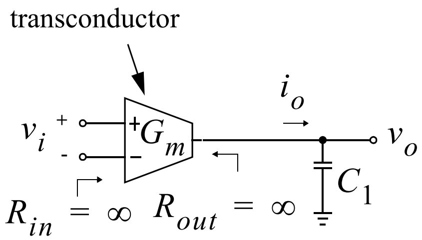
Switched-capacitor filters

+ Accurate transfer-functions
+ High linearity, good noise performance
- Limited in speed
- Requires anti-aliasing filters

Continuous-time filters

- Moderate transfer-function accuracy (requires tuning circuitry)
- Moderate linearity
+ High-speed
+ Good noise performance

G_m-C Integrators



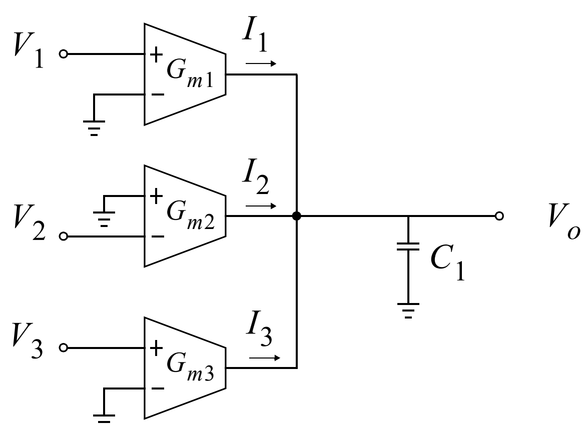
$$V_o = \frac{I_o}{sC_1} = \frac{G_m V_i}{sC_1} \equiv \left(\frac{\omega_{ti}}{s}\right) V_i$$

$$\omega_{ti} = \frac{G_m}{C_1}$$

$$i_o = G_m v_i$$

- Use a transconductor to build an integrator
- Output current is linearly related to input voltage
- Output impedance is ideally infinite
- Note — an OTA (operational transconductance amplifier) has a high G_m value but not usually linear.

Multiple-Input G_m-C Integrator



$$V_o = \frac{1}{sC_1}(G_{m1}V_1 - G_{m2}V_2 + G_{m3}V_3)$$

Example

- What G_m is needed for an integrator having a unity-gain frequency of $\omega_{ti} = 20\text{ MHz}$ when $C = 2\text{ pF}$?

$$G_m = 2\pi \times 20MHz \times 2pF$$
$$= 0.251\ mA/V \qquad (1)$$

or equivalently,

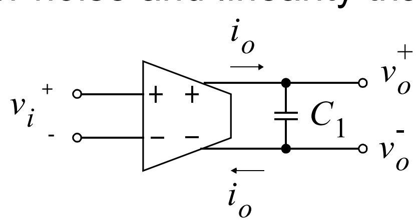
$$G_m = 1/3.98k\Omega \qquad (2)$$

- which is related to unity-gain frequency by

$$2\pi \times 20MHz = \frac{1}{3.98k\Omega \times 2pF} \qquad (3)$$

Fully-Differential Integrators

- Better noise and linearity than single-ended.

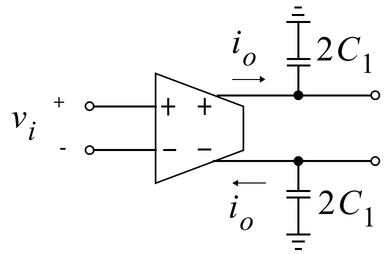


$$v_o = v_o^+ - v_o^-$$
$$i_o = G_m v_i$$

$$V_o = \frac{I_o}{sC_1} = \frac{G_m V_i}{sC_1} \qquad \omega_{ti} = \frac{G_m}{C_1}$$

- Use a single capacitor between differential outputs
- Requires some sort of common-mode feedback to set output common-mode voltage
- Needs some extra caps for compensating common-mode feedback loop.

Fully-Differential Integrators



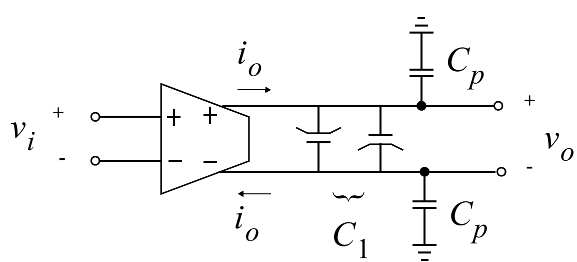
$$V_o^+ = I_o / s(2C_1)$$

$$V_o^- = -I_o / s(2C_1)$$

$$V_o = \frac{2I_o}{s(2C_1)} = \frac{G_m V_i}{sC_1} \qquad \omega_{ti} = \frac{G_m}{C_1} \qquad \begin{aligned} v_o &= v_o^+ - v_o^- \\ i_o &= G_m v_i \end{aligned}$$

- Use 2 grounded capacitors
- Still requires common-mode feedback but compensation caps for common-mode feedback can be the same grounded capacitors

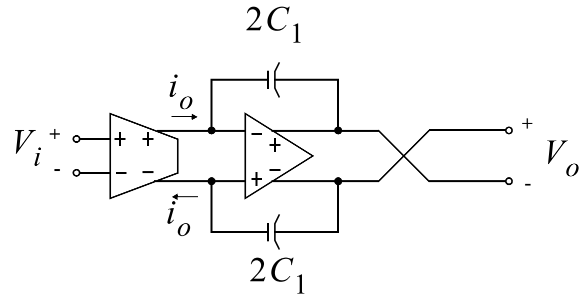
Fully-Differential Integrators



$$V_o = \frac{G_m V_i}{s(C_1 + C_p/2)} \qquad \omega_{ti} = \frac{G_m}{(C_1 + C_p/2)}$$

- Integrated capacitors have top and bottom plate parasitic capacitances.
- To maintain symmetry, usually 2 parallel caps used as shown above
- Note that parasitic capacitance affects time-constant

G_m-C Opamp Integrator



$$V_o = \frac{2I_o}{s(2C_1)} = \frac{G_m V_i}{sC_1} \qquad \omega_{ti} = \frac{G_m}{C_1}$$

- Use an extra opamp to improve linearity and noise performance
- Also known as a “Miller Integrator”

G_m-C Opamp Integrator

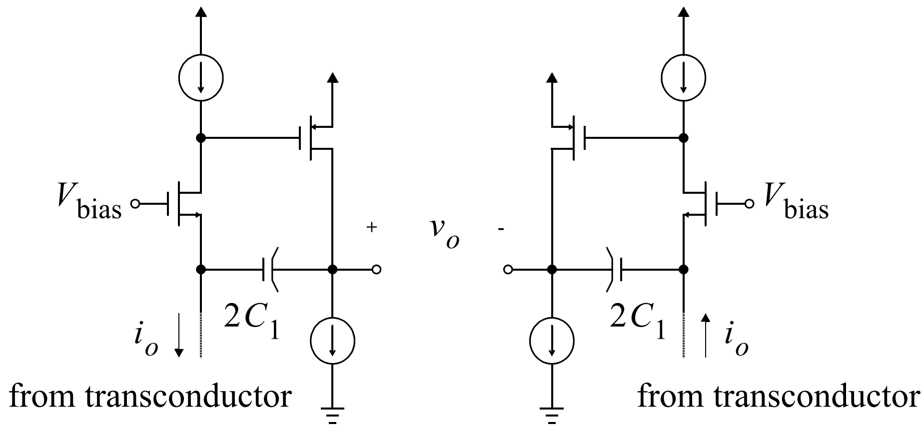
Advantages

- Effect of parasitic caps reduced by opamp gain — more accurate time-constant and better linearity.
- Less sensitive to noise since transconductor output is low impedance (due to opamp feedback).
- G_m cell drives virtual gnd — output-impedance of G_m cell can be lower and smaller voltage swing needed.

Disadvantages

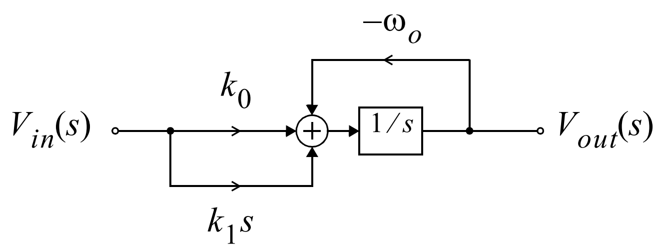
- Lower operating speed because it now relies on feedback
- Larger power dissipation
- Larger silicon area

Example G_m-C Opamp Integrator



- A low input impedance on the order of $2/(g_{m2}^2 r_{ds})$ due to common-gate input impedance and feedback.

First-Order Filter

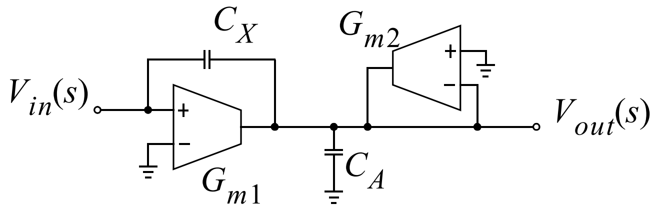


- General first-order transfer-function

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{k_1 s + k_0}{s + \omega_0} \tag{4}$$

- Built with a single integrator and two feedins branches.
- ω_0 sets the pole frequency

First-Order Filter

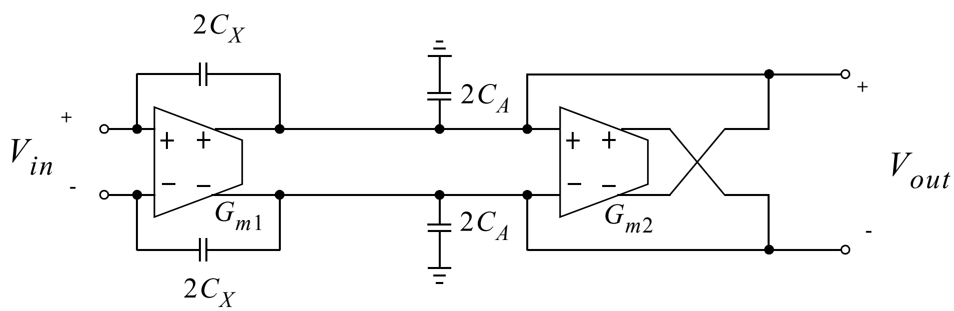


$$C_X = \left(\frac{k_1}{1-k_1}\right) C_A \text{where } (0 \le k_1 < 1) \qquad G_{m1} = k_0(C_A + C_X)$$
$$G_{m2} = \omega_o(C_A + C_X)$$

- Can show that the transfer function is given by

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{sC_X + G_{m1}}{s(C_A + C_X) + G_{m2}} = \frac{s\left(\frac{C_X}{C_A + C_X}\right) + \left(\frac{G_{m1}}{C_A + C_X}\right)}{s + \left(\frac{G_{m2}}{C_A + C_X}\right)} \qquad (5)$$

Fully-Differential First-Order Filter



$$C_X = C_A\left(\frac{k_1}{1-k_1}\right) \text{where } (0 \le k_1 < 1) \qquad G_{m1} = k_0(C_A + C_X)$$
$$G_{m2} = \omega_o(C_A + C_X)$$

- Same eqns as single-ended case but cap sizes doubled
- Can realize $k_1 < 0$ by cross-coupling wires at C_x.

Example

- Find fully-diff values when dc gain = 0.5, a pole at $20MHz$ and a zero at $40MHz$. Assume $C_A = 2pF$.

$$H(s) = \frac{0.25(s + 2\pi \times 40MHz)}{(s + 2\pi \times 20MHz)} = \frac{0.25s + 2\pi \times 10MHz}{s + 2\pi \times 20MHz} \quad (6)$$

$$k_1 = 0.25, \; k_0 = 2\pi \times 10^7, \; \omega_o = 4\pi \times 10^7 \quad (7)$$

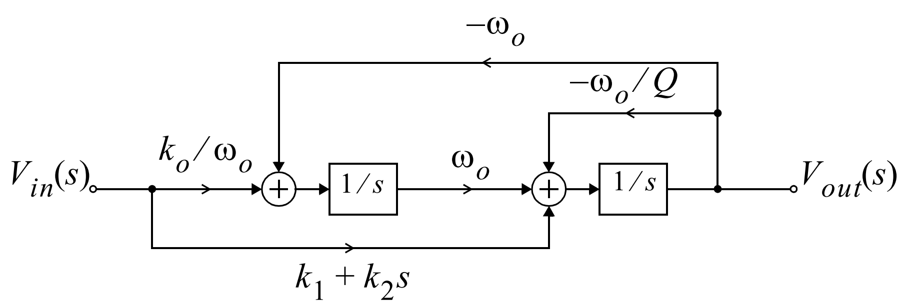
- We find

$$C_X = 2pF \times \frac{0.25}{1 - 0.25} = 0.667pF \quad (8)$$

$$G_{m1} = 2\pi \times 10^7 \times 2.667pF = 0.168 \; mA/V \quad (9)$$

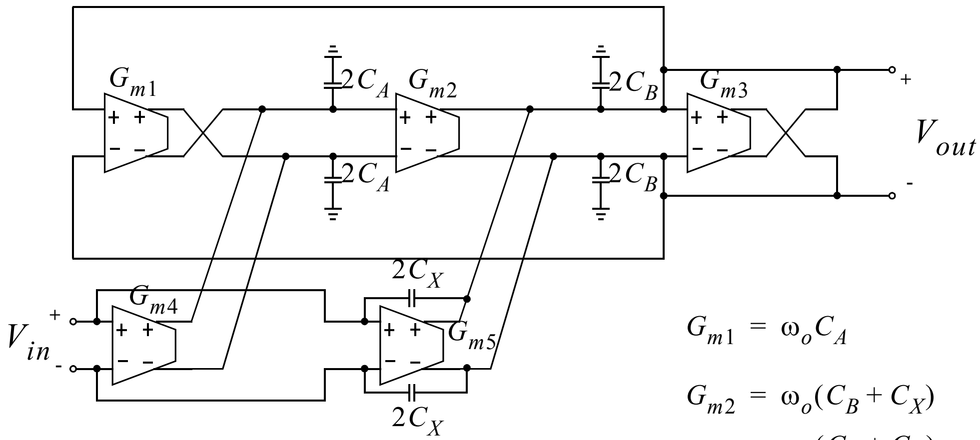
$$G_{m2} = 4\pi \times 10^7 \times 2.667pF = 0.335 \; mA/V \quad (10)$$

Second-Order Filter



$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{k_2 s^2 + k_1 s + k_o}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} \quad (11)$$

Second-Order Filter



$$C_X = C_B\left(\frac{k_2}{1-k_2}\right) \text{ where } (0 \le k_2 < 1)$$

$$G_{m1} = \omega_o C_A$$

$$G_{m2} = \omega_o (C_B + C_X)$$

$$G_{m3} = \frac{\omega_o (C_B + C_X)}{Q}$$

$$G_{m4} = (k_o C_A)/\omega_o$$

$$G_{m5} = k_1 (C_B + C_X)$$

Second-Order Filter

$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{s^2\left(\frac{C_X}{C_X + C_B}\right) + s\left(\frac{G_{m5}}{C_X + C_B}\right) + \left(\frac{G_{m2}G_{m4}}{C_A(C_X + C_B)}\right)}{s^2 + s\left(\frac{G_{m3}}{C_X + C_b}\right) + \left(\frac{G_{m1}G_{m2}}{C_A(C_X + C_B)}\right)} \quad (12)$$

- Note that there is a restriction on the high-frequency gain coeff k_2 as in the first-order case.
- Note that G_{m3} sets the damping of this biquad
- G_{m1} and G_{m2} form two integrators with unity-gain frequencies of ω_0 / s.

Example

- Find values for a bandpass filter with a center frequency of $20MHz$, a Q value of 5, and a center frequency gain of 1.
- Assume $C_A = C_B = 2pF$

$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{Gs\frac{\omega_o}{Q}}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{13}$$

where $G = 1$ is the gain at the center frequency.

Example

- Since, $\omega_o = 2\pi \times 20MHz$ and $Q = 5$, we find

$$k_1 = G\frac{\omega_o}{Q} = 2.513\times10^7 \text{rad/s} \tag{14}$$

- Since k_0 and k_2 are zero, we have $C_x = G_{m4} = 0$
- The transconductance values are:

$$G_{m1} = \omega_o C_A = 0.2513 \text{ mA/V} \tag{15}$$

$$G_{m2} = \omega_o(C_B + C_X) = 0.2513\ mA/V \tag{16}$$

$$G_{m3} = G_{m5} = k_1 C_B = 50.27\mu\text{A/V} \tag{17}$$

Bipolar Transconductors

- 2 main methods

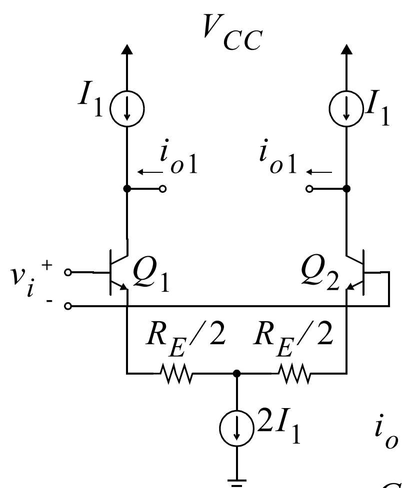
Fixed Transconductor with Gain Cell

- Larger input range, lower transconductance
- Create a transconductor with a fixed G_m value using a resistor
- Tune the transconductance using a gain cell

Multiple Differential Pairs

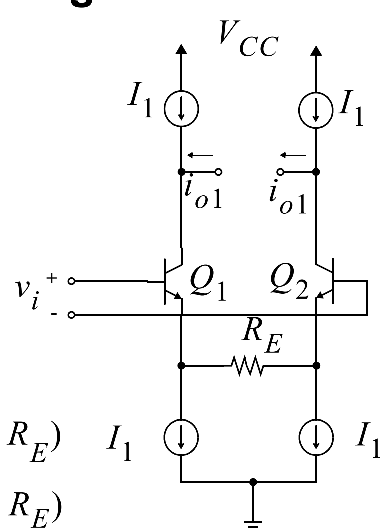
- Smaller input range, higher transconductance
- Use 2 diff pairs to extend linear input range
- Tuning done by adjusting bias current

Fixed Transconductors using Resistors



$$i_{o1} = v_i/(2r_e + R_E)$$

$$G_m = 1/(2r_e + R_E)$$



- Left circuit needs higher common-mode voltage

Max Differential Input Range

- Determine when one of diff transistors turns off
- For example, find when Q_2 turns off in right circuit
- If Q_2 off, then all of I_1 flows through R_E resulting in

$$V_{i,max} = I_1 R_E \tag{18}$$

- However, there is significant distortion at this point since V_{be} is not constant
- Maximum input range might be half that resulting in

$$V_{i,max} = (I_1/2)R_E \tag{19}$$

Distortion

- So far, have assumed V_{be} voltages remain constant which is reasonable if $r_e \ll R_E$

$$r_e \equiv \frac{V_T}{I_E} \tag{20}$$

implying

$$r_{e,max} = \frac{V_T}{I_{E,min}} \ll R_E \tag{21}$$

or equivalently,

$$I_{E,min} \gg \frac{V_T}{R_E} \tag{22}$$

Distortion

Example

- If $R_E = 20k\Omega$ and $V_T = 25mV$, then $I_{E, min} \approx 1.25\ \mu A$

How much is "much greater than"?

- Depends on how much distortion can be tolerated
- If $r_{e, \max} = 0.1R_E$ when $V_{i, \max} = (I_1/2)R_E$, the actual output current is 3% from ideal linear response.
- Results in about a 1% THD (3 times better than peak linearity error)
- Can use smaller input signals but then noise might dominate

Transconductance

- Use small-signal T-model for bipolar transistors

$$i_{o1} = \frac{v_i}{r_{e1} + R_E + r_{e2}} = \frac{v_i}{2r_e + R_E} \tag{23}$$

where r_e is small-signal emitter resist ($r_e = \alpha/g_m$)

$$r_e = \frac{V_T}{I_E} = \frac{V_T}{I_1} \tag{24}$$

- Leading to

$$G_m = \frac{i_{o1}}{v_i} = \frac{1}{2r_e + R_E} \tag{25}$$

Example

- Given $R_E = 3k\Omega$ (i.e. $G_m \approx 0.333\ mA/V$), $V_{i,\max} = \pm 500mV$, find I_1 so $r_{\mathrm{e,max}} < 0.1R_E$

- We have $r_{\mathrm{e,max}} < 0.1R_E = 300\Omega$ which occurs when

$$I_{\mathrm{E2,min}} = \frac{V_T}{r_{\mathrm{e,max}}} = \frac{26mV}{300\Omega} = 86.7\mu A \tag{26}$$

- For this same input voltage of 500 mV

$$I_{RE} \approx \frac{500mV}{3k\Omega} = 167\mu A \tag{27}$$

Example

- Since $I_1 = I_{RE} + I_{E2}$

$$I_1 = 167 + 86.7 = 253\mu A \tag{28}$$

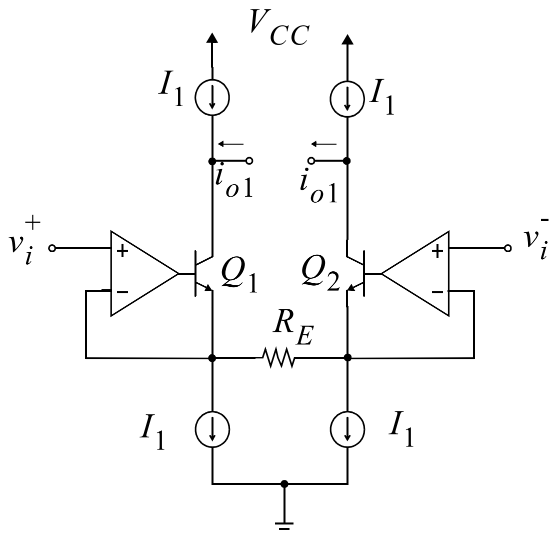
- Thus, a minimum bias current of $253\mu A$ should be chosen resulting in a nominal r_e and G_m given by

$$r_e = \frac{V_T}{I_1} = 103\Omega \tag{29}$$

$$G_m = \frac{1}{(2r_e + R_E)} = 0.312\ mA/V \tag{30}$$

- A 4 times increase in I_1 would improve distortion by about 10 times but use more power.

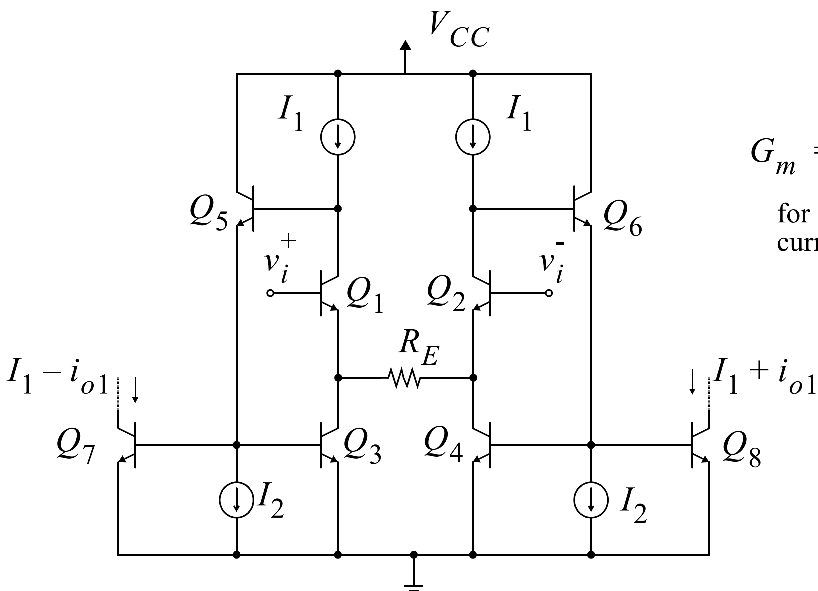
Linear Transconductor — Opamps



$$G_m = 1/R_E$$

- Feedback keeps input voltage across R_E
- Simple opamps used (typically single stage)

Linear Transconductor — Constant Current



$$G_m = 1/R_E$$

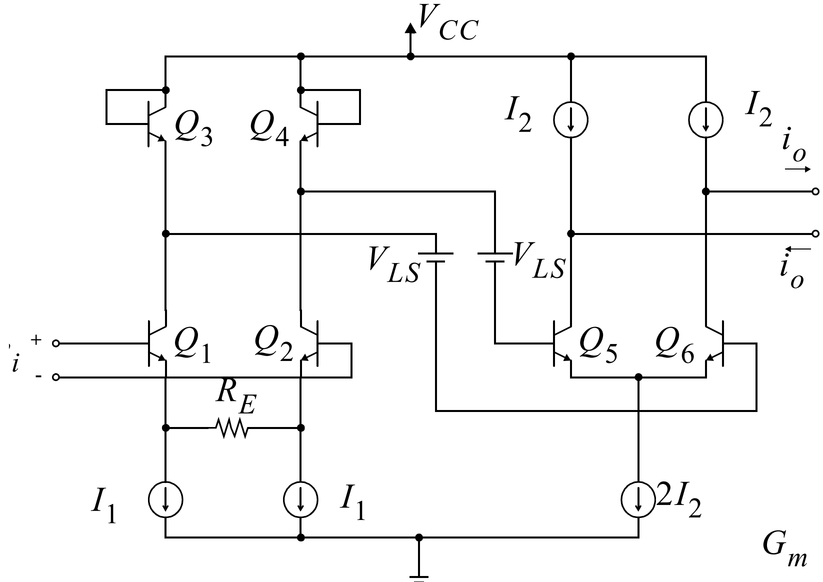
for equal sized current mirrors

- Fix collector currents through diff pair using feedback

Gain-Cell Transconductor

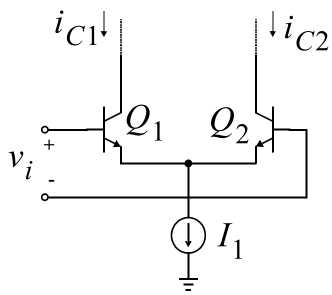
- Use a gain-cell to adjust output current
- Output current of gain-cell is a scaled version of input current determined by ratio of two currents
- Gain-cell is a translinear circuit and is closely related to translinear multiplier (also known as a Gilbert multiplier)
- Gain-cell is highly linear
- Often requires the use of voltage level-shifters

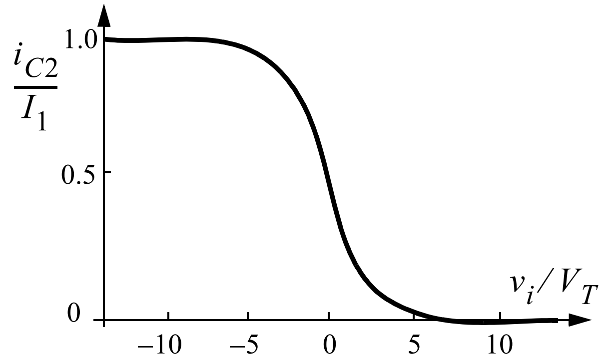
Gain-Cell Transconductor



$$G_m = \left(\frac{1}{R_E}\right)\left(\frac{I_2}{I_1}\right)$$

Differential Pair





$$i_{C2} = \frac{I_1}{1 + e^{v_i/V_T}} \tag{31}$$

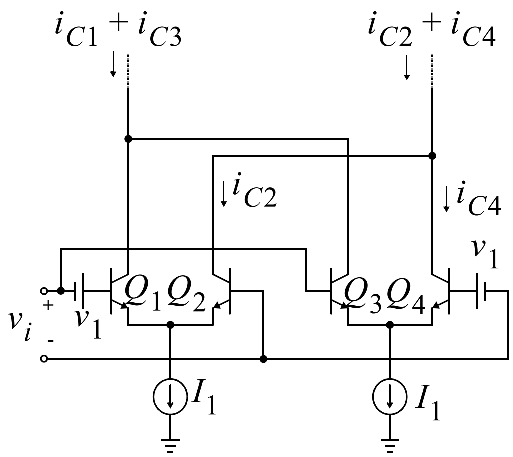
- Relatively linear near $v_i = 0$

$$G_m = \frac{1}{2r_e} = \frac{I_1}{4V_T} \tag{32}$$

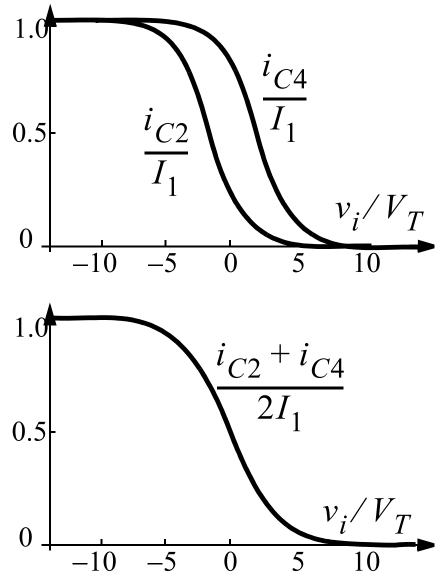
Differential Pair

- G_m proportional to I_1
- However, limited input range — when $v_i > 32\mathrm{mVpp}$, $\mathrm{THD}{>}1\%$.
- Use multiple diff pairs to increase linear input range
- Conceptual — use 2 diff pairs with dc offset
- Actual — replace dc offsets by resizing transistors in differential pairs
- Increases input range to $v_i > 96\mathrm{mVpp}$ for 1% THD

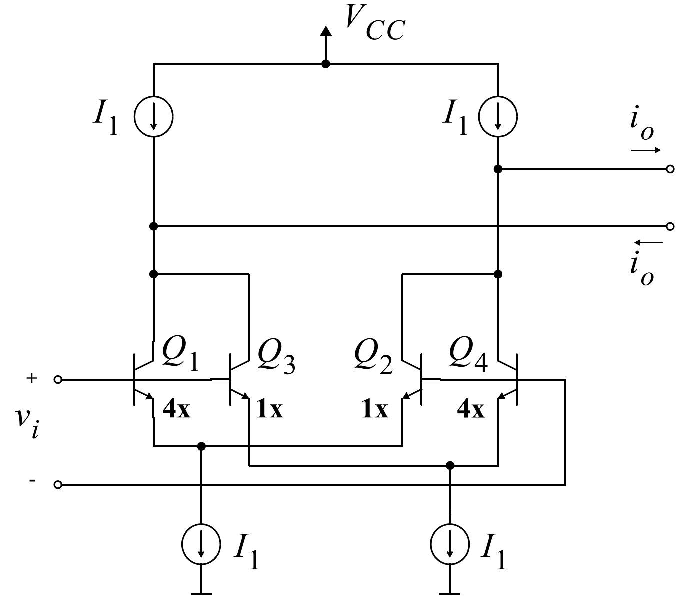
Multiple Diff-Pairs



Choose $v_1 = 1.317 V_T$



Multiple Diff-Pairs



$$G_m = \frac{8I_1}{25V_T}$$

Multiple Diff-Pair

- When $v_i = 0$, I through Q_1 and Q_2 are $0.8I_1$ and $0.2I_1$.

$$G_m = \frac{1}{r_{e1} + r_{e2}} + \frac{1}{r_{e3} + r_{e4}} \tag{33}$$

$$r_{e1} = r_{e4} = \frac{V_T}{0.8I_1} \tag{34}$$

$$r_{e2} = r_{e3} = \frac{V_T}{0.2I_1} \tag{35}$$

$$G_m = \frac{8I_1}{25V_T} \tag{36}$$

- which is 28% larger than diff pair but uses twice the current — same current results in 36% less G_m

CMOS Transconductors

- A large variety of methods
- Best approach depends on application
- 2 main classifications — triode or active transistor based

Triode vs. Active

- Triode based tends to have better linearity
- Active tend to have faster speed for the same operating current

Triode Transconductors

- Recall n-channel triode equation

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left((V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}\right) \qquad (37)$$

where to remain in triode

$$V_{DS} < V_{eff} \quad \text{where} \quad V_{eff} = V_{GS} - V_{tn} \qquad (38)$$

or equivalently, $V_{GS} > V_{DS} + V_{tn}$

- Above models are only reasonably accurate (
- Not nearly as accurate as exponential model in BJTs
- Use fully-differential architectures to reduce even-order distortion terms — also improves common-mode noise rejection

Fixed-Bias Triode Transconductor

- Use a small V_{DS} voltage so V_{DS}^2 term goes to zero

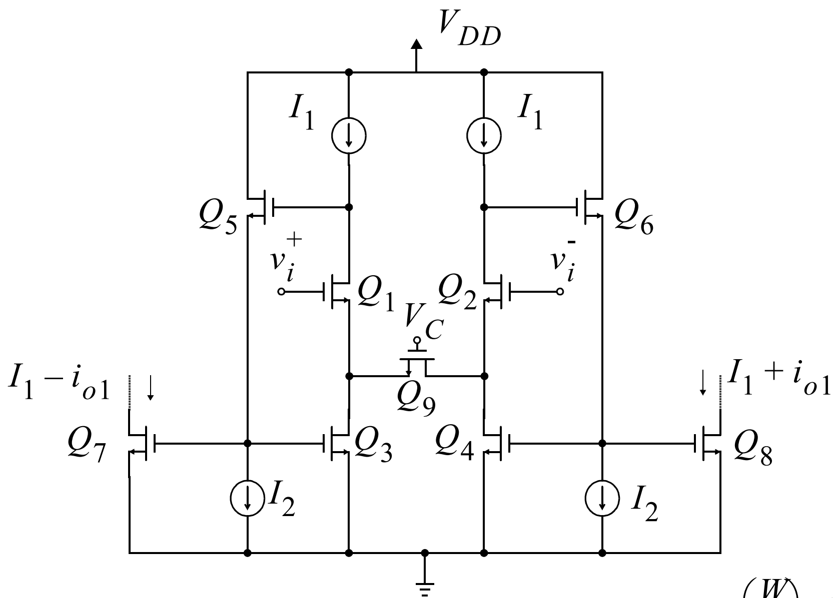
$$r_{DS} \equiv \left.\left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\right|_{v_{DS} = 0} \qquad (39)$$

which results in

$$r_{DS} = \left(\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{tn})\right)^{-1} \qquad (40)$$

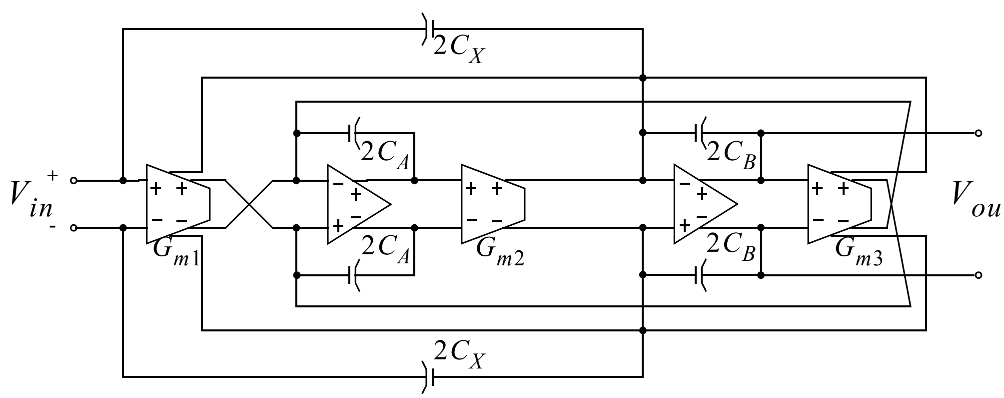
- Can use a triode transistor where a resistor would normally be used — resistance value is tunable

Fixed-Bias Triode Transconductor



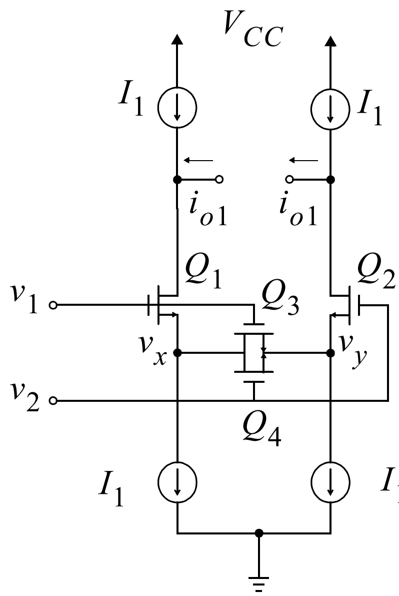
$$G_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_9 (v_{gs9} - V_{tn})$$

Biquad using Multiple Outputs



- Can make use of multiple outputs to build a biquad filter — scale extra outputs to desired ratio
- Reduces the number of transconductors — saves power and die area
- Above makes use of Miller integrators

Varying-Bias Triode Transconductor



$$G_m = \frac{4k_1k_3\sqrt{I_1}}{(k_1+4k_3)\sqrt{k_1}}$$

Varying-Bias Transconductor

- gates of Q_3, Q_4 connected to the differential input
- Q_3 and Q_4 undergo varying bias conditions to improve linearity
- Can show

$$G_m = \frac{4k_1k_3\sqrt{I_1}}{(k_1+4k_3)\sqrt{k_1}} \tag{41}$$

where

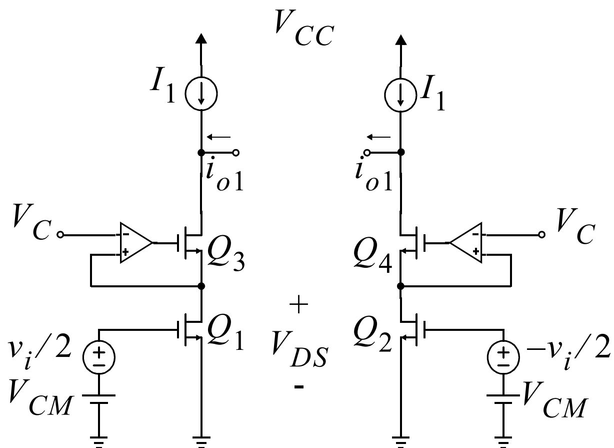
$$k_i = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_i \tag{42}$$

- Note, G_m proportional to square-root of I_1 as opposed to linear relation for a BJT transconductor.

Drain-Source Fixed-Bias Transconductor

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left((V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}\right) \qquad (43)$$

- If V_{DS} kept constant, then i_D linear wrt V_{GS}



$$G_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_1 V_{DS}$$

Drain-Source Fixed-Bias Transconductor

- Can realize around 50 dB linearity (not much better since model is not that accurate)
- Requires a fully-differential structure to cancel even-order terms
- V_C sets V_{DS} voltage — rather than opamp with feedback can use BJTs in a BiCMOS technology
- Requires a non-zero common-mode voltage on input
- Transconductance given by

$$G_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_1 V_{DS} \qquad (44)$$

- Note that G_m roughly proportional to bias current since current roughly proportional to V_{DS}

Example

- $\mu_n C_{ox} = 96\ \mu A/V^2$, $(W/L)_1 = (W/L)_2 = 10$, $V_{tn} = 0.8V$, and $V_{CM} = 2V$

— $V_C = 0.2V$ **Case**

$$G_m = 96\ \mu A/V^2 \times 10 \times 0.2V = 0.192\ mA/V \tag{45}$$

$$I_1 = 96\ \mu A/V^2 \times 10\left((2-0.8)0.2 - \frac{0.2^2}{2}\right) = 0.211\ mA \tag{46}$$

- Max v_i — $V_{\text{eff1}} > V_{DS} = 0.2\text{ V}$ or $V_{G1} > V_{DS} + V_{tn} = 1.0\text{ V}$. Since $V_{CM} = 2\text{ V}$, max $v_i = 2\text{ V}$.

— $V_C = 0.4V$ **Case**

- $G_m = 0.384\ mA/V$, $I_1 = 0.384\ mA$ and max input signal swing is $v_i = 1.6\text{ V}$ (loss of signal swing)

Active-Based Transconductors

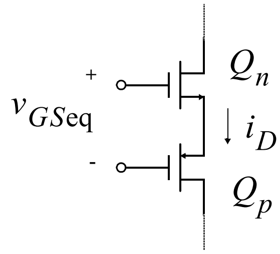
- Active transistors are those operating in the active region
- Active region also referred to as pinch-off or saturation region
- In active region

$$I_D = K_i(V_{GS} - V_{tn})^2 \tag{47}$$

when $V_{DS} \geq V_{GS} - V_{tn} = V_{eff}$ and $V_{GS} \geq V_{tn}$

- Here, $K_i \equiv (\mu_n C_{ox}/2)(W/L)_i$

CMOS Pair



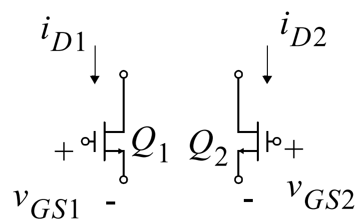
$$i_D = K_{eq}(v_{GSeq} - V_{teq})^2$$

$$K_{eq} = \frac{K_n K_p}{(\sqrt{K_n} + \sqrt{K_p})^2} \qquad V_{teq} = V_{tn} - V_{tp}$$

$$(\text{where } V_{tn} > 0 \text{ and } V_{tp} < 0)$$

- Above circuit acts as a single transistor with threshold V_{teq} and parameter K_{eq}

Constant Sum of Gate-Source Voltages



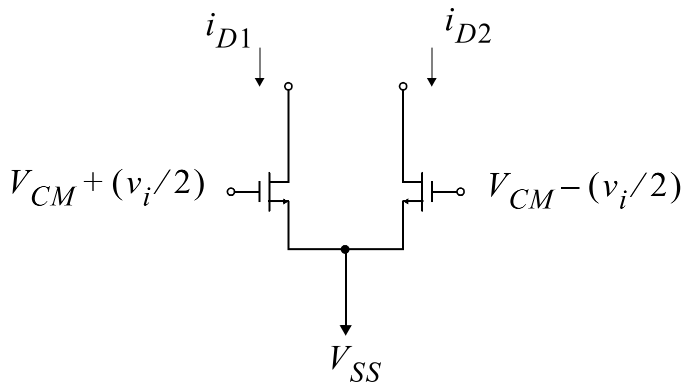
(matched devices)

$$(i_{D1} - i_{D2}) = K(v_{GS1} + v_{GS2} - 2V_{tn})(v_{GS1} - v_{GS2}) \qquad (48)$$

$$K = (\mu_n/2)C_{ox}\left(\frac{W}{L}\right) \qquad (49)$$

- If $V_{GS1} + V_{GS2} = \text{constant}$ then linear transconductor
- Note — Differential output current linear but single-ended currents have large second-order distortion.

Source-Connected Differential Pair



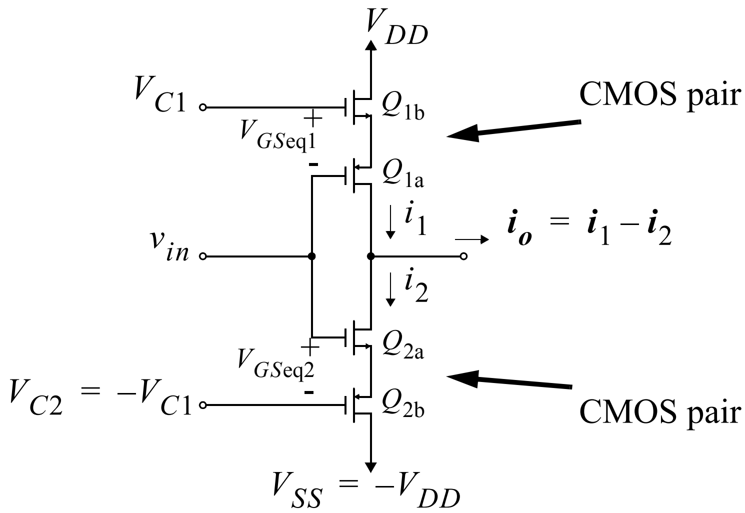
$$(i_{D1}-i_{D2}) = 2K(V_{CM}-V_{SS}-V_{tn})(v_i)$$

$$G_m = 2K(V_{CM}-V_{SS}-V_{tn})$$

Source-Connected Differential Pair

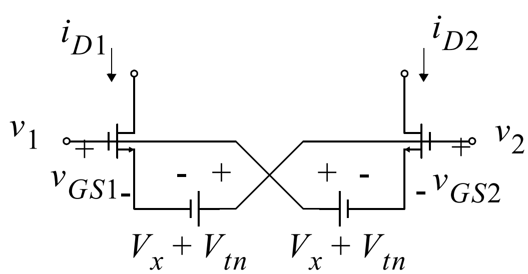
- Input signal varies symmetrically around a common-mode voltage
- Linearity limited due to square-law model being inaccurate
- In addition, even-order harmonics occur if the difference between two drain currents not exact.
- Limited to less than 50 dB linearity
- Adjust G_m by varying V_{CM}
- In a short channel process, velocity saturation limits transconductance variation

Inverter-Based



$$G_m = 4K_{\mathrm{eq}}(V_{C1} - V_{t\mathrm{eq}})$$

Diff-Pair with Floating Voltage Sources



$$(i_{D1} - i_{D2}) = 4KV_x(v_1 - v_2)$$

$$G_m = 4KV_x$$

- Writing a voltage equation around the loop

$$v_{GS1} - (V_x + V_{tn}) + v_{GS2} - (V_x + V_{tn}) = 0 \tag{50}$$

implying

$$v_{GS1} + v_{GS2} = 2(V_x + V_{tn}) \tag{51}$$

- Thus, a constant sum of gate-source voltages occurs — even if input signal is not balanced

Diff-Pair with Floating Voltage Sources

$$v_1 - v_{GS1} + V_x + V_{tn} = v_2 \tag{52}$$

$$v_2 - v_{GS2} + V_x + V_{tn} = v_1 \tag{53}$$

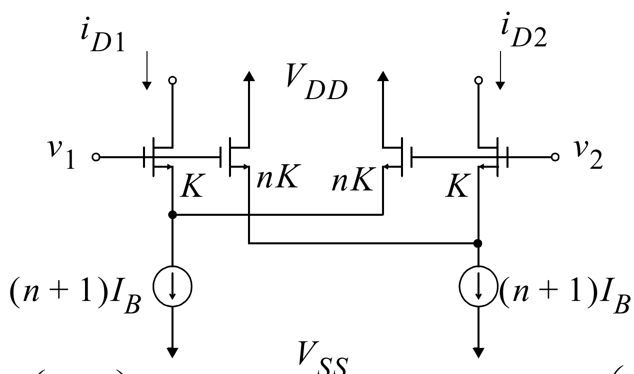
- Subtracting (52) from (53), we obtain

$$v_{GS1} - v_{GS2} = 2(v_1 - v_2) \tag{54}$$

- Finally, output diff current found from (48)

$$(i_{D1} - i_{D2}) = 4KV_x(v_1 - v_2) \tag{55}$$

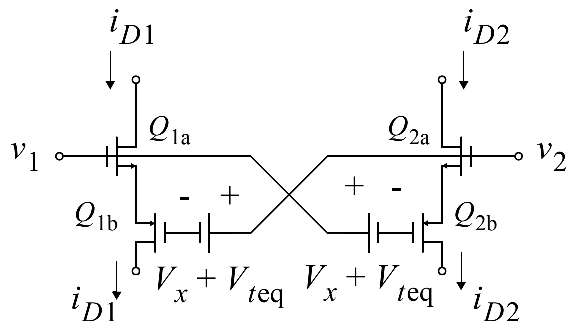
Approach #1



$$(i_{D1} - i_{D2}) = \left(\frac{n}{n+1}\right)4\sqrt{KI_B}(v_1 - v_2) \qquad G_m = \left(\frac{n}{n+1}\right)4\sqrt{KI_B}$$

- Floating voltage sources built using large transistors (n times larger with n typically greater than 5)
- Disadvantage — large bias current and moderate linearity

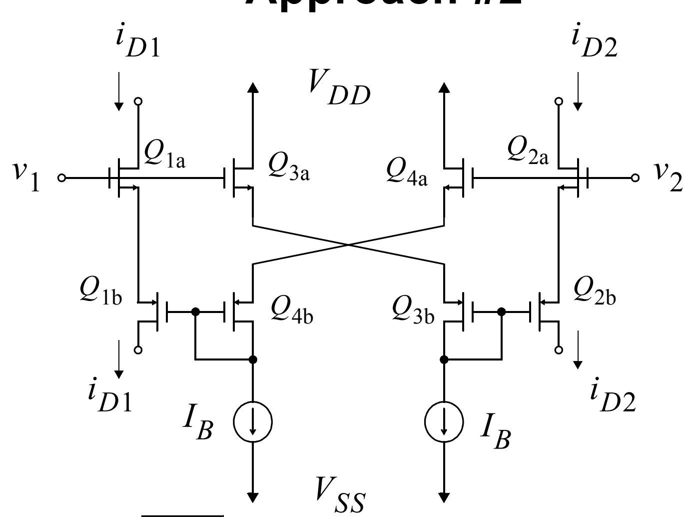
Approach #2



$$(i_{D1} - i_{D2}) = 4K_{eq}V_x(v_1 - v_2)$$

- Replace diff-pair transistors with CMOS pairs
- Now replace floating voltage sources with CMOS pairs

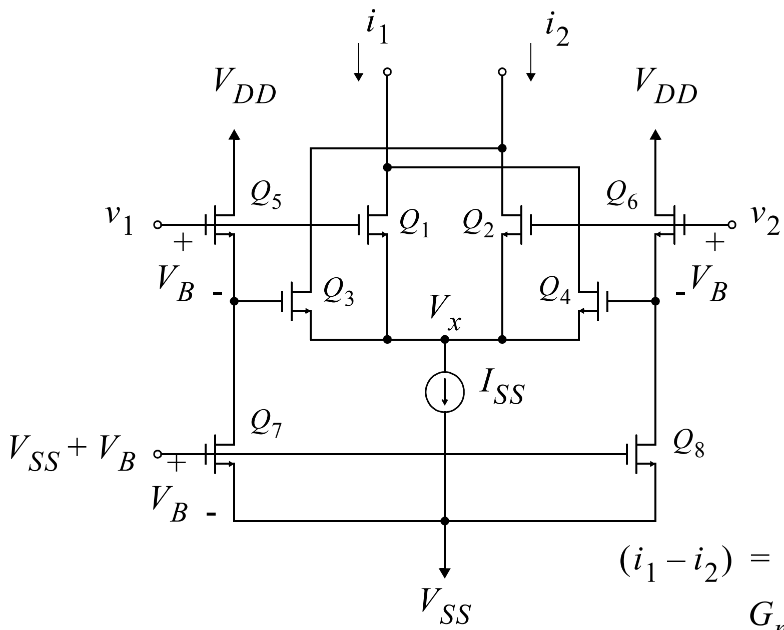
Approach #2



$$(i_{D1} - i_{D2}) = 4\sqrt{K_{eq}I_B}(v_1 - v_2) \qquad G_m = 4\sqrt{K_{eq}I_B}$$

- G_m proportional to $\sqrt{I_B}$
- Requires a large power supply

Bias-Offset Cross-Coupled Diff-Pairs



$$(i_1 - i_2) = 2KV_B(v_1 - v_2)$$
$$G_m = 2KV_B$$

Bias-Offset Cross-Coupled Diff-Pairs

$$i_1 = K(v_1 - V_x - V_{tn})^2 + K(v_2 - V_B - V_x - V_{tn})^2 \quad (56)$$

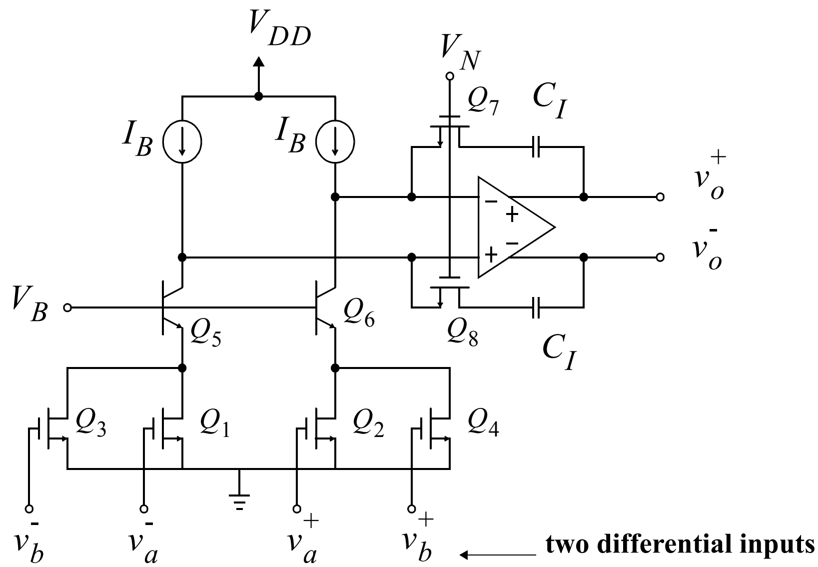
$$i_2 = K(v_2 - V_x - V_{tn})^2 + K(v_1 - V_B - V_x - V_{tn})^2 \quad (57)$$

$$(i_1 - i_2) = 2KV_B(v_1 - v_2) \quad (58)$$

- The output diff current is linear wrt diff input voltage
- G_m proportion to V_B which is proportional to $\sqrt{I_B}$
- Bias current, I_{SS}, does not affect G_m but does set maximum (or minimum) output current available

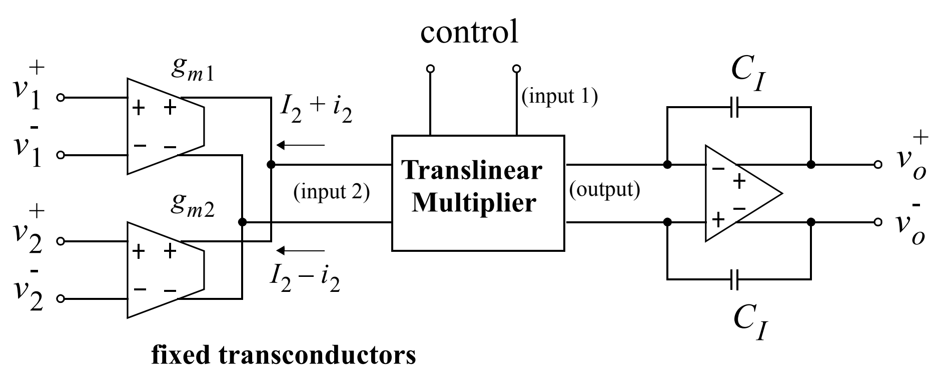
BiCMOS Transconductors

Tunable MOS in Triode



BiCMOS Transconductors

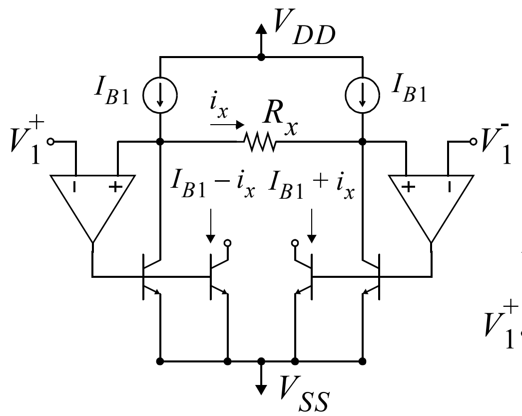
Fixed-Transconductor with Translinear Multiplier



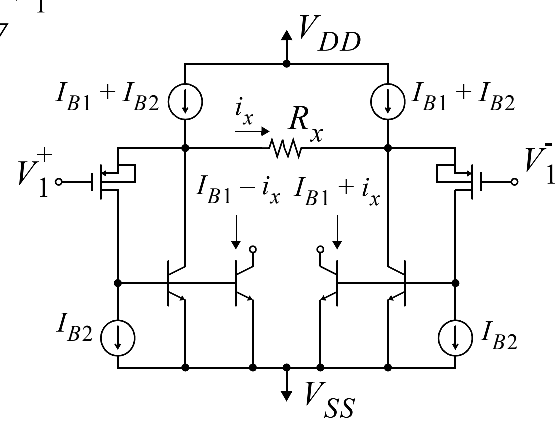
- Translinear multiplier used to tune transconductance
- Miller integrator used to maintain high linearity

BiCMOS Transconductors

Circuit GM Implementation



conceptual

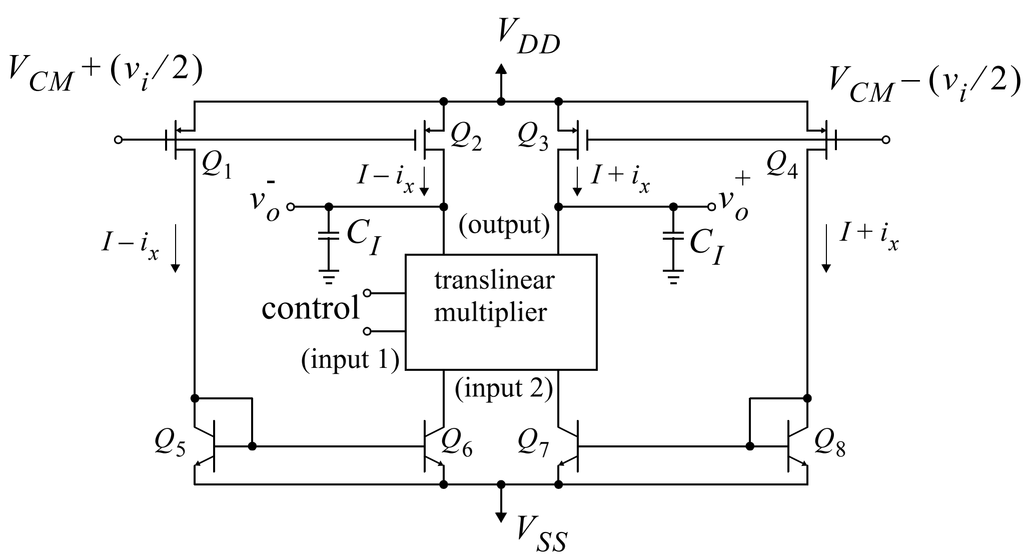


circuit

$(I_{B2} - i_x)$ and $(I_{B2} + i_x)$
go to the translinear multiplier

BiCMOS Transconductors

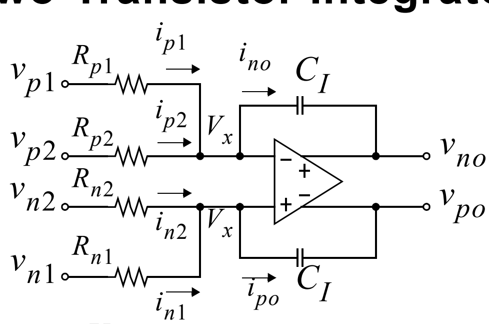
Fixed MOS Gm with a Translinear Multiplier

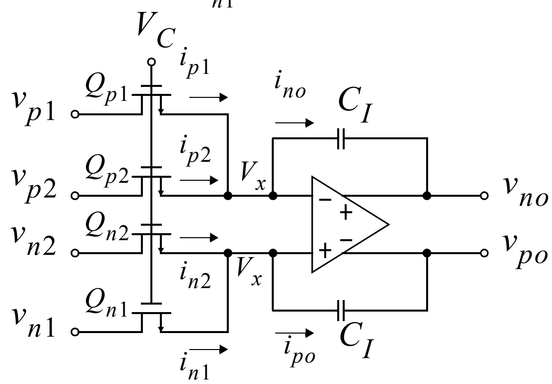


MOSFET-C Filters

- Gm-C filters are most common but MOSFET-C show promise in BiCMOS where power is important
- MOSFET-C filters similar to active-RC filters but resistors replaced with MOS transistors in triode
- Generally slower than Gm-C filters since opamps capable of driving resistive loads required
- Also rely on Miller integrators
- 2 main types — 2 transistor and 4 transistor

Two-Transistor Integrators





Two-Transistor Integrators

- For resistor integrator

$$v_{\text{diff}} = \frac{1}{sR_1C_I}(v_{p1} - v_{n1}) + \frac{1}{sR_2C_I}(v_{p2} - v_{n2}) \qquad (59)$$

- Negative integration — cross-couple wires
- For MOSFET-C integrator

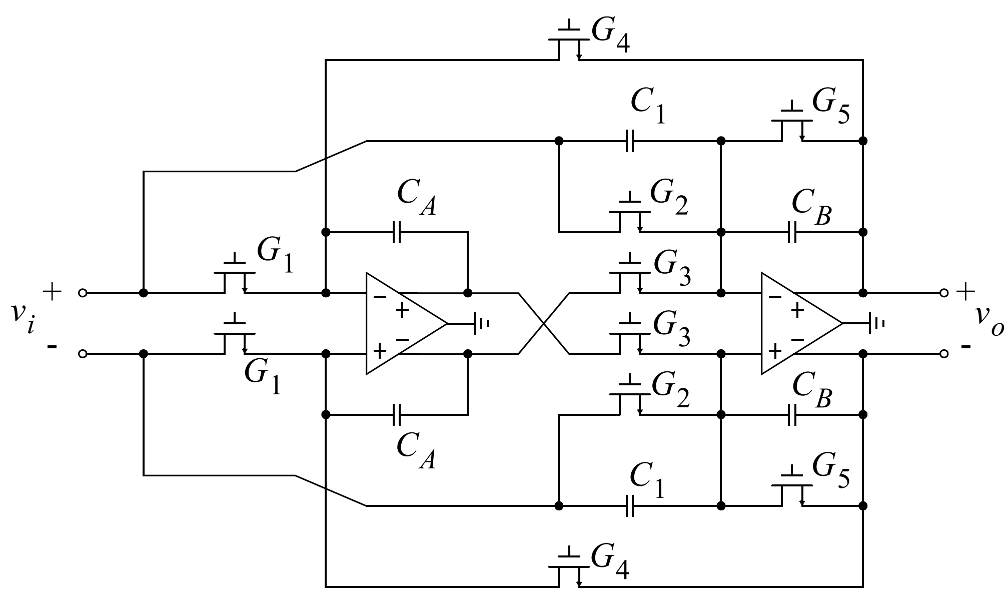
$$r_{DS} = \left(\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_{tn})\right)^{-1} \qquad (60)$$

leading to

$$v_{\text{diff}} = \frac{1}{sr_{DS1}C_I}(v_{p1} - v_{n1}) + \frac{1}{sr_{DS2}C_I}(v_{p2} - v_{n2}) \qquad (61)$$

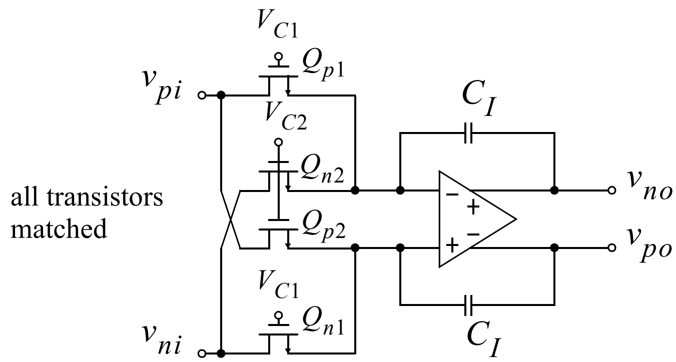
$$r_{DSi} = \left(\mu_n C_{ox}\left(\frac{W}{L}\right)_i(V_C - V_x - V_{tn})\right)^{-1} \qquad (62)$$

MOSFET-C Biquad Filter



Four-Transistor Integrator

- Can improve linearity of MOSFET-C integrators by using 4 transistors rather than 2



- Analyzed by treating it as a two-input integrator with inputs $(v_{pi} - v_{ni})$ and $(v_{ni} - v_{pi})$.

Four-Transistor Integrator

- If all four transistor matched,

$$v_{\text{diff}} = v_{po} - v_{no} = \frac{1}{sr_{DS}C_I}(v_{pi} - v_{ni}) \tag{63}$$

$$r_{DS} = \left(\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{C1} - V_{C2})\right)^{-1} \tag{64}$$

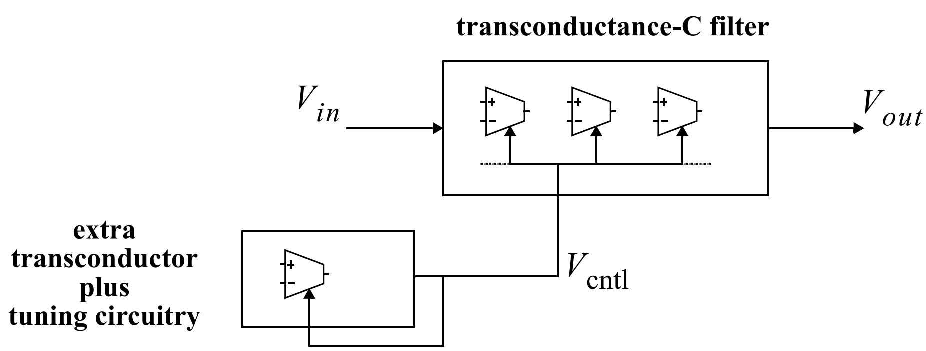
Distortion

- Model for drain-source current shows non-linear terms not dependent on controlling gate-voltage
- All even and odd distortion products will cancel
- Model only valid for older long-channel length technologies
- In practice, about a 10 dB linearity improvement

Tuning Circuitry

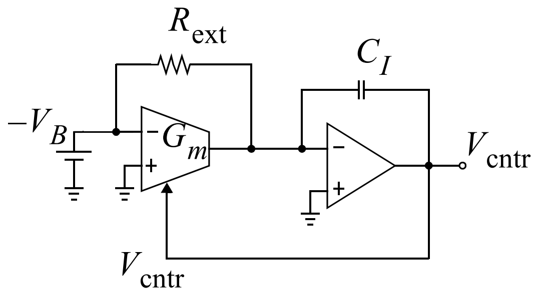
- Tuning can often be the MOST difficult part of a continuous-time integrated filter design
- Tuning required for cont-time integrated filters to account for capacitance and transconductance variations — 30 percent time-constant variations
- Must account for process, temperature, aging, etc.
- While absolute tolerances high, ratio of two like components can be matched to under 1 percent
- Note that SC filters do not need tuning as their transfer-function accuracy set by ratio of capacitors and a clock-frequency

Indirect Tuning

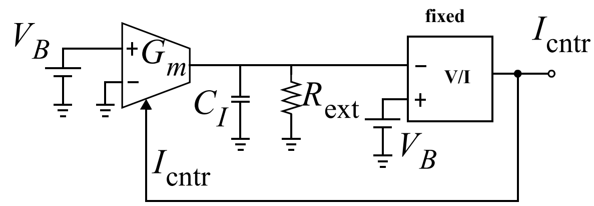


- Most common method — build an extra transconductor and tune it
- Same control signal is sent to filter's transconductors which are scaled versions of tuned extra
- Indirect since actual filter's output not measured

Constant Transconductance

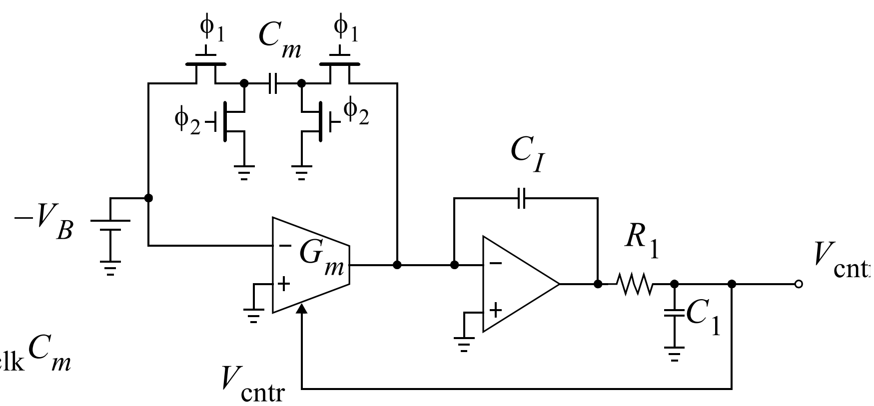


$$G_m = \frac{1}{R_{ext}}$$



- Can tune Gm to off-chip resistance and rely on capacitor absolute tolerance to be around 10 percent

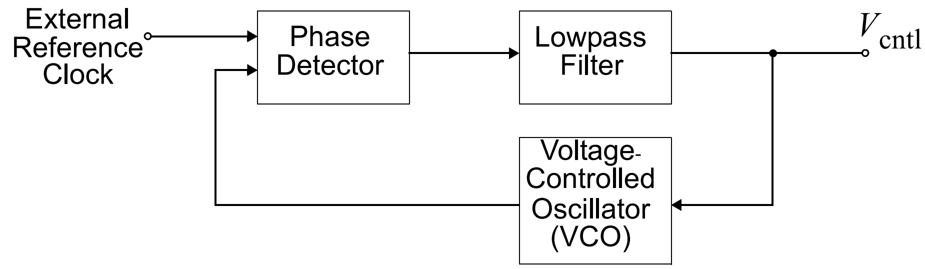
Frequency Tuning



$$G_m = f_{clk} C_m$$

- A precise G_m / C ratio set — time period needed
- External resistance replaced by SC equivalent

Frequency Tuning



- Use a PLL to tune 2 integrators which realize a VCO
- Once VCO set to external freq, then G_m/C of VCO is set to correct value
- Choice of external clock freq is difficult.
  — Leaks into filter if within passband
  — Poor matching if too far from passband

Q-Factor Tuning

- Most industrial applications do not presently use Q-tuning and rely on matching
- For very high-performance circuits, may have to also tune Q-factor as well as G_m/C ratio
- Can use a magnitude locked-loop
- Can use adaptive filtering techniques where filter output is directly observed
- Example: look at step response for a square-wave type input (i.e. digital transmission signal)
  — slope determined by time-constant
  — peak determined by Q-factor

Dynamic Range Performance

- Linearity limits the value of the largest useful signals
- Noise limits the value of the smallest useful signals
- Linearity and noise together determine dynamic range of a filter
- Integrated continuous-time filters are often seriously impaired by their dynamic range performance

Measures

- Total Harmonic Distortion (THD)
- Third-order intercept point (IP3)
- Spurious-Free Dynamic Range (SFDR)

Total-Harmonic-Distortion (THD)

$$\mathrm{THD} = 10\log\left(\frac{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \ldots}{V_f^2}\right) \quad \text{in dB} \tag{65}$$

- V_f — amplitude of the fundamental
- V_{hi} — amplitude of the i'th harmonic component.

$$THD = \frac{\sqrt{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \ldots}}{V_f} \times 100 \quad \text{in \%} \tag{66}$$

- Typically, only power of first few harmonics used since distortion components usually fall off quickly

THD Limits

- THD will give be optimistic if harmonics fall in stopband
- However, if a lower fundamental frequency is used, then THD is optimistic as distortion often degrades with high input frequencies
- Would like to measure distortion with input signals near the upper passband edge.
- Need an intermodulation test!

Example

- A $21MHz$ lowpass filter is being tested
- A $5MHz$ input signal has harmonics at 10, 15 and 20 but then fall in the stopband
- Want to test the filter with a $20\mathrm{MHz}$ input

Third-Order Intercept Point (IP3)

- Here IP3 is described as third-order distortion often dominates in fully-diff circuits — can also define IP2
- Consider

$$v_o(t) = a_1 v_{in}(t) + a_2 v_{in}^2(t) + a_3 v_{in}^3(t) + a_4 v_{in}^4(t) + \dots \qquad (67)$$

- The linear term is a_1
- a_2, a_3, and a_4 determine second, third and fourth order distortion terms.
- In fully-differential circuits, all even terms small and typically a_3 dominates

$$v_o(t) \approx a_1 v_{in}(t) + a_3 v_{in}^3(t) \qquad (68)$$

Third-Order Intercept Point (IP3)

- If $v_{in}(t)$ is a sinusoidal

$$v_{in}(t) = A\cos(\omega t) \tag{69}$$

$$v_o(t) \approx a_1 A\cos(\omega t) + \frac{a_3}{4}A^3(3\cos(\omega t) + \cos(3\omega t)) \tag{70}$$

- Define H_{D1} and H_{D3} to be the amplitudes of the fundamental and third-harmonic terms

$$v_o(t) \equiv H_{D1}\cos(\omega t) + H_{D3}\cos(3\omega t) \tag{71}$$

- Since typically, $(3/4)a_3A^3 \ll a_1A$, then approximate

$$H_{D1} = a_1 A \tag{72}$$

Third-Order Intercept Point (IP3)

- Amplitude of third-order term is

$$H_{D3} = \frac{a_3}{4}A^3 \tag{73}$$

- Unfortunately, distortion term lies at $3\omega t$ for a single sinusoidal input and thus we resort to an intermodulation test
- Consider now

$$v_{in}(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t) \tag{74}$$

- Can show that

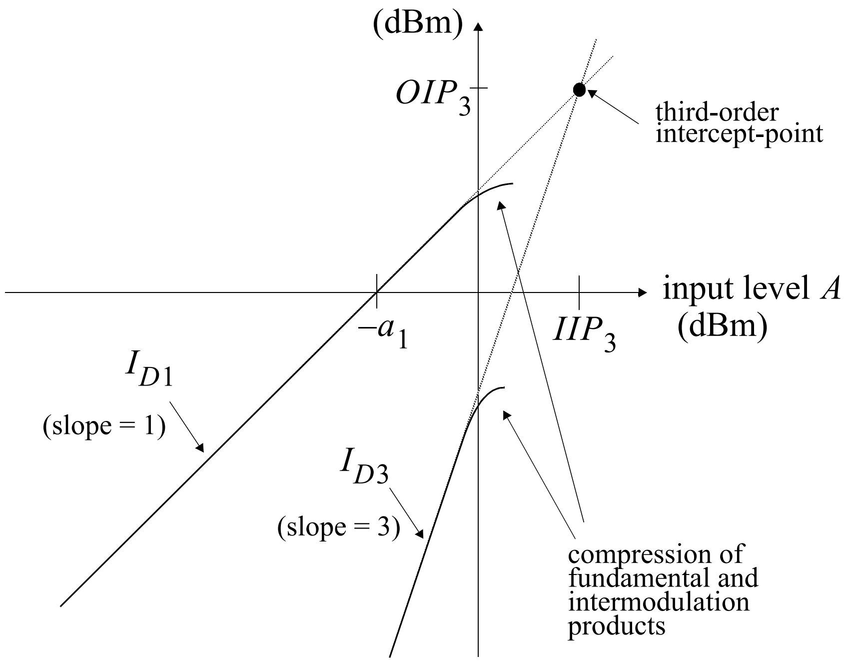
$$I_{D1} = a_1 A \tag{75}$$

$$I_{D3} = \frac{3a_3}{4}A^3 \tag{76}$$

Third-Order Intercept Point (IP3)

- The fundamental appears at ω_1 and ω_2
- The third-order term appears at $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$
- As A increased, fundamental rises linearly while third-order term rises as a cubic.
- Every 1dB increase in signal level increases the fundamental by 1dB but the intermod term by 3dB.
- **There is a 2dB worse intermod ratio for every 1dB increase in signal level.**
- Third-order intercept defined to be the point where third-order term will equal fundamental term
- Not physically possible (but an extrapolation) since other distortion terms will start to become important

Third-Order Intercept Point (IP3)



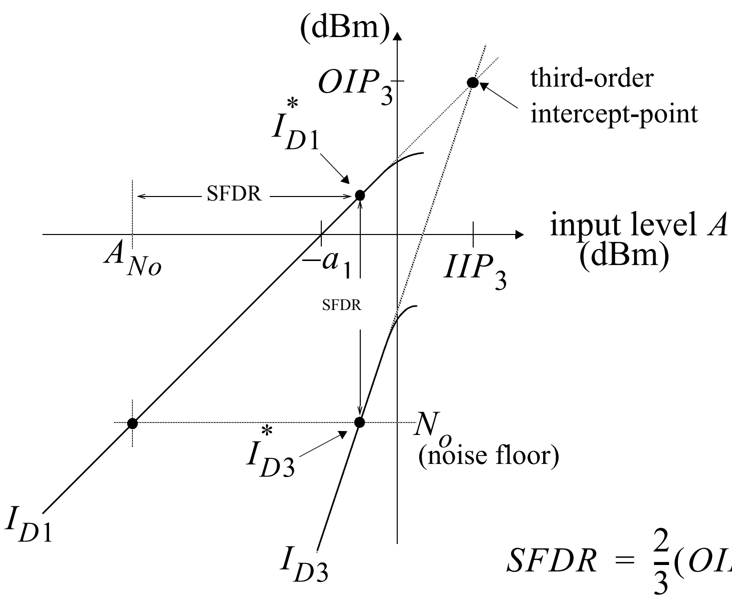
Third-Order Intercept Point (IP3)

- Knowing IP3 is useful to determine what signal level should be used for a certain intermodulation-ratio

Example

- If $OIP_3 = 20dBm$, what output signal level should be used such that the third-order intermodulation products are $60dB$ below the fundamental?
- Since we obtain a 2dB improvement for every dB drop in output signal level and we want a 60dB improvement from the intercept point, we need to lower the output by $60/2 = 30\text{dB}$
- The output level should be -10dBm

Spurious-Free Dynamic Range (SFDR)



$$SFDR = \frac{2}{3}(OIP3 - N_o)$$

SFDR

- Spurious-free dynamic range (SFDR) is the SNR when the power of the third-order intermodulation products equals the noise power.
- If the signal is larger, the distortion dominates
- If the signal is smaller, the noise dominates
- Actual dynamic range is 3dB lower since noise and distortion are equal

Example

- At an input signal level of 0dBm, an intermodulation ratio $-40dB$ was measured in an filter with a gain of 2dB.
- Since performance worsens by 2dB for each 1dB increase in signal level, the intermodulation ratio will be 0dB at an input level of 20dBm. Therefore, IIP3=20dBm and OIP3=22dBm
- If one desires an intermodulation ratio of $-45dB$ then the input should be lowered by 2.5dB or equivalently, it should be at a level of -2.5dBm
- If the noise power at the output is measured to be $-50dBm$, the expected SFDR is found by

$$SFDR = \frac{2}{3}(22+50) = 48dB \tag{77}$$

Example

- In other words, the intermod ratio should be $48\mathrm{dB}$ for the distortion power to equal the noise power.
- In intermod of $48\mathrm{dB}$ is obtained for an input signal value of $-4\mathrm{dBm}$ and an output signal value of $-2\mathrm{dBm}$
- A higher level implies that the distortion dominates while a lower signal level implies that the noise dominates.
- Signal-to-noise+distortion (SNDR) equals $45\mathrm{dB}$.