EXAMPLE DESIGN

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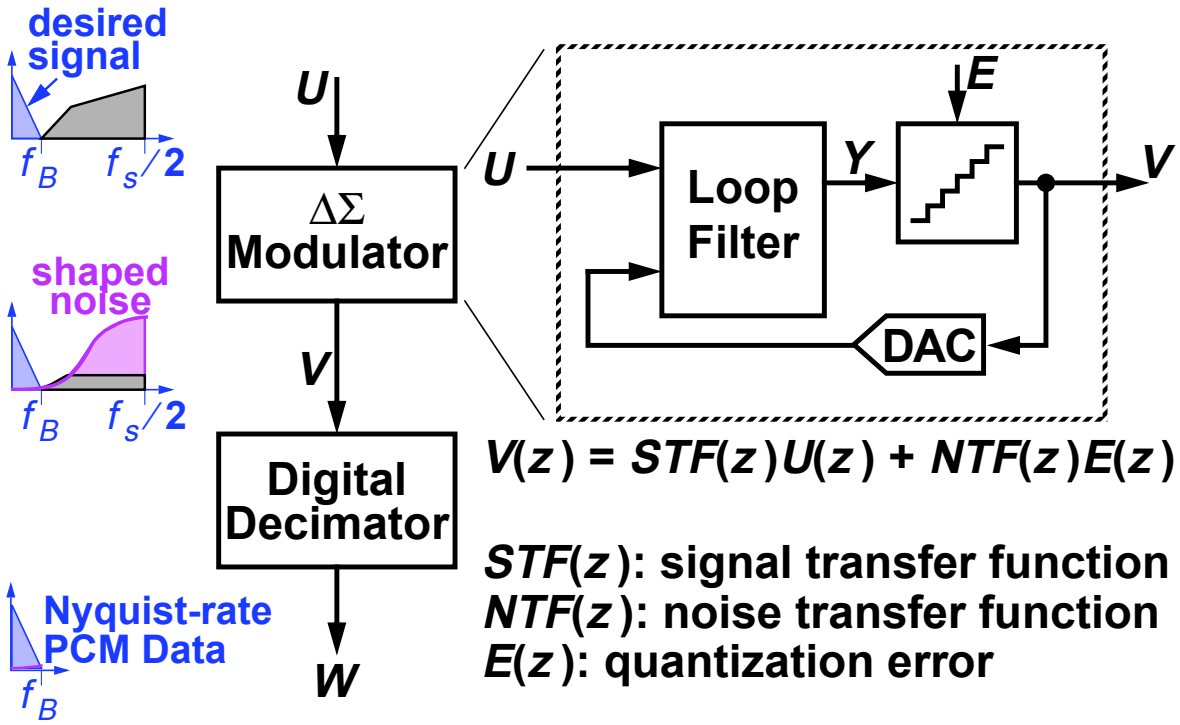
Highlights
(i.e. What you will learn today)

1. MOD2 implementation
2. Switched-capacitor integrator
   - Switched-C summer & DAC too
3. Dynamic-range scaling
4. kT/C noise
5. Verification strategy

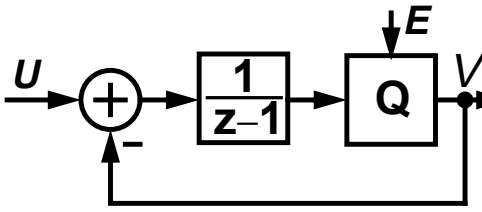
Review: A ΔΣ ADC System



$V(z) = STF(z)U(z) + NTF(z)E(z)$

$STF(z)$: signal transfer function
$NTF(z)$: noise transfer function
$E(z)$: quantization error

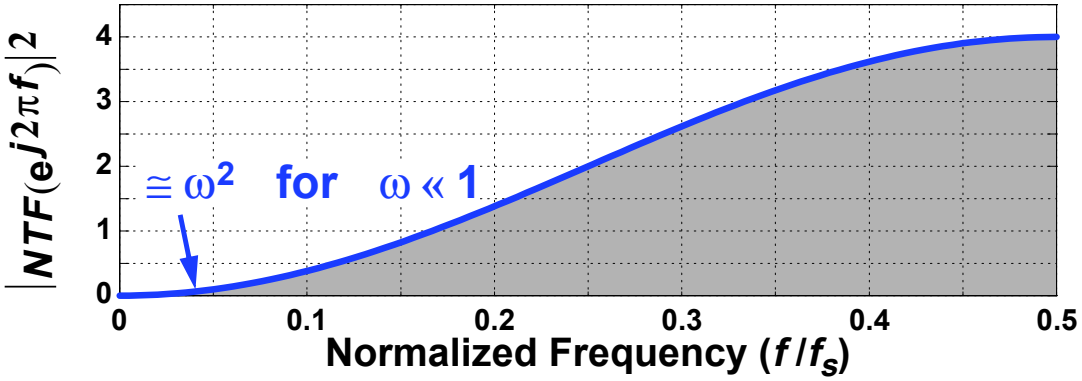
Review: MOD1



$$V(z) = NTF(z)E(z) + STF(z)U(z)$$

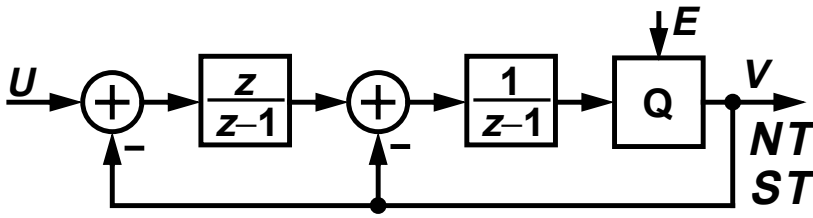
$$NTF(z) = (1 - z^{-1})$$

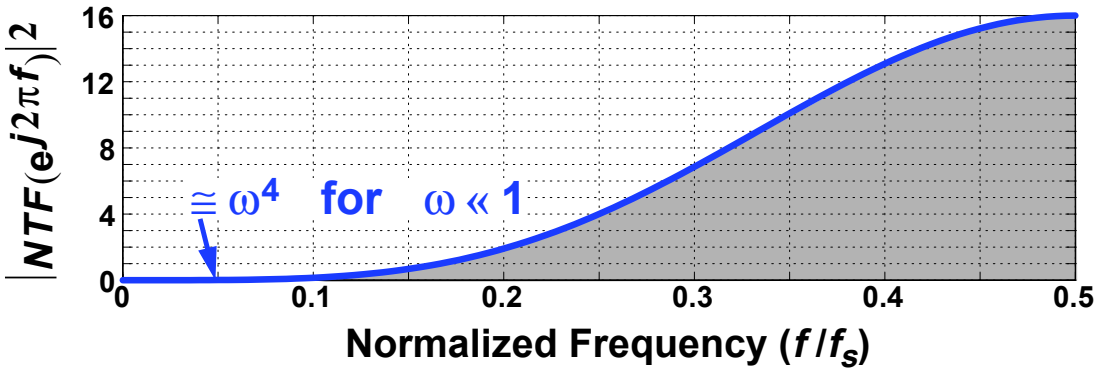
$$STF(z) = z^{-1}$$



- **Doubling OSR improves SQNR by 9 dB**
  Peak SQNR $\approx$ **dbp**$(9 \cdot OSR^3/(2\pi^2))$; **dbp**$(x) \equiv 10\log_{10}(x)$

Review: MOD2

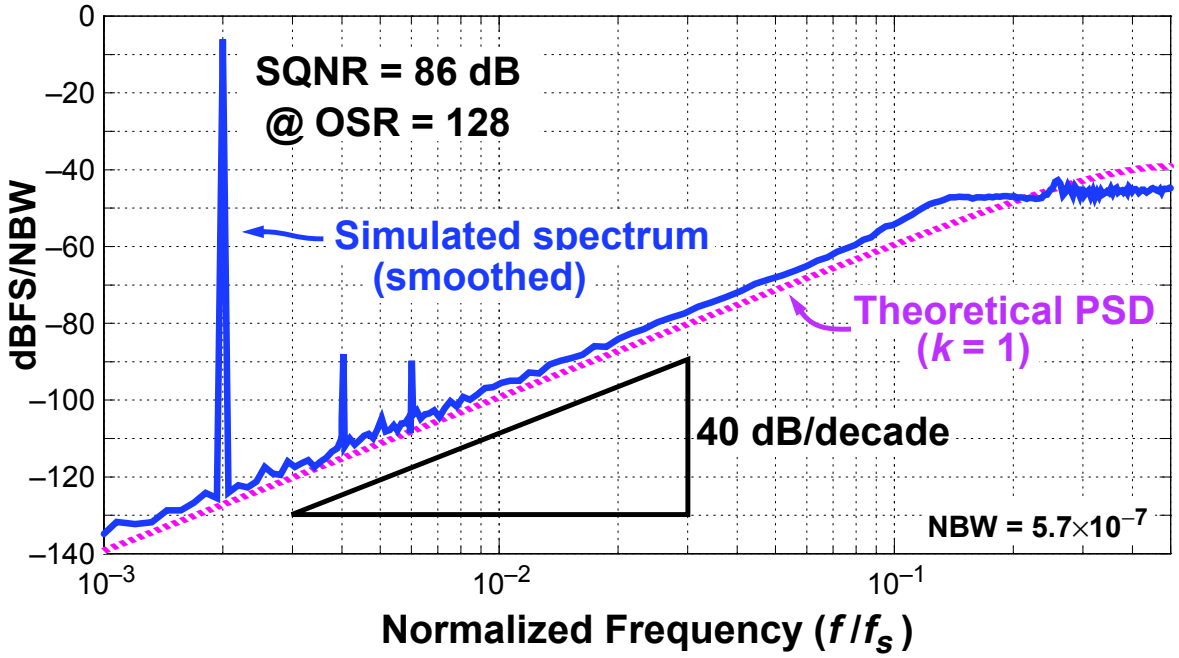




- **Doubling OSR improves SQNR by 15 dB**
  Peak SQNR ≈ dbp$((15 \cdot OSR^5)/(4\pi^4))$

Review: Simulated MOD2 PSD

Input at 50% of FullScale



Review: Advantages of $\Delta\Sigma$

- **ADC: Simplified Anti-Alias Filte**

  Since the input is oversampled, only very high frequencies alias to the passband.
  A simple RC section often suffices

  If a continuous-time loop filter is used, the anti-alia filter can often be eliminated alto ether.

- **DAC: Simplified Reconstruction Filte**

  The nearby images present in Nyquist-rate reconstruction can be removed digitally.

+ **Inherent Linearity**

  Simple structures can yield very high SNR.

+ **Robust Implementation**

  $\Delta\Sigma$ tolerates sizable component errors.

Let's Try Making One!

- **Clock at f_s = 1 MHz.**
  Assume BW = 1 kHz.

$\Rightarrow$ $OSR = f_s/(2 \cdot BW) = 500 \approx 2^9$

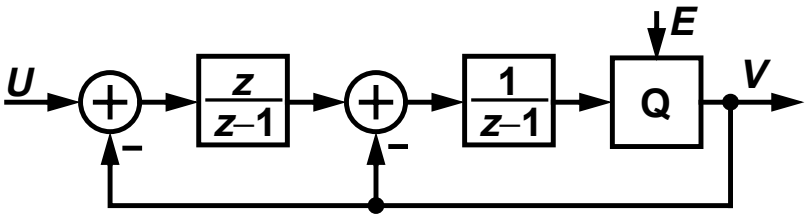
- **MOD1: SQNR $\approx$ 9 dB/octave • 9 octaves = 81 dB**
- **MOD2: SQNR $\approx$ 15 dB/octave • 9 octaves =135 dB**

  Actually more like 120 dB.

- **SQNR of MOD1 is not bad, but SQNR of MOD2 is awesome!**

  In addition to MOD2's SQNR advantage, MOD2 is usually preferred over MOD1 because MOD2's quantization noise is more well-behaved.

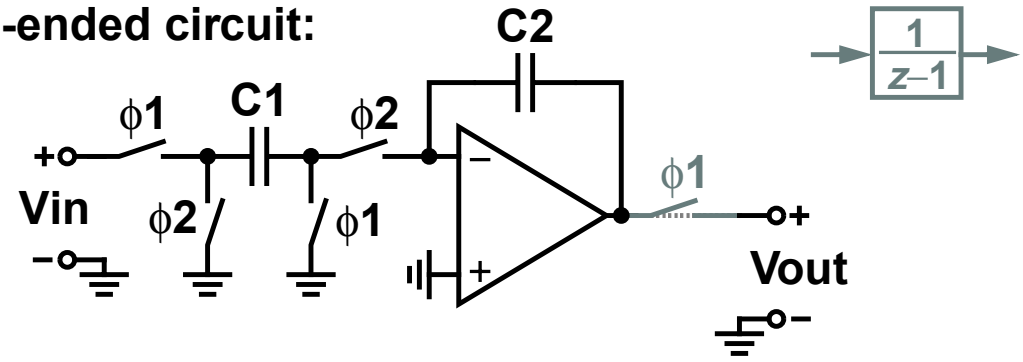
What Do We Need?



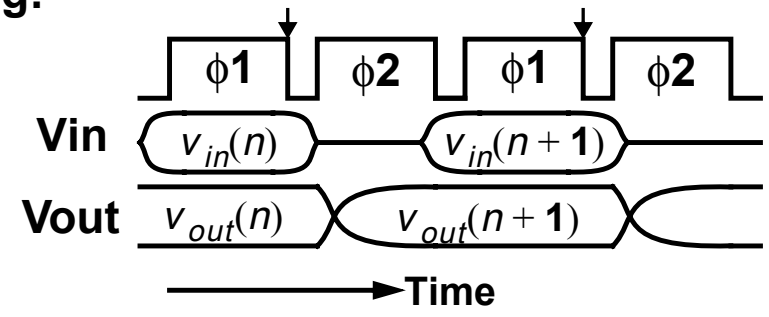
1. Summation blocks
2. Delaying and non-delaying discrete-time integrators
3. Quantizer (1-bit)
4. Feedback DACs (1-bit)
5. Decimation filter (not shown)
   - Digital and therefore “easy.”

Switched-Capacitor Integrator

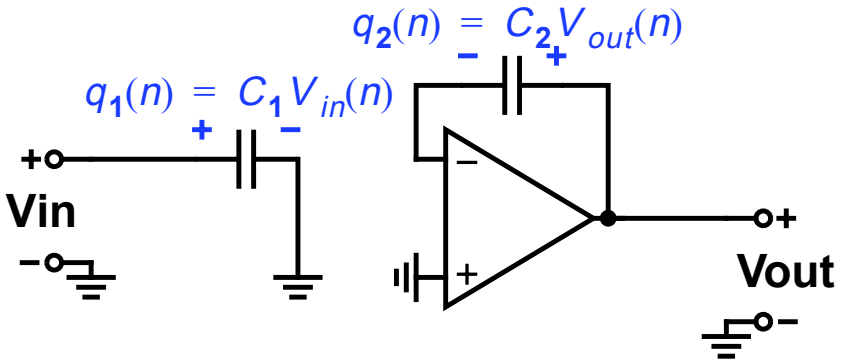
Single-ended circuit:



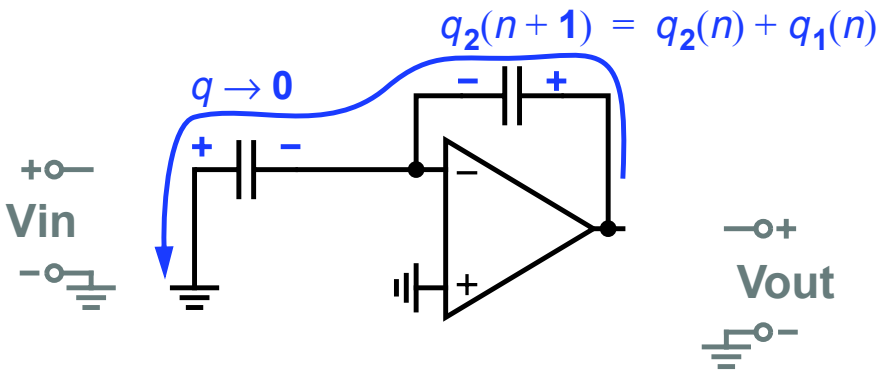
Timing:



$\phi 1$:



$\phi 2$:



$$q_2(n+1) = q_2(n) + q_1(n)$$

$$zQ_2(z) = Q_2(z) + Q_1(z)$$

$$Q_2(z) = \frac{Q_1(z)}{z-1}$$

- **This circuit integrates charge**

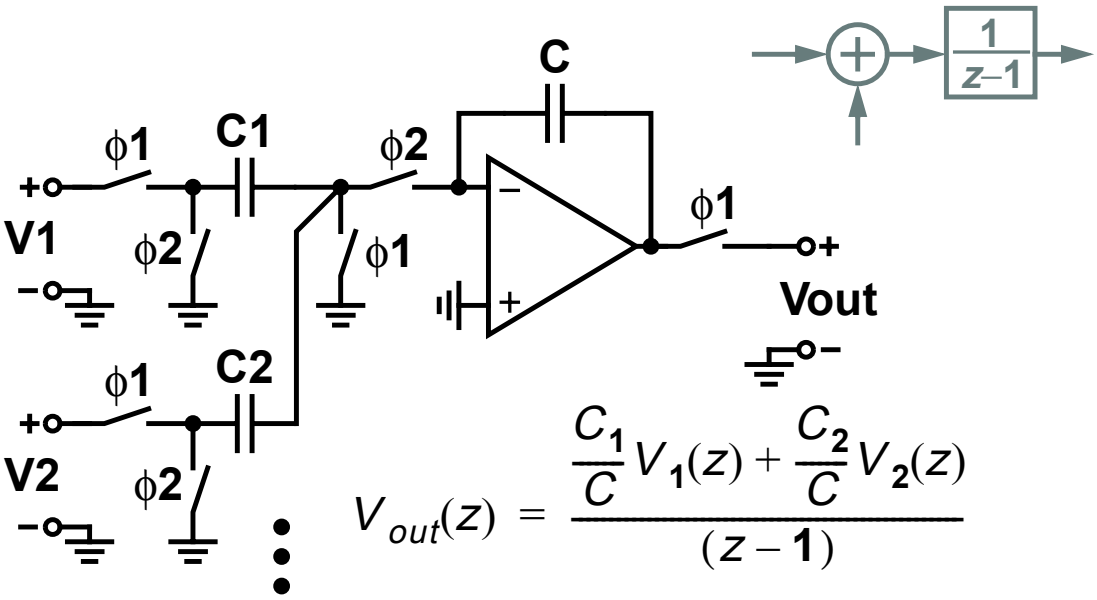
- **Since $Q_1 = C_1 V_{in}$ and $Q_2 = C_2 V_{out}$**

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1/C_2}{z-1}$$

- **Note that the voltage gain is controlled by a *ratio* of capacitors**

  With careful layout, 0.1% accuracy is possible.

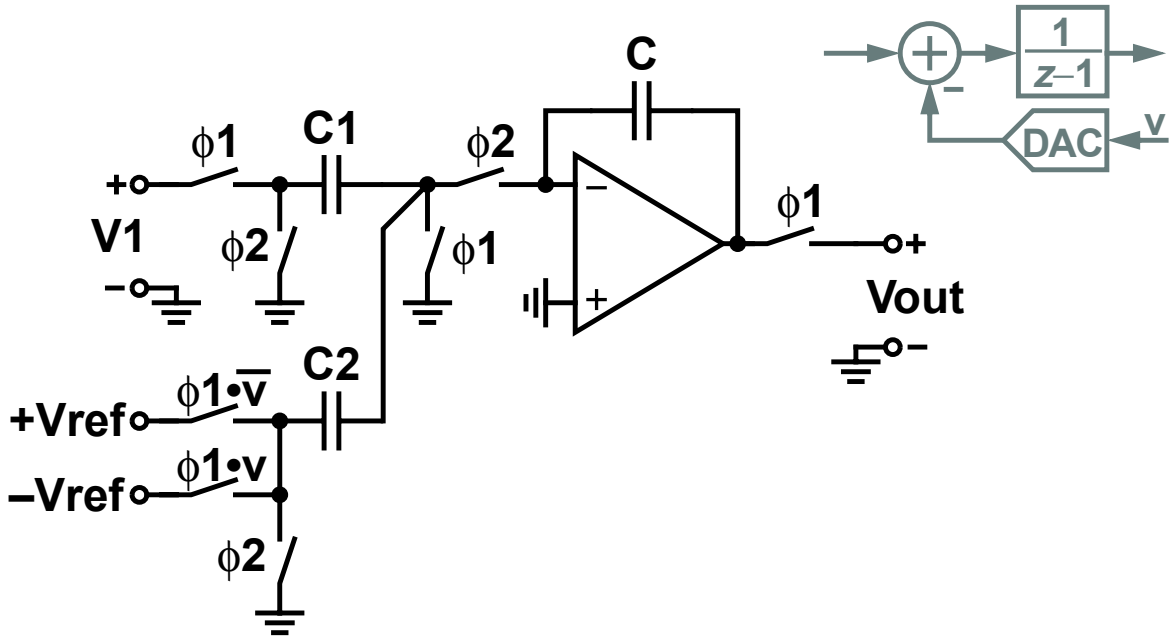
Summation + Integration



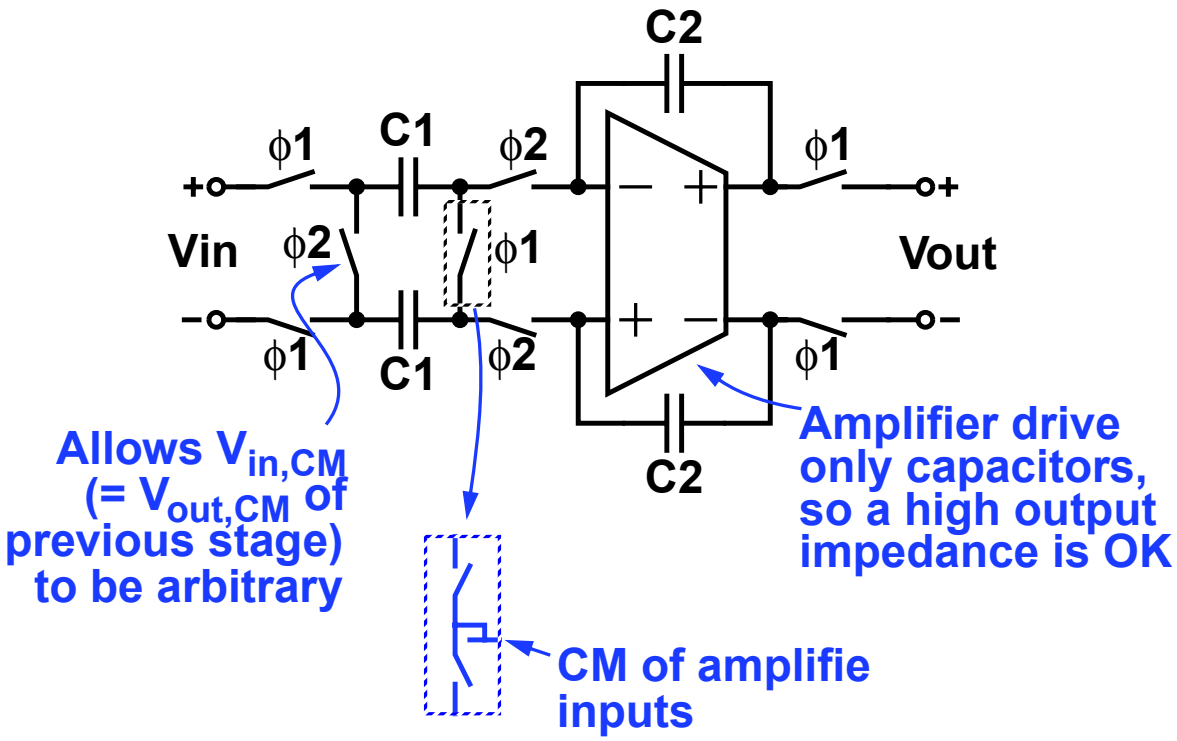
$$V_{out}(z) = \frac{\frac{C_1}{C}V_1(z) + \frac{C_2}{C}V_2(z)}{(z-1)}$$

⇒ **Adding an extra input branch accomplishes addition, with weighting**

1b DAC + Summation + Integration

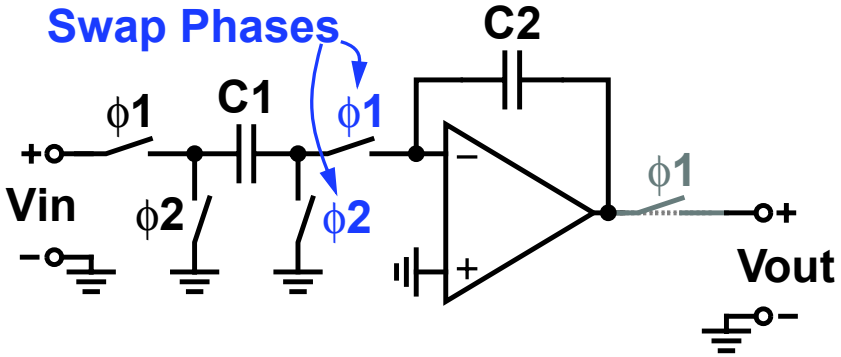


Differential Integrator

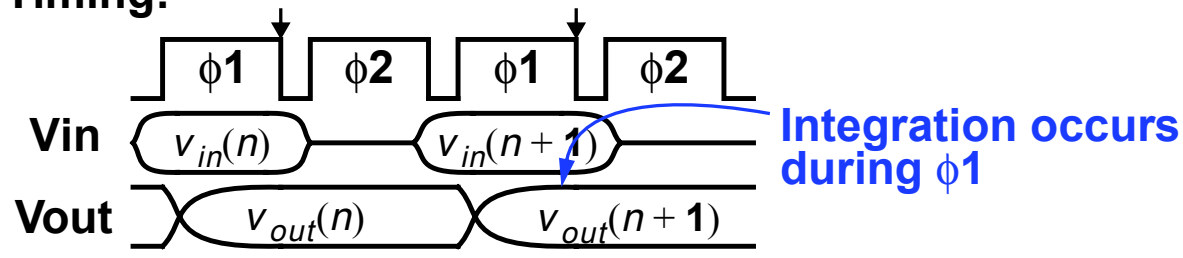


Non-Delaying Integrator

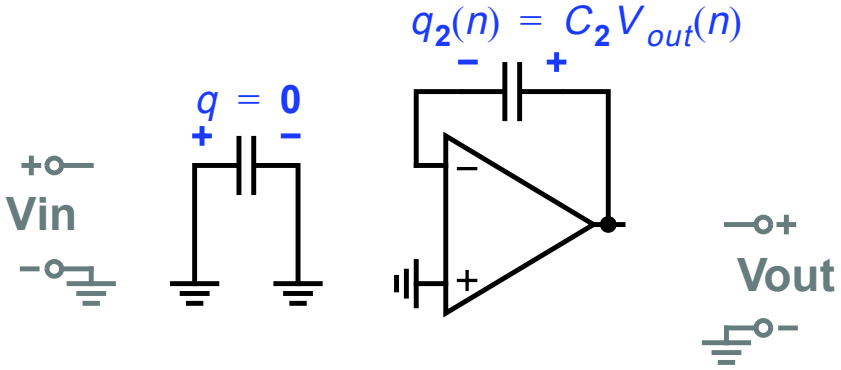
Single-ended circuit:



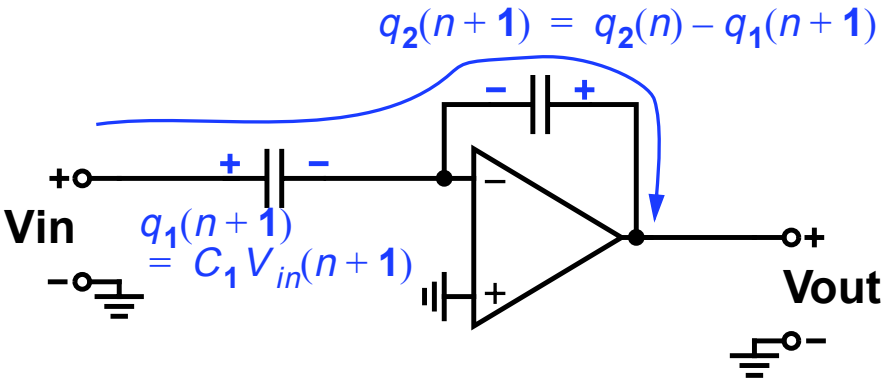
Timing:



ϕ2:



ϕ1:



$$q_2(n+1) = q_2(n) - q_1(n+1)$$

$$zQ_2(z) = Q_2(z) - zQ_1(z)$$

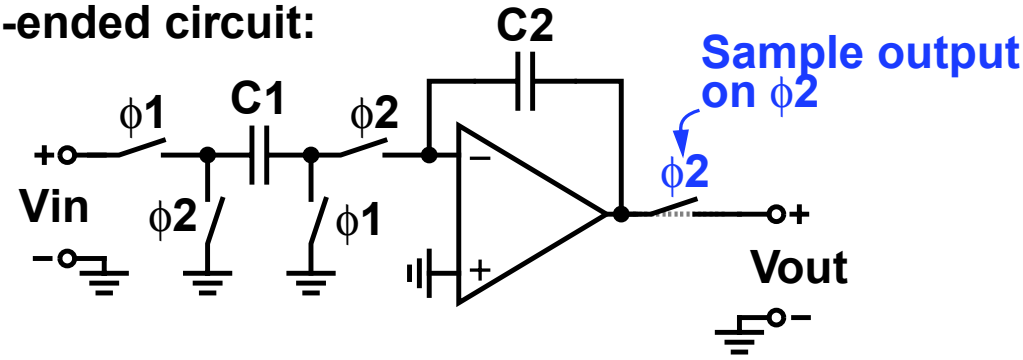
$$\frac{Q_2(z)}{Q_1(z)} = -\frac{z}{z-1}$$

$$\frac{V_{out}(z)}{V_{in}(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1}$$

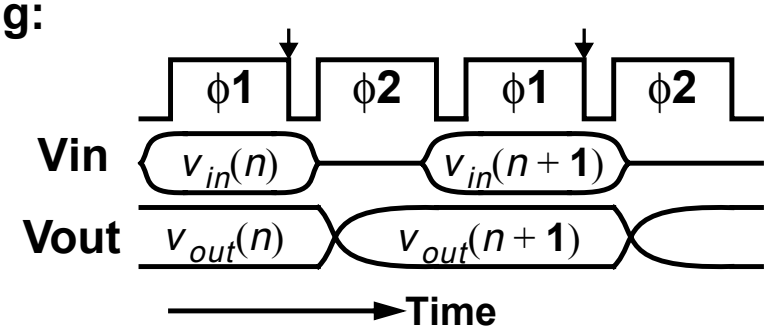
- **Delay-free integrator (inverting)**

"Half-Delay" Integrator

Single-ended circuit:



Timing:



Half-Delay Integrator

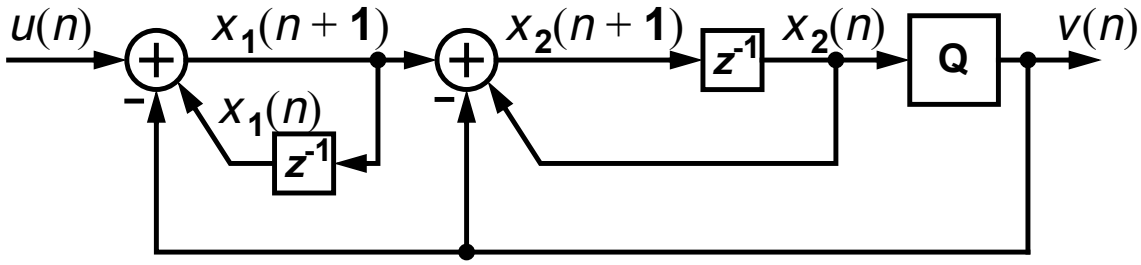
- **Output is sampled on a different phase than the input**
- **Some use the notation $H(z) = \frac{z^{-1/2}}{z-1}$ to denote the shift in sampling time**

  I consider this an abuse of notation.
- **An alternative method is to declare that the border between time *n* and *n*+1 occurs at the end of a specific phase, say ϕ2**

$\Rightarrow$ **A circuit which samples on ϕ1 and updates on ϕ2 is non-delaying, i.e. $H(z) = z/(z-1)$, whereas a circuit which samples on ϕ2 and updates on ϕ1 is delaying, i.e. $H(z) = 1/(z-1)$.**

Timing in a ΔΣ ADC

- **The safest way to deal with timing is to construct a timing diagram and verify that the circuit implements the desired difference equations**
- **E.g. MOD2:**



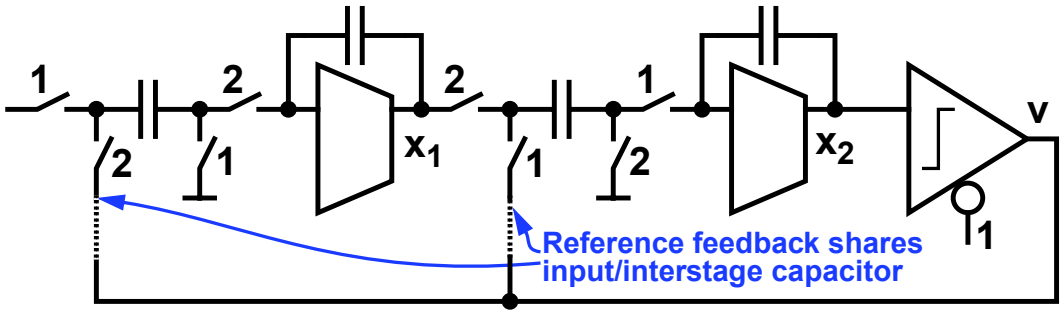
Difference Equations:

$$v(n) = Q(x_2(n)) \quad \textbf{(0)}$$

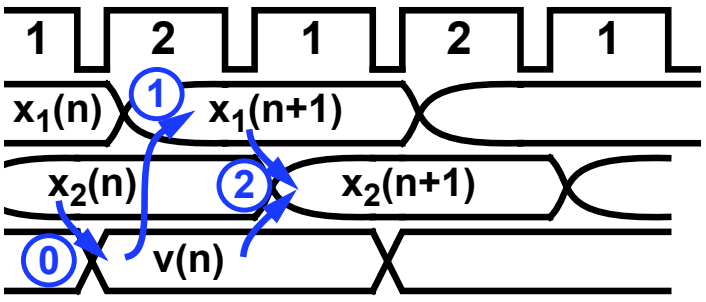
$$x_1(n+1) = x_1(n) - v(n) + u(n) \quad \textbf{(1)}$$

$$x_2(n+1) = x_2(n) - v(n) + x_1(n+1) \quad \textbf{(2)}$$

Switched-Capacitor Realization



Timing



Timing looks OK!

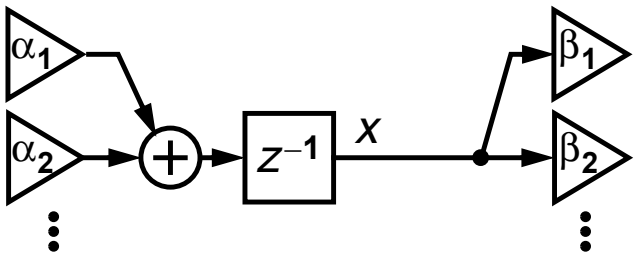
Signal Swing

- So far, we have not paid any attention to how much swing the op amps can support, or to the magnitudes of u, V_{ref}, x_1 and x_2
- For simplicity, assume:
  the full-scale range of u is ± 1 V,
  the op-amp swing is also ± 1 V and
  $V_{ref} = 1$ V
- We still need to know the ranges of x_1 and x_2 in order to accomplish *dynamic-range scaling*

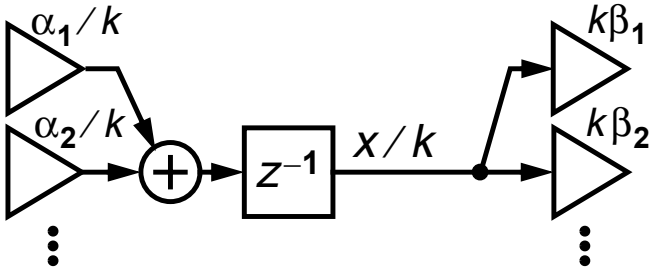
Dynamic-Range Scaling

- In a linear system with known state bounds, the states can be scaled to occupy any desired range

e.g. one state of original system:



state scaled by 1/*k*:



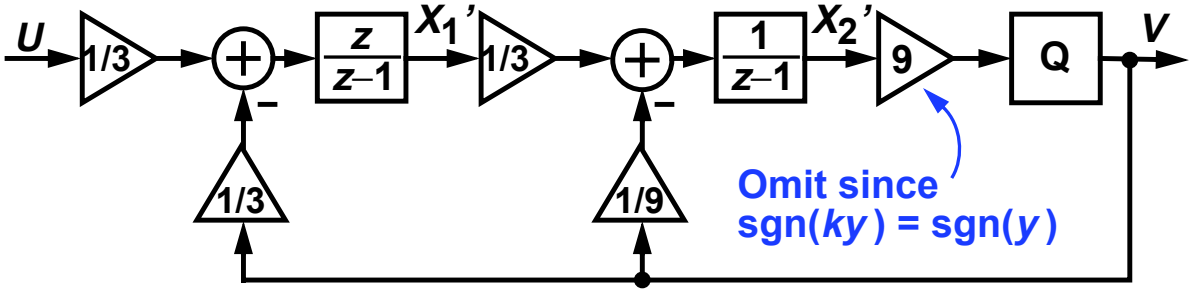
Scaled MOD2

- Take $\|x_1\|_\infty = 3$ and $\|x_2\|_\infty = 9$

  The first integrator should not saturate.

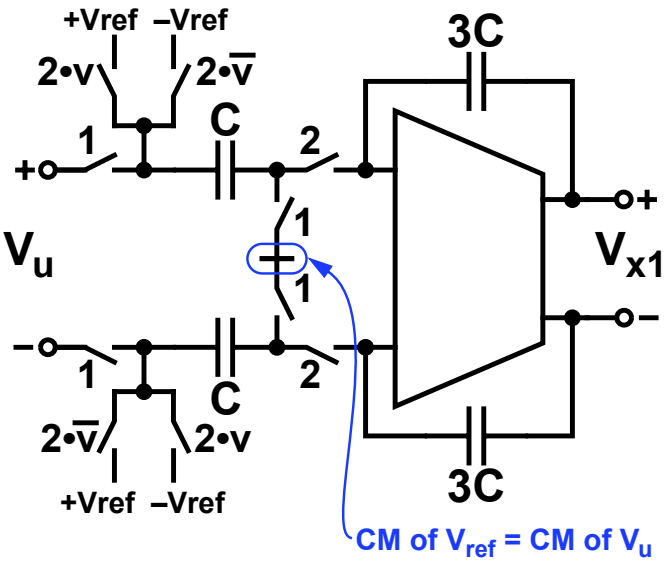
  The second integrator will not saturate for dc inputs up to –3 dBFS and possibly as high as –1 dBFS.

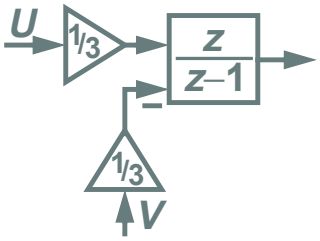
- Our scaled version of MOD2 is thus



First Integrator (INT1)

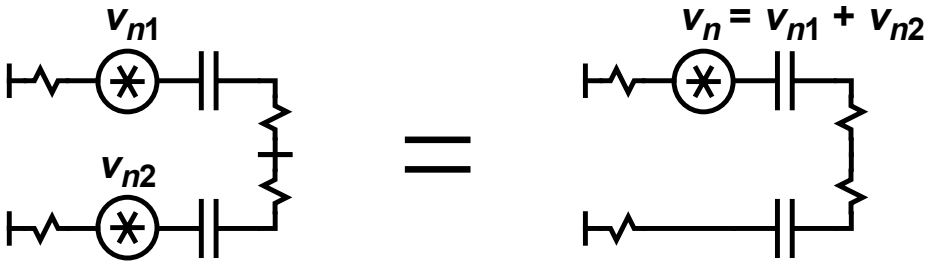
Shared Input/Reference Caps





- How do we determine C?

Differential Noise



$$\overline{v_n^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2}$$

- **Twice as many switched caps $\Rightarrow$ twice as much noise power**
- **The input-referred noise power in our differential integrator is**

$$\overline{v_n^2} = 4kT/C_1$$

INT1 Absolute Capacitor Sizes

For SNR = 100 dB @ –3-dBFS input

- **The signal power is**

$$\overline{v_s^2} = \underbrace{\frac{1}{2}}_{\text{–3 dBFS}} \bullet \frac{(1\text{ V})^2}{2} = 0.25\text{ V}^2$$

$\frac{A^2}{2}$

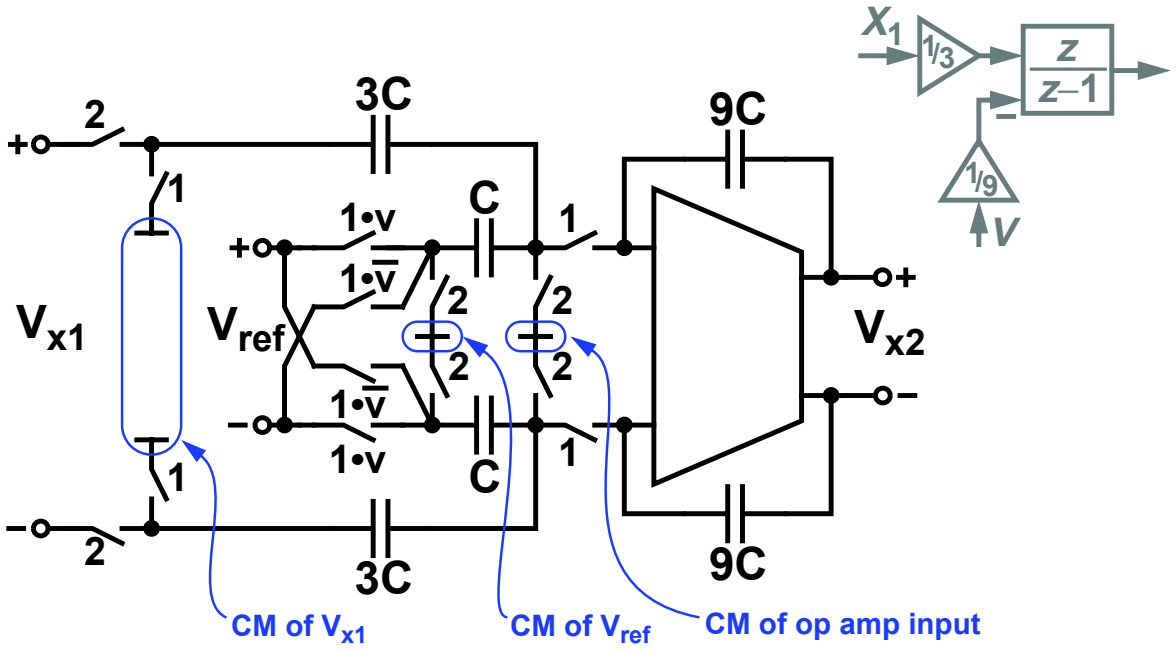
- **Therefore we want $\overline{v_{n,\text{ in-band}}^2} = 0.25 \times 10^{-10}\text{ V}^2$**
- **Since $\overline{v_{n,\text{ in-band}}^2} = \overline{v_n^2}/OSR$**

$$C_1 = \frac{4kT}{\overline{v_n^2}} = 1.33\text{ pF}$$

- **If we want 10 dB more SNR, we need 10x caps**

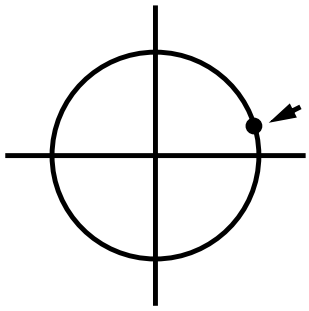
Second Integrator (INT2)

Separate Input and Feedback Caps



INT2 Absolute Capacitor Sizes

- **In-band noise of second integrator is greatly attenuated**



$\omega_B = \frac{\pi}{OSR}$

INT1 gain @ pb edge: $A = \frac{1/3}{\omega_B} = \frac{OSR}{3\pi}$

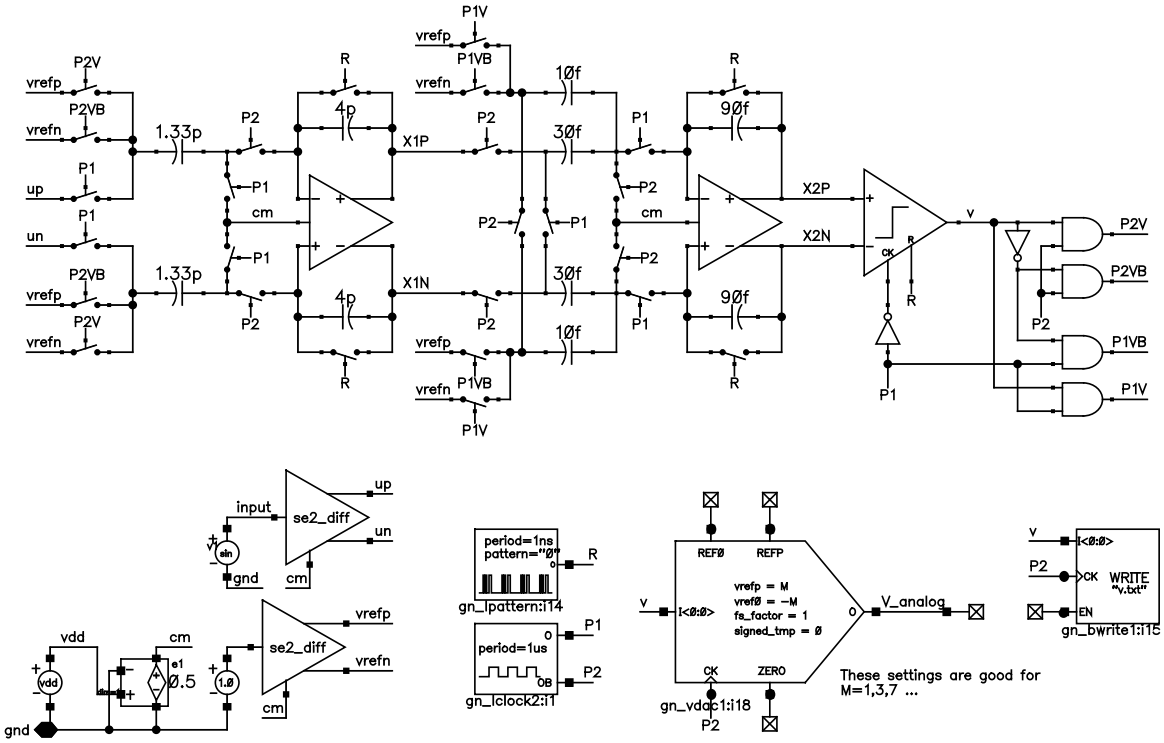
INT2 noise attenuation: $> OSR \cdot A^2 \approx 10^6$

$\Rightarrow$ **Capacitor sizes not dictated by thermal noise**

- **Charge injection errors and desired ratio accuracy set absolute size**

  A reasonable size for a small cap is currently ~10 fF.

Behavioral Schematic



Verification

Open-loop verification

1. **Loop filter**
2. **Comparator**

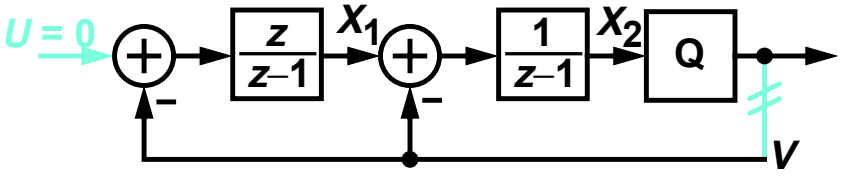
   Since MOD2 is a 1-bit system, all that can go wrong is the polarity and the timing. Usually the timing is checked by (1), so this verification step is not needed.

Closed-loop verification

3. **Swing of internal states**
4. **Spectrum: SQNR, STF gain**
5. **Sensitivity, start-up, overload recovery, …**

Loop-Filter Check— Theory

- **Open the feedback loop, set $u = 0$ and drive an impulse through the feedback path**

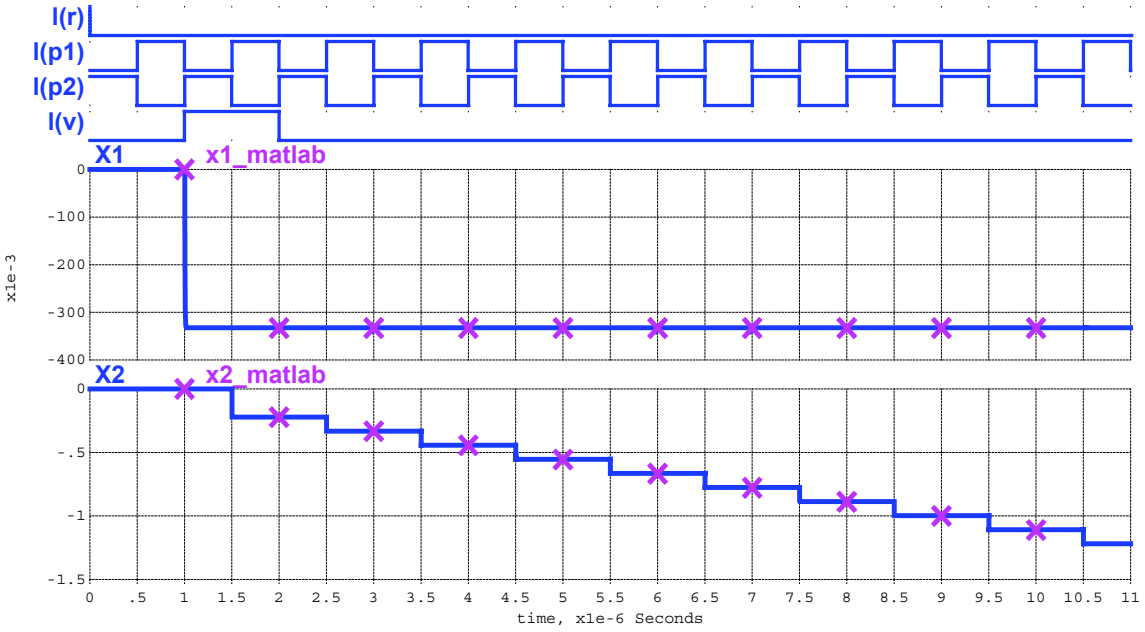


$$X_2 = \frac{-1}{z-1}\left(1 + \frac{z}{z-1}\right)Y$$

$$\therefore y(n) = \{1, 0, 0, \ldots\} \Rightarrow x_2(n) = \{-2, -3, -4, \ldots\}$$

- **If x_2 is as predicted then the loop filter is correct**
  - **At least for the feedback signal, which implies that the NTF will be as designed.**

Loop Filter Check— Practice*



*. "In theory there is no difference between theory and practice. But in practice there is."

Hey! You Cheated!

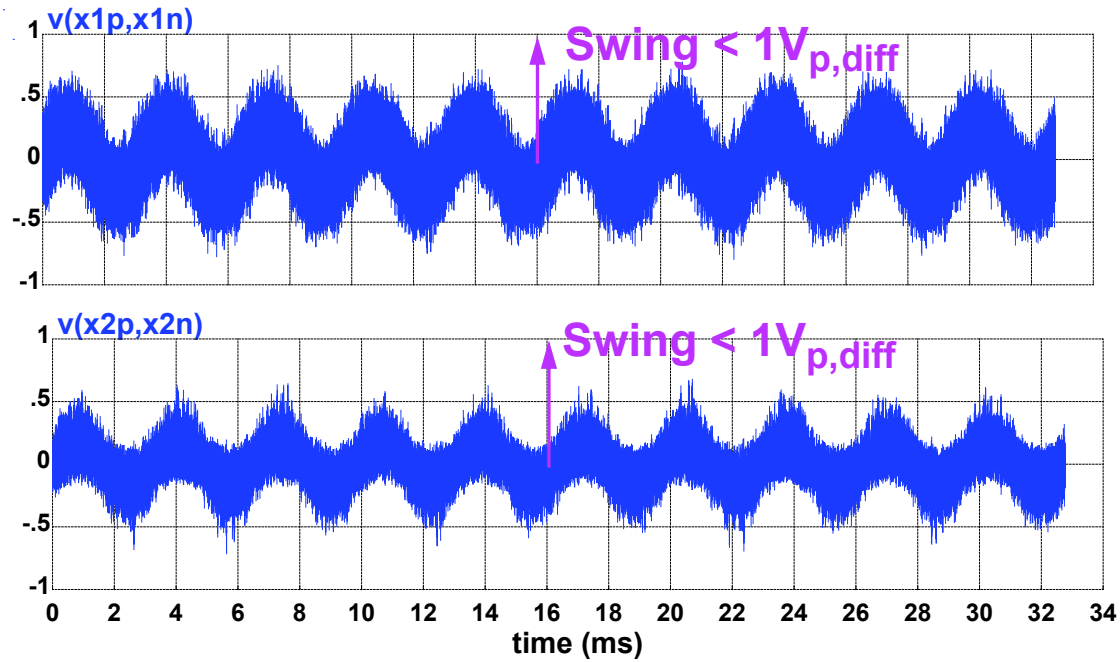
- An impulse is {1,0,0,…}, but a binary DAC can only output ±1, i.e. it cannot produce a 0

Q: So how can we determine the impulse response of the loop filter through simulation?

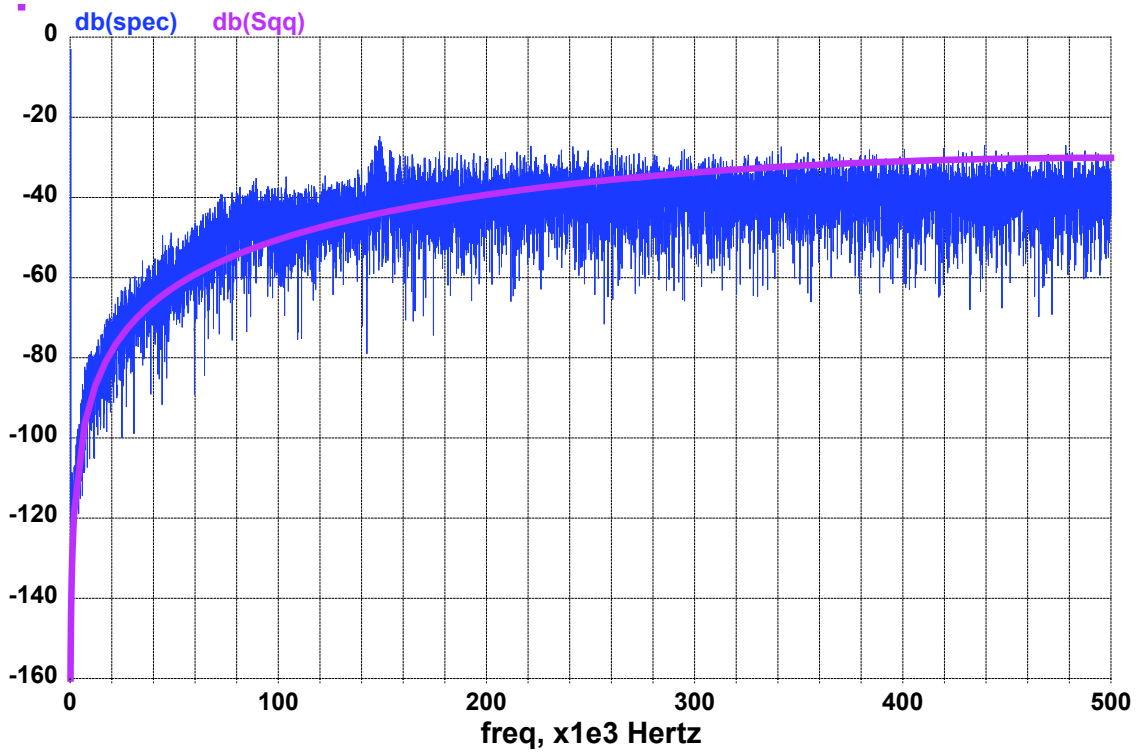
A: Do two simulations: one with v = {–1,–1,–1,…} and one with v = {+1,–1,–1,…}.
Then take the difference.
According to superposition, the result is the response to v = {2,0,0,…}, so divide by 2.

To keep the integrator states from growing too quickly, you could also use v = {–1,–1,+1,–1,…} and then v = {+1,–1,+1,–1,…}.

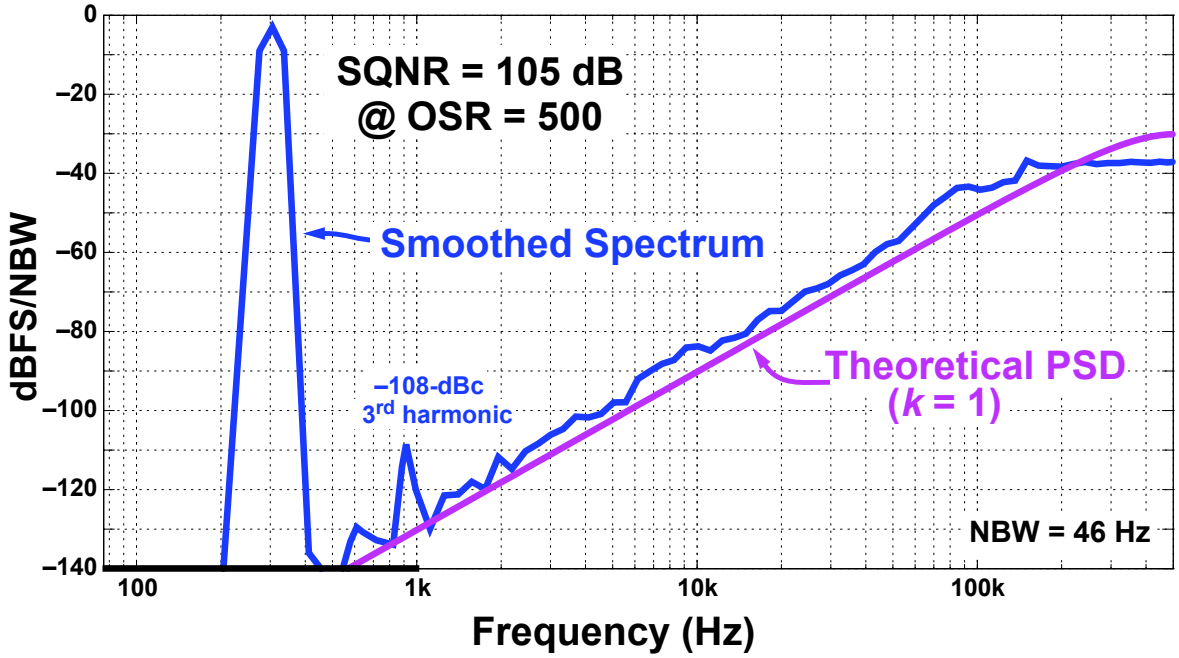
Simulated State Swings
–3-dBFS ~300-Hz sine wave



Unclear Spectrum



Professional Spectrum



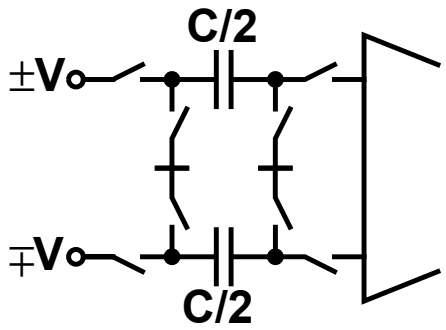
- **SQNR dominated by –109-dBFS 3rd harmonic**

Implementation Summary

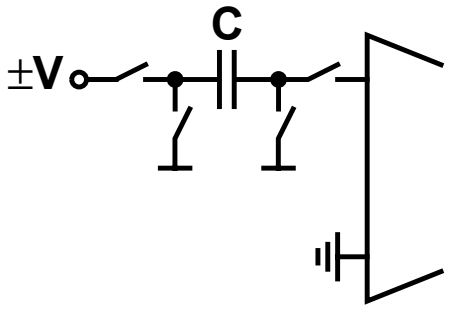
1. **Choose a viable SC topology and manually verify timing**
2. **Do dynamic-range scaling**
   - **You now have a set of capacitor ratios.**
   - **Verify operation: loop filter, timing, swing, spectrum.**
3. **Determine absolute capacitor sizes**
   - **Verify noise.**
4. **Determine op-amp specs and construct a transistor-level schematic**
   - **Verify everything.**

Differential vs. Single-Ended

- **Differential is more complicated and has more caps and more noise ⇒ single-ended is better?**



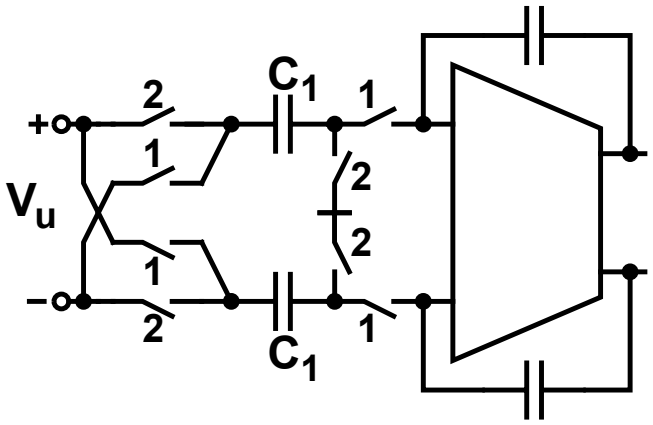
$$SNR = \frac{(2V)^2/2}{4kT/(C/2)} = \frac{CV^2}{4kT}$$



$$SNR = \frac{V^2/2}{2kT/C} = \frac{CV^2}{4kT}$$

- **Same capacitor area ⇒ same SNR**
  - **Differential is generally preferred due to rejection of even-order distortion and common-mode noise/ interference.**

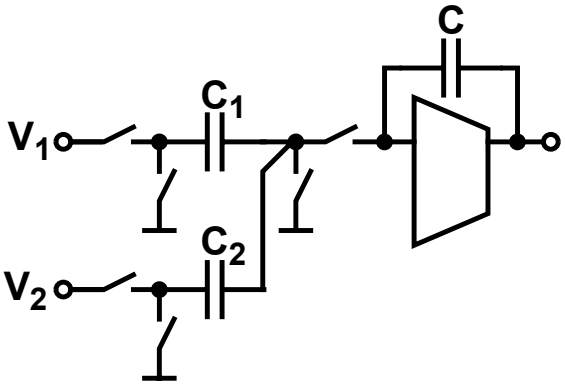
Double-Sampled Input



- **Doubles the effective input signal**
- **Allows C_1 to be 1/4 the size for the same SNR**
- **Doubles the sampling rate of the signal, thereby easing AAF further**

Shared vs. Separate Input Caps

- **Separate caps ⇒ More noise:**



V_1 input: $\overline{v_{n1}^2} = 2kT/C_1$

V_2 input: $\overline{v_{n2}^2} = 2kT/C_2$

V_2 gain / V_1 gain: C_2/C_1

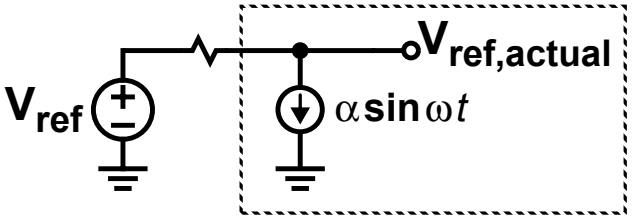
v_{n2} referred to V_1: $v_{n2}C_2/C_1$

Total noise referred to V_1:
$(2kT/C_1)(1 + C_2/C_1)$

- **But using separate caps allows input CM to be different from reference CM, and so is often preferred in a general-purpose ADC**

Signal-Dependent Ref. Loading

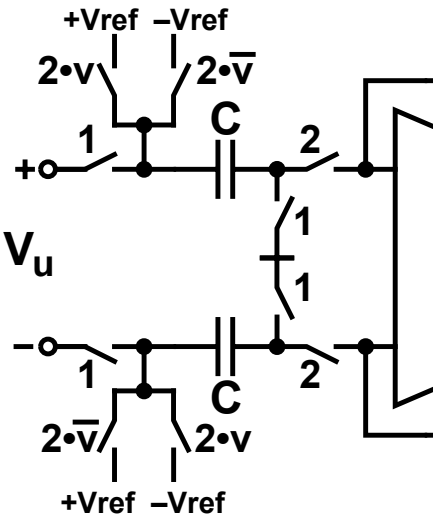
- **Another practical concern is the current draw from the reference**

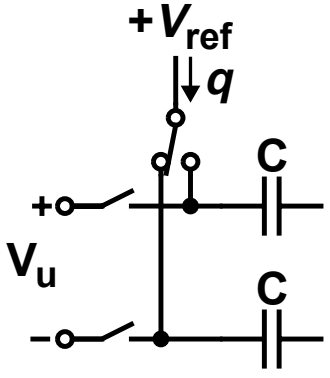


$$\text{ADC Output} \propto \frac{V_{in}}{V_{ref}(1-\varepsilon \sin \omega t)} \approx \frac{V_{in}}{V_{ref}}(1+\varepsilon \sin \omega t)$$

- **If the reference current is signal-related, harmonic distortion can result**

Shared Caps and Ref. Loading





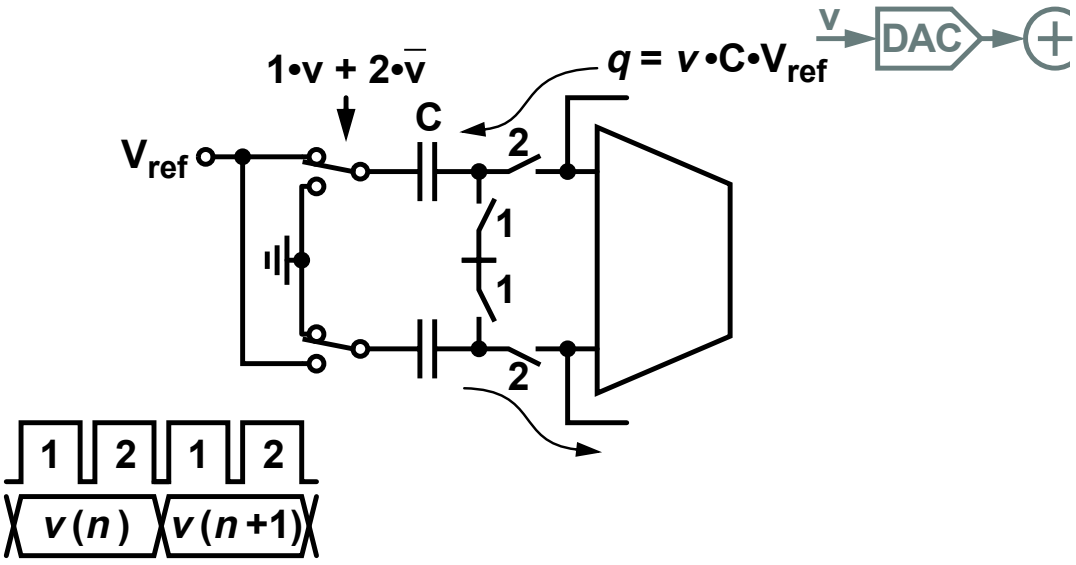
$$q = \begin{cases} C(V_{ref} - V_u/2)\ , & v = +1 \\ C(V_{ref} + V_u/2)\ , & v = -1 \end{cases}$$

Thus

$$\bar{I} = \frac{C}{T}(V_{ref} - v \cdot V_u/2)$$

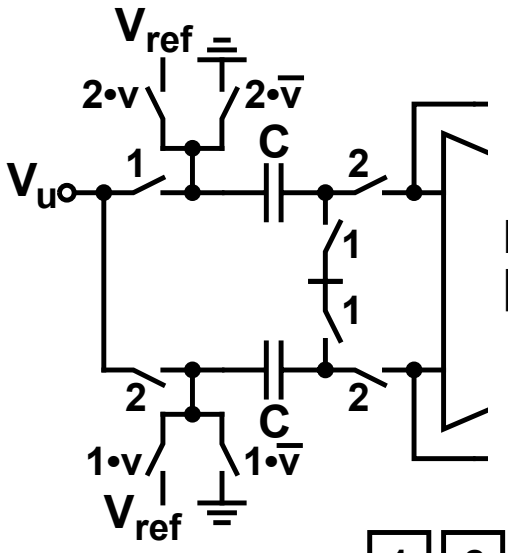
- **If $u = A\sin\omega_u t$, then $v = u + error$ also contains a component at ω_u and thus *I* contains a component at $\omega = 2\omega_u$.**
- **Since ADC Output $\propto V_{in}(1 + \varepsilon\sin\omega t)$, the signal-dependent reference current in our circuit can produce 3rd-harmonic distortion**
  - **Also, the load presented to the driving circuit is dependent on *v* and this noisy load can cause trouble.**
- **With separate caps, the reference current is signal-independent**
  - **Yet another reason for using separate caps.**

Unipolar Reference

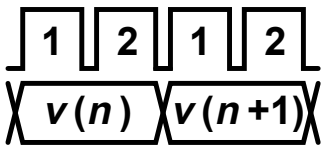


- **Be careful of the timing of *v* relative to the integration phase!**

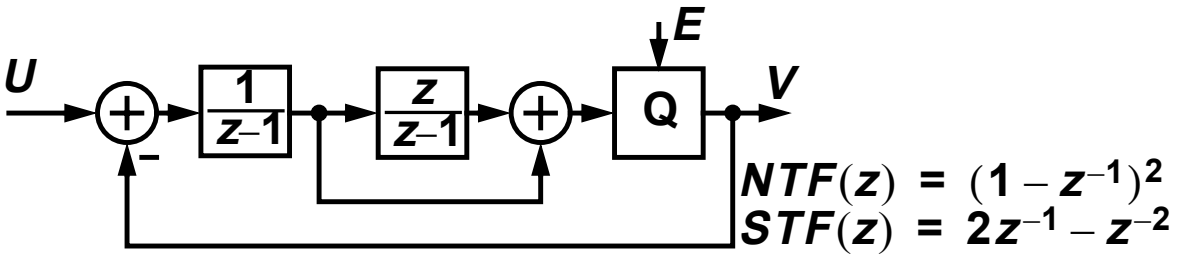
Single-Ended Input
Shared Caps



Full-scale range of V_u is $[0,V_{ref}]$.

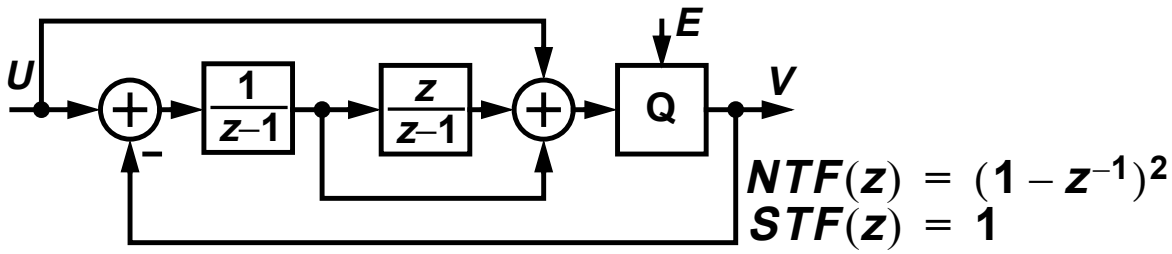


Topological Variant– Feed-Forward



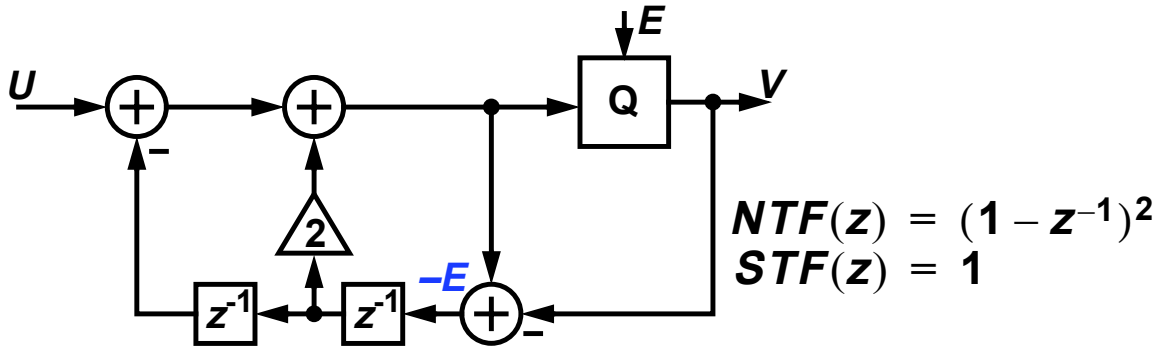
+ Output of first integrator has no DC component
  - Dynamic range requirements of this integrator are relaxed.
– Although $|STF| \approx 1$ near $\omega = 0$, $|STF| = 3$ for $\omega = \pi$
  - Instability is more likely.

Topological Variant– Feed-Forward with Extra Feed-In



+ No DC component in either integrator's output
  Reduced dynamic range requirements in both integrators, esp. for multi-bit modulators.
+ Perfectly flat STF
  No increased risk of instability.
– Timing is tricky

Topological Variant– Error Feedback



+ Simple
– Very sensitive to gain errors
  Only suitable for digital implementations.

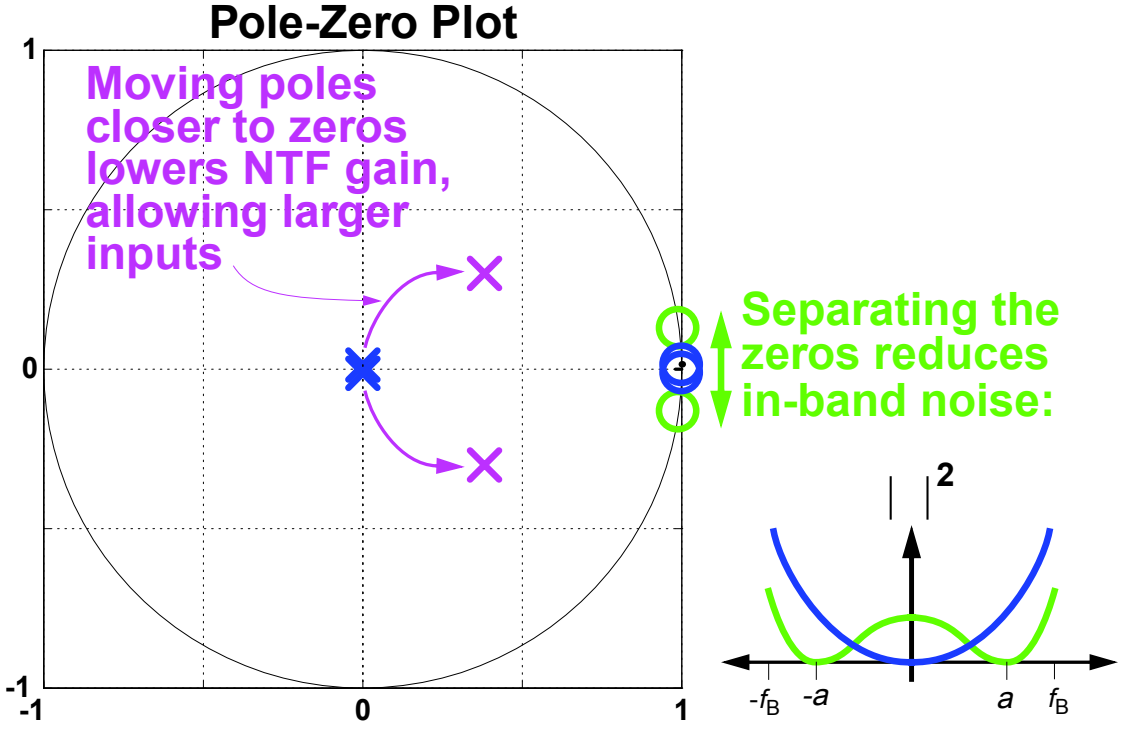
Is MOD2 The Only 2nd-Order Modulator?

- Except for the filtering p ovided by the STF, any modulator with the same NTF as MOD2 has the same input-output behavior as MOD2
  - SQNR curve is the same.
  - Tonality of the quantization noise is unchanged.
- Internal states, sensitivity, thermal noise etc. can differ from realization to realization

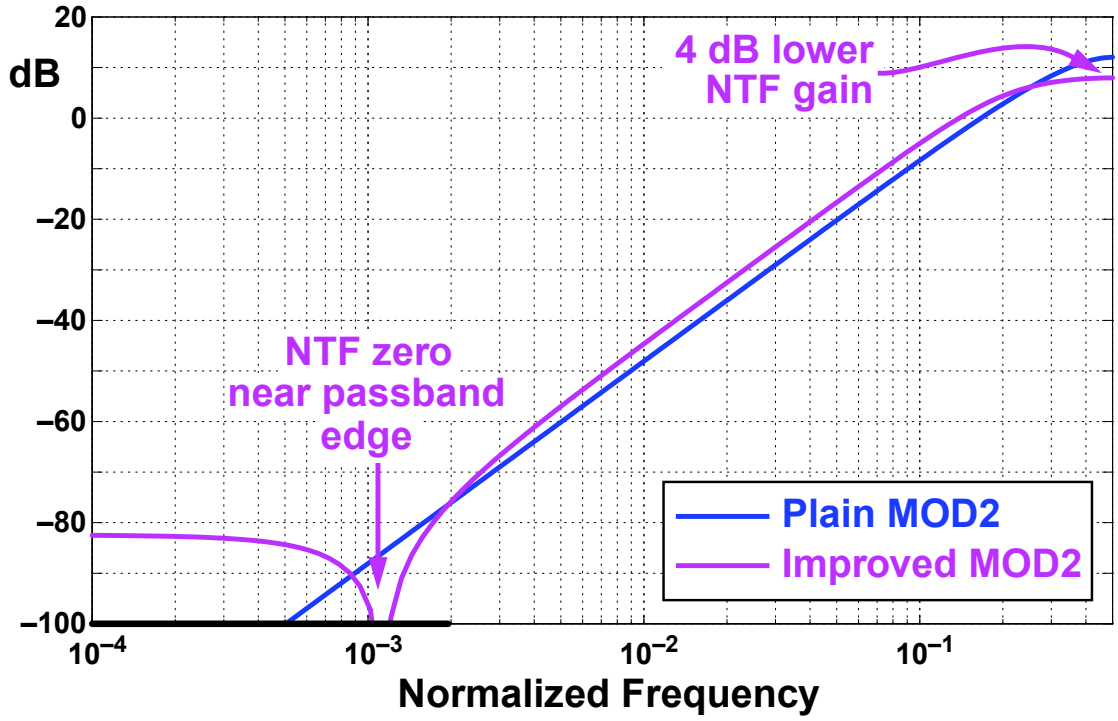
BUT, in terms of input-output behavior,

- A 2nd-order modulator is truly different only if it possesses a truly different (2nd-order) NTF

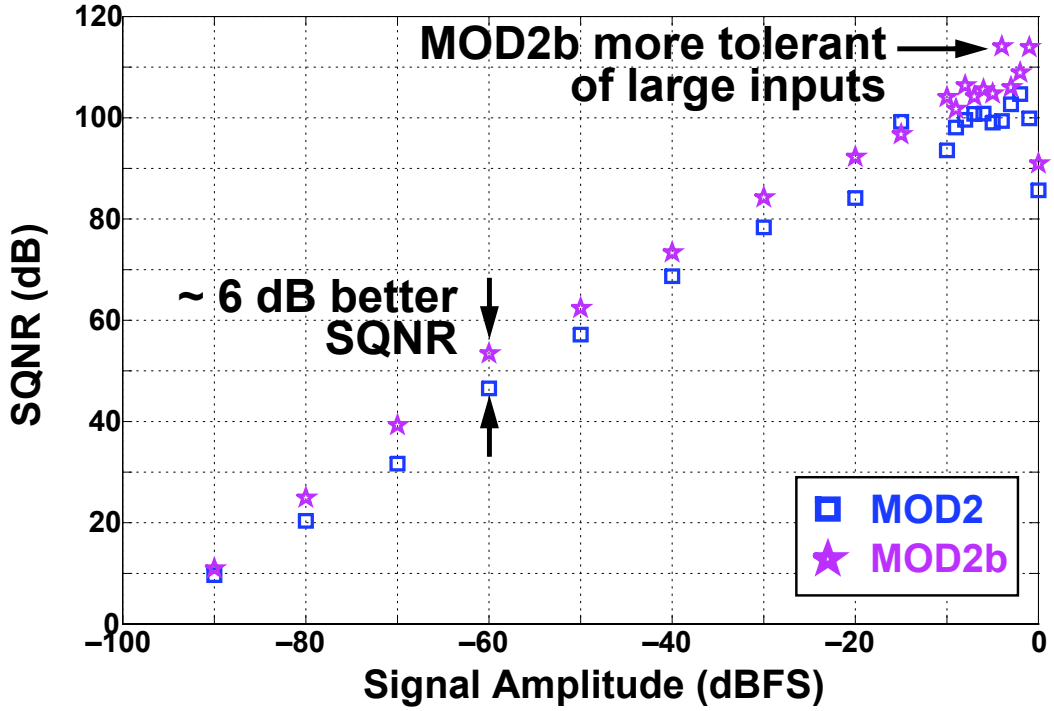
A Better 2nd-Order NTF



NTF Comparison

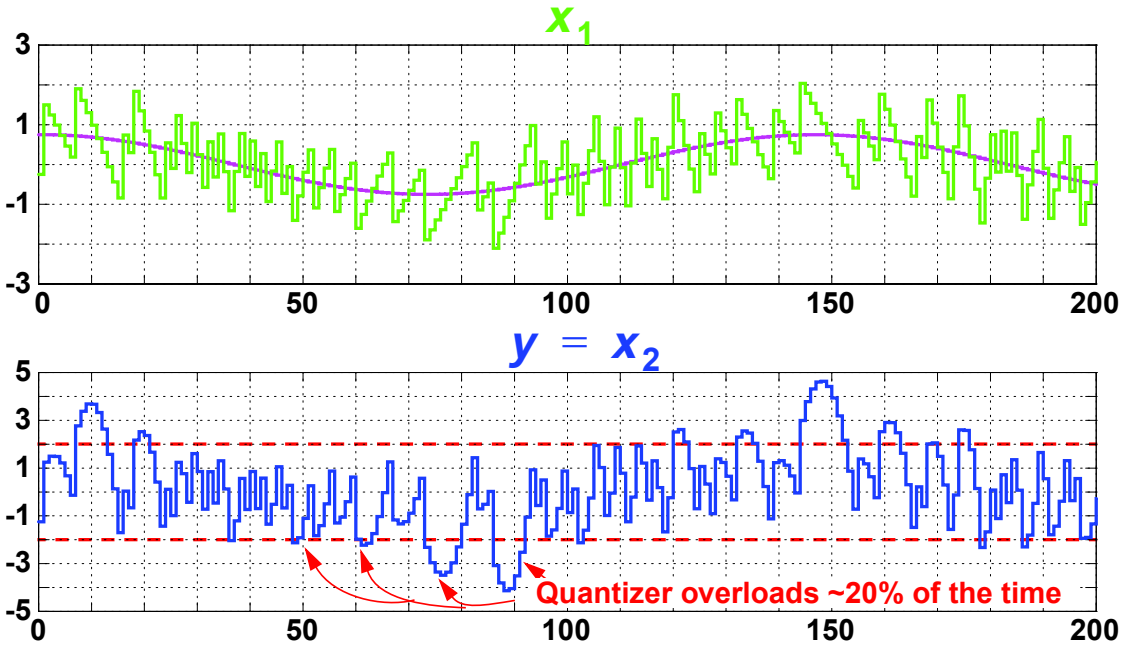


SNR vs. Amp Comparison



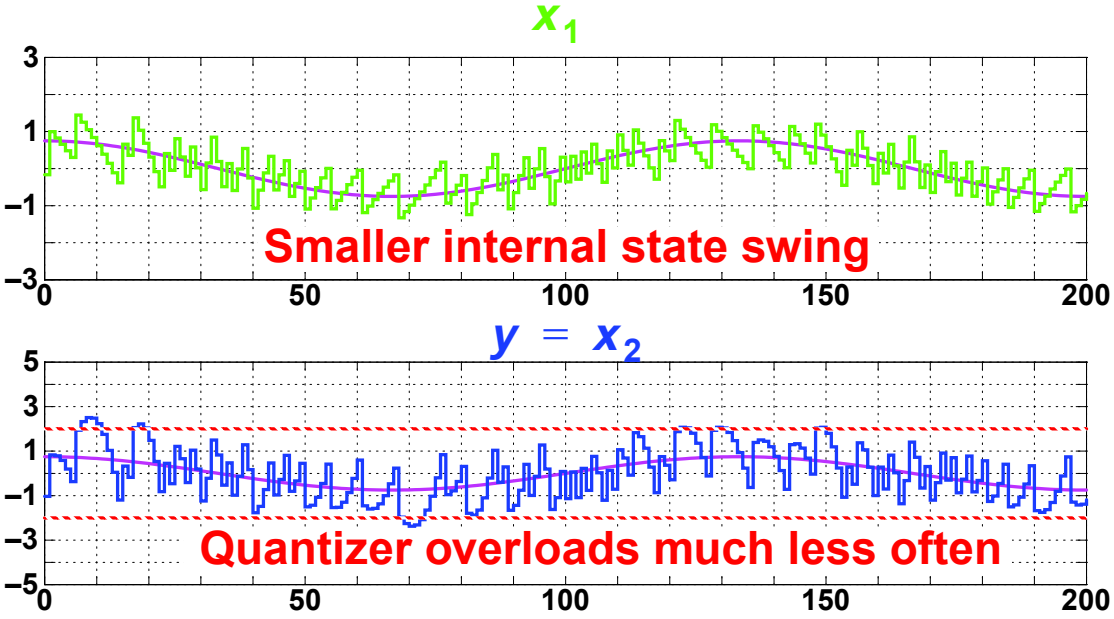
MOD2 Internal Waveforms

Input @ 75% of FS

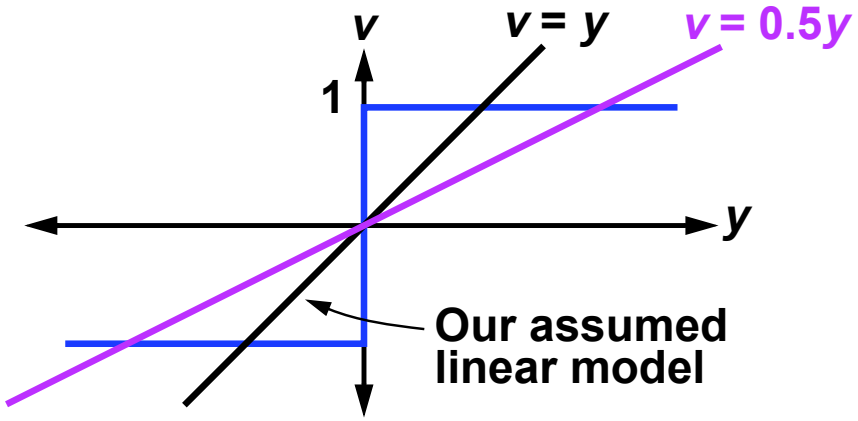


MOD2b Internal Waveforms

Input @ 75% of FS



Gain of a Binary Quantizer



- The effective gain of a binary quantizer is not known a priori
- The gain (*k*) depends on the statistics of the quantizer's input

  Halving the signal doubles the gain.

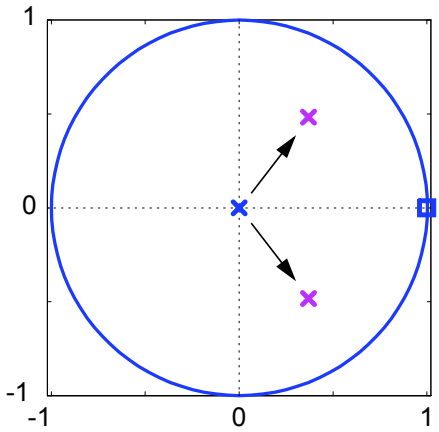
Gain of the Quantizer in MOD2

- The effective gain of a binary quantizer can be computed from the simulation data using

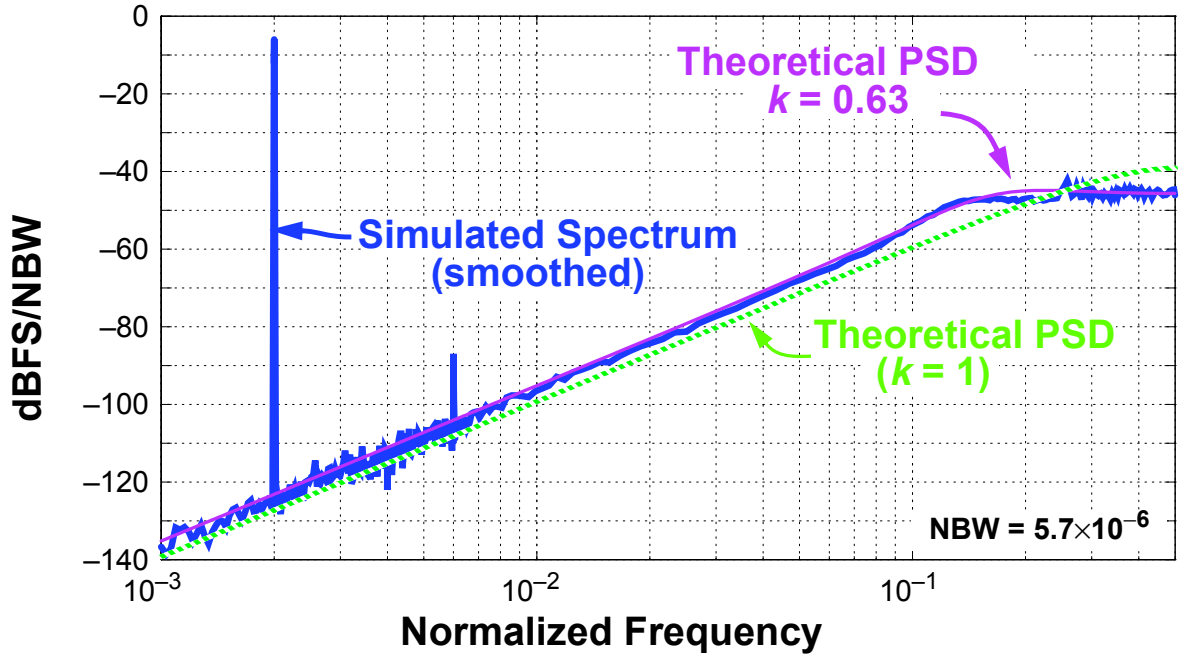
$$k = \frac{E[|y|]}{E[y^2]}$$ [S&T Eq. 2.5]

- For the simulation of 2-14, $k = 0.63$
- $k \neq 1$ alters the NTF:

$$NTF_k(z) = \frac{NTF_1(z)}{k + (1-k)NTF_1(z)}$$



Revised PSD Prediction



- **Agreement is now excellent**

Variable Quantizer Gain

- **When the input is small (below –12 dBFS), the effective gain of MOD2's quantizer is $k = 0.75$**
- **MOD2's "small-signal NTF" is thus**

$$NTF(z) = \frac{(z-1)^2}{z^2 - 0.5z + 0.25}$$

- **This NTF has 2.5 dB less quantization noise suppression than the $(1 - z^{-1})^2$ NTF derived from the assumption that $k = 1$**

  Thus the SQNR should be about 2.5 dB lower than ✳.

- **As the input signal increases, k decreases and the suppression of quantization noise degrades**

  SQNR increases less quickly than the signal power. Eventually the SQNR saturates and then decreases as the signal power reaches full-scale.