University of Toronto

Final Exam - Online

Date — Dec 17, 2020: 6:30pm

Duration — 3 hrs (submit by 9:30pm)

ECE 331 — Analog Electronics

Lecturer — D. Johns

- Open book (Equation sheet is on the last page for convenience)
- Unless otherwise stated, assume $g_m r_o \gg 1$
- Notation: 15e3 is equivalent to 15×10^3
- Grading indicated by [ ].
- Upload your solutions as a **single pdf file**
- At the beginning of the first page of your solution, write

  Last Name; First Name; Student Number; SEED Number:

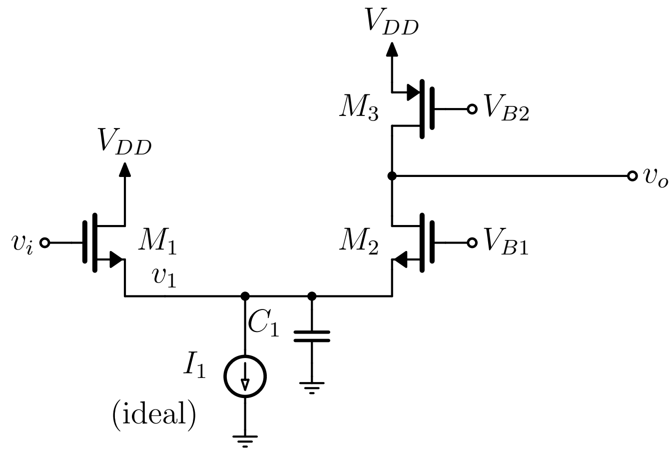
  (SEED number is shown below)

Question	1	2	3	4	5	6	Total
Points:	6	6	6	6	6	6	36
Score:							

Grading Table

SEED: 01

Q1. Consider the amplifier stage shown below and only consider the shown capacitors.



All transistor have the same g_m and r_o

$g_m = 800\,\mu\text{A/V}$

$r_o = 40\,\text{k}\Omega$

$C_1 = 1.4\,\text{pF}$

[3] (a) Find the small-signal dc gain v_o/v_i?

Solution

$r_{s1} = 1/g_{m1} = 1/(800e-6) = 1.25\,\text{k}\Omega$; $r_{s2} = 1/g_{m2} = 1/(800e-6) = 1.25\,\text{k}\Omega$

Find the short-circuit current at v_o relative to v_i assuming all $r_o \to \infty$.

$i_{sc}/v_i = 1/(r_{s1} + r_{s2}) = 1/((1.25e3) + (1.25e3)) = 400\,\mu\text{A/V}$

Find the output impedance at v_o

$R_o = r_{o3}||((1 + g_{m2} * r_{s1}) * r_{o2}) = (40e3)||((1 + (800e-6) * (1.25e3)) * (40e3)) = 26.67\,\text{k}\Omega$

The gain is given by

$v_o/v_i = i_{sc}/v_i * R_o = (400e-6) * (26.67e3) = 10.67\,\text{V/V}$

[3] (b) Find the pole frequency at node v_1 in rad/s?

Solution

Define R_x to be the impedance seen looking into the source of M_2

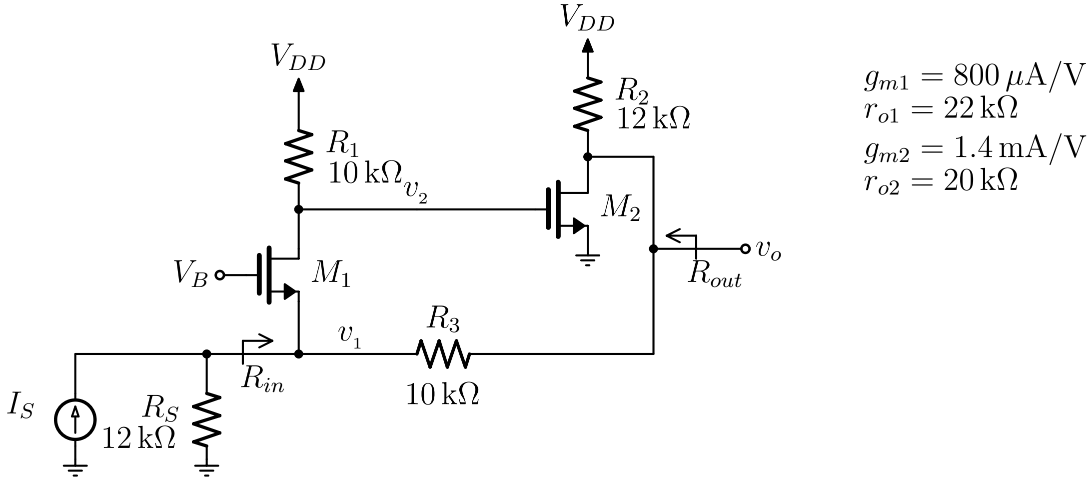
$R_x = r_{s2} + r_{o3}/(g_{m2} * r_{o2}) = (1.25e3) + (40e3)/((800e-6) * (40e3)) = 2.5\,\text{k}\Omega$

The impedance to gnd seen at node v_1 is given by

$R_{v1} = r_{s1}||R_x = (1.25e3)||(2.5e3) = 833.3\,\Omega$

The pole freq is $\omega_{p1} = 1/(R_{v1} * C_1) = 1/((833.3) * (1.4e-12)) = 857.1\,\text{Mrad/s}$

Q2. Consider feedback amp shown below where the input is a current source, I_S with a parallel resistance of R_S.



[3] (a) Find L, $A_{L\infty}$ and A_{CL}. (Assume $A_{L0} = 0$)

Solution

Define R_x to be the impedance looking into the source of M_1

$R_x = 1/g_{m1} + R_1/(g_{m1} * r_{o1}) = 1/(800e-6) + (10e3)/((800e-6)*(22e3)) = 1.818\,\mathrm{k\Omega}$

Define R_y to be the impedance at the v_o node with the loop broken

$R_y = r_{o2}||R_2||(R_3 + R_S||R_x) = (20e3)||(12e3)||((10e3) + (12e3)||(1.818e3)) = 4.552\,\mathrm{k\Omega}$

Starting at the gate of M_2 (node v_2) and going around the loop, we have

$v_o/v_2 = -g_{m2} * R_y = -(1.4e-3)*(4.552e3) = -6.372\,\mathrm{V/V}$

$v_1/v_o = (R_S||R_x)/(R_S||R_x + R_3) = ((12e3)||(1.818e3))/((12e3)||(1.818e3) + (10e3)) = 0.1364\,\mathrm{V/V}$

$v_2/v_1 = g_{m1} * (r_{o1}||R_1) = (800e-6)*((22e3)||(10e3)) = 5.5\,\mathrm{V/V}$

$L = -v_o/v_2 * v_1/v_o * v_2/v_1 = -(-6.372)*(0.1364)*(5.5) = 4.779$

$A_{L\infty} = -R_3 = -(10e3) = -10\,\mathrm{k\Omega}$

$A_{CL} = A_{L\infty} * (L/(1+L)) = (-10e3)*((4.779)/(1+(4.779))) = -8.27\,\mathrm{k\Omega}$

[3] (b) Find R_{in} and R_{out}

Solution

For R_{out}, $R'_{out} = R_y = 4.552\,\mathrm{k\Omega}$ (from above) is the output resistance with the loop broken

$L_S = 0$ and $L_O = L$

$R_{out} = R'_{out} * (1 + L_S)/(1 + L_O) = (4.552e3)*(1+(0))/(1+(4.779)) = 787.6\,\Omega$

For R_{in}, define R_{in2} to be the input resistance that INCLUDES R_S

R'_{in2} is the input resistance (including R_S) with the loop broken

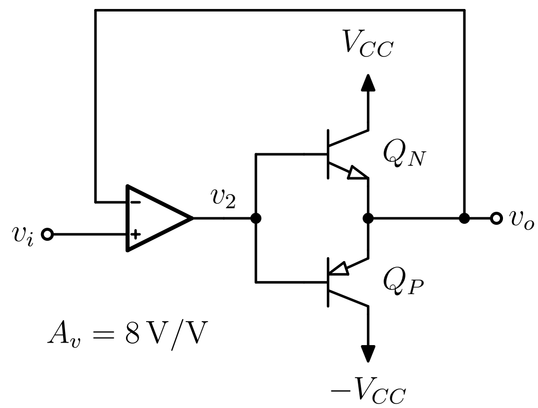
$R'_{in2} = R_S||(R_3 + r_{o2}||R_2)||R_x = (12e3)||((10e3) + (20e3)||(12e3))||(1.818e3) = 1.448\,\mathrm{k\Omega}$

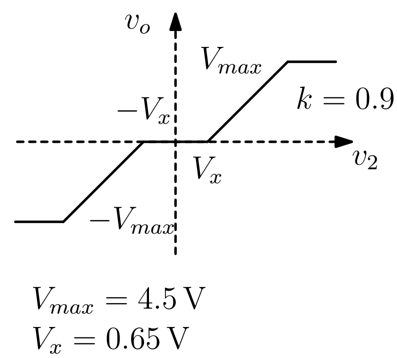
$R_{in2} = R'_{in2} * (1 + L_S)/(1 + L_O) = (1.448e3)*(1+(0))/(1+(4.779)) = 250.6\,\Omega$

Since $R_{in2} = R_S||R_{in}$ we have

$R_{in} = 1/(1/R_{in2} - 1/R_S) = 1/(1/(250.6) - 1/(12e3)) = 255.9\,\Omega$

Q3. Consider the amplifier stage shown below where the input/output characteristic for the class B output stage (from v_2 to v_o) is shown. For this class B output stage, the gain is $k = 0.9$ for $|v_2| > V_x$ until $|v_o|$ reaches V_{max} while the dead-band region results in $v_o = 0$ for $|v_2| < V_x$. The gain of the opamp is $A_v = 8\,\mathrm{V/V}$.





[2] (a) What is the dead-band region for v_i to v_o?

Solution

The dead-band region is reduced by the gain of the amplifier (the class-B output stage gain does not affect the dead-band region).

$V_x{}' = V_x/A_v = (0.65)/(8) = 81.25\,\mathrm{mV}$

[2] (b) What is the gain outside the dead-band region but before the output reaches V_{max}?

Solution

The gain outside the dead-band region and before $v_o = V_{max}$ is given by
$k' = L/(1+L)$ where L is the loop gain in the region given by
$L = A_v * k = (8) * (0.9) = 7.2$

$k' = L/(1+L) = (7.2)/(1+(7.2)) = 0.878\,\mathrm{V/V}$

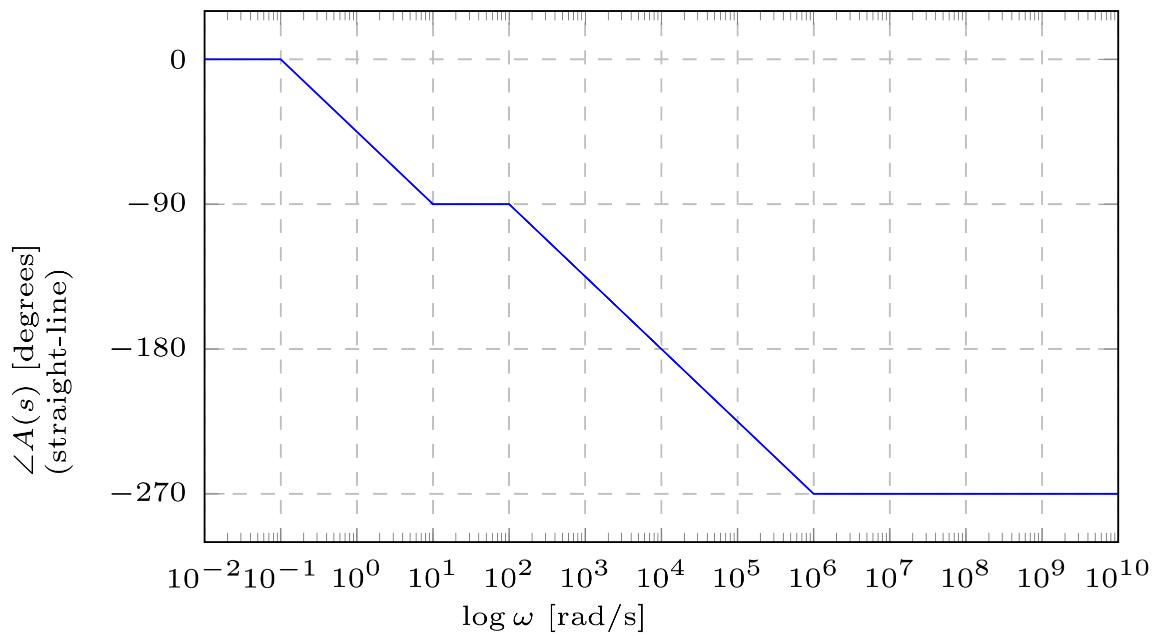
[2] (c) What is the value of v_i when the output just reaches V_{max}?

Solution

Outside the dead-band region, v_o is given by the equation
$v_o = (v_i - V_x{}')k'$ where $V_x{}'$ is the new dead-band region and k' is the closed-loop gain
Setting v_o equal to $V_{max} = 4.5\,\mathrm{V}$ and solving for v_i, we have

$v_i = (V_{max}/k') + V_x{}' = ((4.5)/(0.878)) + (81.25e-3) = 5.206\,\mathrm{V}$

Q4. Assume an opamp is ideal with the transfer-function,
$A(s) = \frac{k_{dc}}{(1+s/\omega_{p1})(1+s/\omega_{p2})(1+s/\omega_{p3})}$
The straight-line Bode phase plot for the amplifier is shown below and the dc gain is given by $k_{dc} = 1.5e3$
Assume the poles are widely spaced apart.



[2] (a) Find the values for ω_{p1}, ω_{p2}, and ω_{p3} in rad/s

Solution

The pole frequencies can be found by looking at the straight-line Bode phase plot.
Assuming the poles are widely spaced apart,
the phase at where the poles occur are at $-45°$, $-135°$, $-225°$
Therefore, the pole locations are

$\omega_{p1} = 1\,\text{rad/s}$

$\omega_{p2} = 1\,\text{krad/s}$

$\omega_{p3} = 100\,\text{krad/s}$

[4] (b) Ignoring the effect of the highest frequency pole, if this amplifier is used in a non-inverting configuration, what is the smallest dc closed-loop amplifier gain that will result in a phase margin of 65 °? (use the actual $A(s)$ and NOT the straight-line Bode plot).

Solution

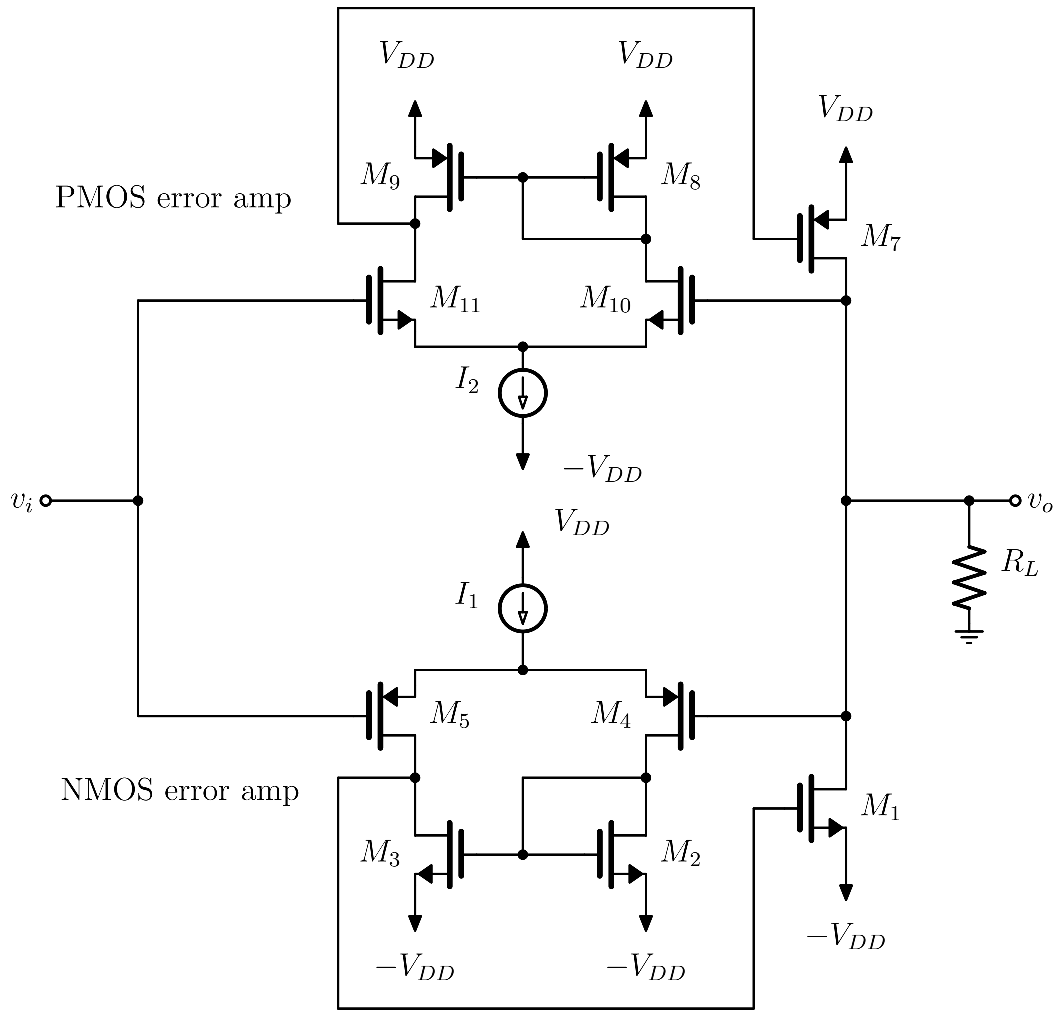
The loop gain is $A(s)\beta$ resulting in $L(s) = A(s)\beta = \frac{k_{dc}\beta}{(1+s/\omega_{p1})(1+s/\omega_{p2})}$
(ω_{p3} is ignored so it is set to ∞ in $A(s)$)
$\angle L(j\omega) = -\,\text{atan}(\omega/\omega_{p1}) - \text{atan}(\omega/\omega_{p2})$
$PM = \angle L(j\omega_1) - (-180°)$ where ω_1 is defined as $|L(j\omega_1)| = 1$
We know that for $\text{PM} = 65\,°$, the unity gain freq ω_1 will have the relationship $\omega_{p1} \ll \omega_1 < \omega_{p2}$
so reconizing that $\omega_1/\omega_{p1} \gg 1$, we can make the approximation
$\text{atan}(\omega_1/\omega_{p1}) \approx 90°$ leading to
$PM = 90° - \text{atan}(\omega_1/\omega_{p2}) = 65\,°$
$\omega_1 = \omega_{p2} * \tan(((90 - \text{PM})/180) * \pi) = (1e3) * \tan(((90 - (65))/180) * (3.142)) = 466.3\,\text{rad/s}$

and we now find β by making use of $|L(j\omega_1)| = 1$
$\beta = (\omega_1/\omega_{p1}) * (\sqrt{1 + (\omega_1/\omega_{p2})^2})/k_{dc} = ((466.3)/(1)) * (\sqrt{1 + ((466.3)/(1e3))^2})/(1.5e3) = 0.343$
The closed-loop gain, A_{cl} is given by $A_{cl} = A_0/(1 + A_0\beta)$ where $A_0 = k_{dc}$ resulting in the min A_{cl} given by

$A_{cl} = k_{dc}/(1 + k_{dc} * \beta) = (1.5e3)/(1 + (1.5e3) * (0.343)) = 2.91\,\text{V/V}$

(we could also have used $A_{cl} \approx 1/\beta$ since $k_{dc}\beta \gg 1$)
The minimum closed-loop gain that results in $\mathrm{PM} = 65\,^\circ$ is $A_{cl} = 2.91\,\mathrm{V/V}$

Q5. Consider the CMOS push-pull output stage shown below. The size for the NMOS output transistor has $W_1 = 90\,\mu\mathrm{m}$ and $L_1 = 90\,\mathrm{nm}$ while the PMOS output transistor has $W_7 = 180\,\mu\mathrm{m}$ and $L_7 = 105\,\mathrm{nm}$. It is desired that $I_Q = 800\,\mu\mathrm{A}$ while $I_1 = I_2 = 66.67\,\mu\mathrm{A}$.



[3] (a) Find the width and length for M_2, M_3, M_8, M_9 so that the desired currents are obtained.

Solution

M_2 and M_3 are matched and M_8 and M_9 are matched so we just need the sizes of M_2 and M_8.
The length of M_2 should match the length of M_1 so $L_2 = L_1 = (90e-9) = 90\,\mathrm{nm}$
We also have a current mirror between M_2 and M_1 when $v_o = 0$ given by
$I_Q = I_{D1} = (W_1/W_2) * (I_1/2)$ resulting in

$W_2 = ((I_1/2)/I_Q) * W_1 = (((66.67e-6)/2)/(800e-6)) * (90e-6) = 3.75\,\mu\mathrm{m}$

The length of M_8 should match the length of M_7 so $L_8 = L_7 = (105e-9) = 105\,\mathrm{nm}$
We also have a current mirror between M_8 and M_7 when $v_o = 0$ given by
$I_Q = I_{D7} = (W_7/W_8) * (I_2/2)$ resulting in

$W_8 = ((I_2/2)/I_Q) * W_7 = (((66.67e-6)/2)/(800e-6)) * (180e-6) = 7.5\,\mu\mathrm{m}$

[3] (b) When simulating this power amp, it is found that the gain of the NMOS error amp is too large and should be reduced to improve the stability of the circuit. What changes can be made to the circuit to reduce the error amp gain by a factor of 2 while keeping I_Q unchanged?

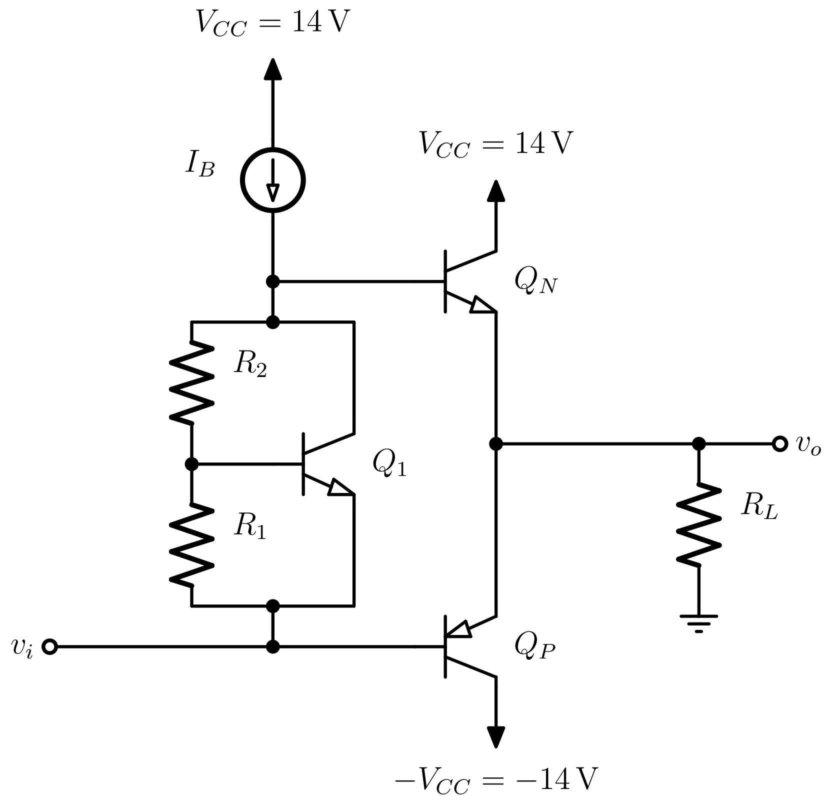
Solution

The gain of the error amp is $A_v = g_{m5} * (r_{o5}||r_{o3})$. To reduce the gain, we can either reduce g_{m5} or the output impedances. It is generally preferable to reduce g_m (as there are 2 output impedances involved and also, you would need either more current or a shorter length but the length of M_3 has to match the length of M_1).

To reduce g_{m5} by a factor of 2, you need to reduce the W_5 by a factor of 4 (due to the square root relationship assuming the current remains unchanged). Of course, W_4 would also be reduced by a factor of 4.

Reduce both W_4 and W_5 by a factor of 4

Q6. Consider a class AB BJT output stage as shown below with an output load, $R_L = 30\,\Omega$ and a maximum amplitude of $\pm 12\,\text{V}$ (limited by the input swing). The power transistors (Q_N and Q_P) both have $I_{S,pow} = 200\,\text{fA}$ and $\beta_{pow} = 50$ while the bias transistor (Q_1) has $I_S = 20\,\text{fA}$ and $\beta_1 = 180$. Assume $V_T = 25\,\text{mV}$



[2] (a) Assuming a quiescent current (in the power transistors) of 12 mA, find the 3 values of the input voltage corresponding to when the output is either -12 V, 0 V or 12 V.

Solution

Define $\alpha_{pow} = \beta_{pow}/(\beta_{pow} + 1) = (50)/((50) + 1) = 0.9804$

Define $I_{S\alpha,pow} = I_{S,pow}/\alpha_{pow} = 204\,\text{fA}$

The quadratic equation for class-AB BJT amplifiers is ...

$i_n^2 - i_L i_n - I_Q^2 = 0$

When $i_L = 0$, $i_n = I_Q$
When $i_L \gg I_Q$, we can ignore the I_Q^2 term leading to
$i_n \approx i_L$
In addition, we can find the pnp emitter current from
$i_p = I_Q^2/i_n$ which is found from the equation $i_n i_p = I_Q^2$

To find the input voltage, we make use of
$v_o = v_i + V_{EB,P}$ leading to $v_i = v_o - V_{EB,P}$
We need to find the 3 values of $V_{EB,P}$ which are found from the i_p values using...
$V_{EB,p} = V_T * \ln(i_p/(I_{S\alpha}))$

$v_o = 0\,\mathrm{V}$:
$i_L = 0$ leading to $i_p = I_Q = (12e-3) = 12\,\mathrm{mA}$
$V_{EB,p} = V_T * \log(i_p/I_{S\alpha,pow}) = (25e-3) * \log((12e-3)/(204e-15)) = 0.6199\,\mathrm{V}$
$v_i = v_o - V_{EB,p} = (0) - (0.6199) = -0.6199\,\mathrm{V}$

$v_o = 12\,\mathrm{V}$:
$i_L = v_o/R_L = (12)/(30) = 0.4\,\mathrm{A}$ leading to $i_n \approx i_L = 0.4\,\mathrm{A}$
$i_p = I_Q^2/i_n = (12e-3)^2/(0.4) = 360\,\mu\mathrm{A}$
$V_{EB,p} = V_T * \log(i_p/I_{S\alpha,pow}) = (25e-3) * \log((360e-6)/(204e-15)) = 0.5323\,\mathrm{V}$
$v_i = v_o - V_{EB,p} = (12) - (0.5323) = 11.47\,\mathrm{V}$

$v_o = -12\,\mathrm{V}$:
$i_L = v_o/R_L = (-12)/(30) = -0.4\,\mathrm{A}$ leading to $i_p \approx -i_L = 0.4\,\mathrm{A}$ (by symmetry)
$V_{EB,p} = V_T * \log(i_p/I_{S\alpha,pow}) = (25e-3) * \log((0.4)/(204e-15)) = 0.7076\,\mathrm{V}$
$v_i = v_o - V_{EB,p} = (-12) - (0.7076) = -12.71\,\mathrm{V}$

[4] (b) Design the bias circuit for a quiescent current (in the power transistors) of 12 mA and a minimum current of 1.2 mA through the Vbe multiplier circuit.

Solution

Define $V_{o,max} = 12\,\mathrm{V}$ as the maximum peak output voltage
Define $I_{min} = 1.2\,\mathrm{mA}$ as the min current through Vbe multiplier
I_B is sized by choosing I_B to be $I_{min} + I_{Bn,max}$ where $I_{Bn,max}$ is the largest current into the base of Q_N.
$I_{Bn,max} = (V_{o,max}/R_L) * (1/(\beta_{pow}+1)) = ((12)/(30)) * (1/((50)+1)) = 7.843\,\mathrm{mA}$
$I_B = I_{min} + I_{Bn,max} = (1.2e-3) + (7.843e-3) = 9.043\,\mathrm{mA}$
When I_{min} is going to the Vbe multiplier, we choose to let half flow through R_2 and half flow through I_{C1} of Q_1 (this is a reasonable design choice).
As more current flows into the Vbd multiplier, I_{C1} will absorb most of the extra current
So $I_R = I_{min}/2 = (1.2e-3)/2 = 600\,\mu\mathrm{A}$

We have from part(a) that for $v_o = 0$, and $I_Q = 12\,\mathrm{mA}$ then $V_{EB,p} = 0.6199\,\mathrm{V}$
and due to matching, $V_{BE,n} = V_{EB,p} = 0.6199\,\mathrm{V}$ leading to
$V_{BB} = V_{BE,n} + V_{EB,p} = (0.6199) + (0.6199) = 1.24\,\mathrm{V}$

Define $\alpha_1 = \beta_1/(\beta_1+1) = (180)/((180)+1) = 0.9945$
Define $I_{S\alpha,1} = I_S/\alpha_1 = 20.11\,\mathrm{fA}$
(since β_1 is so large, we could have ignored the effect of α_1 here)

At $v_o = 0$, $i_n = I_Q$ resulting in Q_N base current given by
$I_{Bn,Q} = I_Q/(\beta_{pow} + 1) = (12e - 3)/((50) + 1) = 235.3\,\mu\text{A}$
$I_{C1} = I_B - I_R - I_{Bn,Q} = (9.043e - 3) - (600e - 6) - (235.3e - 6) = 8.208\,\text{mA}$
$V_{be1} = V_T * \log(I_{C1}/I_{S\alpha,1}) = (25e - 3) * \log((8.208e - 3)/(20.11e - 15)) = 0.6684\,\text{V}$
$R_1 = V_{be1}/I_R = (0.6684)/(600e - 6) = 1.114\,\text{k}\Omega$ (Assuming $I_{B1} \approx 0$)
$V_{BB} = V_{be1} + (V_{be1}/R_1) * R_2 = V_{be1} * (1 + R_2/R_1)$
$R_2 = ((V_{BB}/V_{be1}) - 1) * R_1 = (((1.24)/(0.6684)) - 1) * (1.114e3) = 952.5\,\Omega$
$R_1 = 1.114\,\text{k}\Omega$; $R_2 = 952.5\,\Omega$

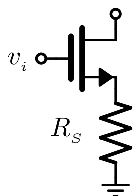
Equation Sheet

Constants: $k = 1.38 \times 10^{-23}\,\mathrm{J\,K^{-1}}$; $q = 1.602 \times 10^{-19}\,\mathrm{C}$; $V_T = kT/q \approx 26\mathrm{mV}$ at $300\,\mathrm{K}$; $\epsilon_0 = 8.85 \times 10^{-12}\,\mathrm{F\,m^{-1}}$; $k_{ox} = 3.9$; $C_{ox} = (k_{ox}\epsilon_0)/t_{ox}$; $\omega = 2\pi f$

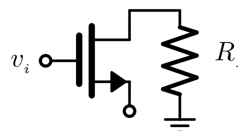
NMOS: $k_n = \mu_n C_{ox}(W/L)$; $V_{tn} > 0$; $v_{DS} \geq 0$; $V_{ov} = V_{GS} - V_{tn}$
(triode) $v_{DS} \leq V_{ov}$; $v_D < v_G - V_{tn}$; $i_D = k_n(V_{ov}v_{DS} - (v_{DS}^2/2))$
(active) $v_{DS} \geq V_{ov}$; $i_D = 0.5k_nV_{ov}^2(1 + \lambda v_{DS})$; $g_m = k_nV_{ov} = 2I_D/V_{ov} = \sqrt{2k_nI_D}$; $r_s = 1/g_m$; $r_o = L/(|\lambda'|I_D)$

PMOS: $k_p = \mu_p C_{ox}(W/L)$; $V_{tp} < 0$; $v_{SD} \geq 0$; $V_{ov} = V_{SG} - |V_{tp}|$
(triode) $v_{SD} \leq V_{ov}$; $v_D > v_G + |V_{tp}|$; $i_D = k_p(V_{ov}v_{SD} - (v_{SD}^2/2))$
(active) $v_{SD} \geq V_{ov}$; $i_D = 0.5k_pV_{ov}^2(1 + |\lambda| v_{SD})$; $g_m = k_pV_{ov} = 2I_D/V_{ov} = \sqrt{2k_pI_D}$; $r_s = 1/g_m$; $r_o = L/(|\lambda'|I_D)$

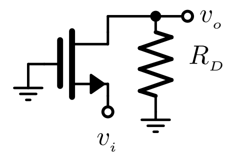
BJT: (active) $i_C = I_Se^{(v_{BE}/V_T)}(1 + (v_{CE}/V_A))$; $g_m = \alpha/r_e = I_C/V_T$; $r_e = V_T/I_E$; $r_\pi = \beta/g_m$; $r_o = |V_A|/I_C$; $i_C = \beta i_B$; $i_E = (\beta+1)i_B$; $\alpha = \beta/(\beta+1)$; $i_C = \alpha i_E$; $R_b = (\beta+1)(r_e + R_E)$; $R_e = (R_B + r_\pi)/(\beta+1)$



$i_{sc} \approx -(1/g_m + R_S)^{-1}v_i$
$R_x \approx (1 + g_mR_S)r_o$
Approx due to $g_mr_o \gg 1$



$v_{oc} \approx v_i$
$R_x \approx 1/g_m + R_D/(g_mr_o)$



$v_o/v_i \approx g_m(r_o||R_D)$

Diff Pair: $A_d = g_mR_D$; $A_{CM} = -(R_D/(2R_{SS}))(\Delta R_D/R_D)$; $A_{CM} = -(R_D/(2R_{SS}))(\Delta g_m/g_m)$; $V_{OS} = \Delta V_t$; $V_{OS} = (V_{OV}/2)(\Delta R_D/R_D)$; $V_{OS} = (V_{OV}/2)(\Delta(W/L)/(W/L))$
Large signal: $i_{D1} = (I/2) + (I/V_{ov})(v_{id}/2)(1 - (v_{id}/2V_{ov})^2)^{1/2}$

1st order: step response $y(t) = Y_\infty - (Y_\infty - Y_{0+})e^{-t/\tau}$;
unity gain freq for $T(s) = A_M/(1 + (s/\omega_{3dB}))$ for $A_M \gg 1 \Rightarrow \omega_t \simeq |A_M|\omega_{3dB}$

Freq: for real axis poles/zeros $T(s) = k_{dc}\dfrac{(1 + s/z_1)(1 + s/z_2)\ldots(1 + s/z_m)}{(1 + s/\omega_1)(1 + s/\omega_2)\ldots(1 + s/\omega_n)}$
OTC estimate $\omega_H \simeq 1/(\sum\tau_i)$; dominant pole estimate $\omega_H \simeq 1/(\tau_{max})$
STC estimate $\omega_L \simeq \sum 1/\tau_i$; dominant pole estimate $\omega_L \simeq 1/(\tau_{min})$

Miller: $Z_1 = Z/(1 - K)$; $Z_2 = Z/(1 - 1/K)$

Mos caps: $C_{gs} = (2/3)WLC_{ox} + WL_{ov}C_{ox}$; $C_{gd} = WL_{ov}C_{ox}$; $C_{db} = C_{db0}/\sqrt{1 + V_{db}/V_0}$;
$\omega_t = g_m/(C_{gs} + C_{gd})$; for $C_{gs} \gg C_{gd} \Rightarrow f_t \simeq (3\mu V_{ov})/(4\pi L^2)$

Feedback: $A_f = A/(1 + A\beta)$; $x_i = (1/(1 + A\beta))x_s$; $dA_f/A_f = (1/(1 + A\beta))dA/A$; $\omega_{Hf} = \omega_H(1 + A\beta)$; $\omega_{Lf} = \omega_L/(1 + A\beta)$;
Loop Gain $L \equiv -s_r/s_t$; $A_f = A_\infty(L/(1 + L)) + d/(1 + L)$; $Z_{port} = Z_{p^o}((1 + L_S)/(1 + L_O))$: $PM = \angle L(j\omega_t) + 180$; $GM = -|L(j\omega_{180})|_{db}$;
Pole splitting $\omega'_{p1} \simeq 1/(g_mR_2C_fR_1)$; $\omega'_{p2} \simeq (g_mC_f)/(C_1C_2 + C_f(C_1 + C_2))$

Pole Pair: $s^2 + (\omega_o/Q)s + \omega_o^2$; $Q \leq 0.5 \Rightarrow$ real poles; $Q > 1/\sqrt{2} \Rightarrow$ freq resp peaking

Power Amps: Class A : $\eta = (1/4)(\hat{V}_O/IR_L)(\hat{V}_O/V_{CC})$; Class B : $\eta = (\pi/4)(\hat{V}_O/V_{CC})$; $P_{DN\_max} = V_{CC}^2/(\pi^2R_L)$;
Class AB : $i_ni_p = I_Q^2$; $I_Q = (I_S/\alpha)e^{V_{BB}/(2V_T)}$; $i_n^2 - i_Li_n - I_Q^2 = 0$

2-stage opamp: $\omega_{p1} \simeq (R_1G_{m2}R_2C_c)^{-1}$; $\omega_{p2} = G_{m2}/C_2$; $\omega_z = (C_c(1/G_{m2} - R))^{-1}$;
$SR = I/C_c = \omega_tV_{ov1}$; will not SR limit if $\omega_t\hat{V}_O < SR$