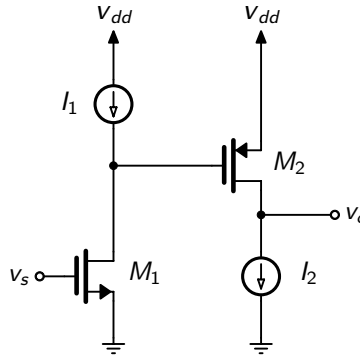**Problem Set 3 - Cascode**

**Question 1**

Given a two-stage common-source amplifier where the biasing current sources $I_1$ and $I_2$ have output resistances equal to those of $M_1$ and $M_2$ respectively, determine an expression for the voltage gain, $v_o/v_s$, in terms of $g_{m1}$, $g_{m2}$, $r_{o1}$ and $r_{o2}$.



# Solution

Looking at the first stage, and defining $v_1$ to be the small signal voltage at the drain of $M_1$, we have an output impedance at $v_1$ given by

$$r_{out1} = r_{o1} || r_{I1} = r_{o1}/2$$

since it was given that the output impedance of $I_1$ is equal to $r_{o1}$.

As a result, we get a voltage transfer function of:

$$v_1/v_s = -g_{m1}r_{out1} = -g_{m1}r_{o1}/2$$

Looking at the second stage, we get a voltage transfer function of:

$$v_o/v_1 = -g_{m2}r_{out2} = -g_{m2}r_{o2}/2$$

As such, the total transfer function is:

$$v_o/v_s = (v_1/v_s)(v_o/v_1) = (g_{m1}g_{m2}r_{o1}r_{o2})/4$$

$$v_o/v_s = (g_{m1}g_{m2}r_{o1}r_{o2})/4$$

**Question 2**

Given transistor $M_1$ which has $\mu_n C_{ox} = 240\mu A/V^2$, $\lambda'_n = 50nm/V$, $V_t = 0.5V$, $W = 1\mu m$, and $L = 200nm$:

a) Ignoring any DC current in $R_2$ and assuming $r_o \to \infty$, determine $V_{GS}$.

b) Determine the DC current in $R_2$, determine $V_{DS}$, and justify your neglection of the DC current when calculating $V_{GS}$ in part a).

c) Determine the small-signal voltage gain $v_o/v_{in}$. (Assume an ideal current source)

d) Assuming the negative swing of the output limits the overall output swing, what is the min output voltage, max output voltage and output peak-to-peak swing?

e) What is the corresponding input amplitude, max and min voltages at the gate?
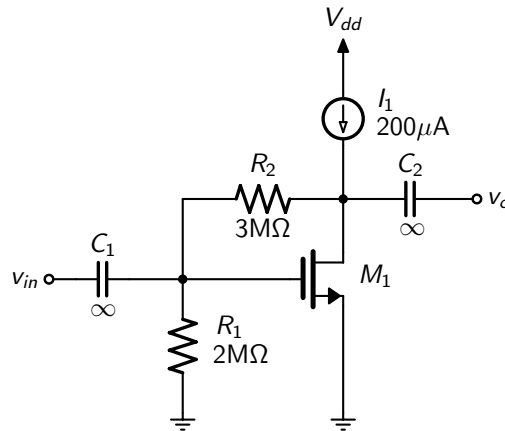


## Solution

a) Assuming all the current goes through the channel and none goes into $R_2$ since it is so large:

$$I_D = 0.5\mu_n C_{ox}(W/L)V_{ov}^2$$

$$V_{ov} = sqrt(2*I_D/(\mu_n C_{ox}*(W/L))) = sqrt(2*(200e-6)/((240e-6)*((1e-6)/(200e-9)))) = 0.5774V$$

$$V_{GS} = V_{ov} + V_t = (0.5774) + (0.5) = 1.077V$$

b) Rearranging the voltage division rule: $V_{GS} = V_{DS} * R_1/(R_1 + R_2)$

$$V_{DS} = V_{GS} + R_2 * V_{GS}/R_1 = (1.077) + (3e6)*(1.077)/(2e6) = 2.693V$$
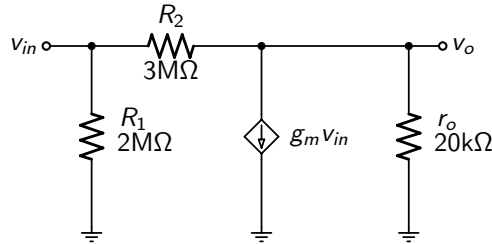
$$V_{DS} = 2.693V$$

As such, the current in $R_2$ is:

$$I_{FB} = V_{DS}/(R_1 + R_2) = (2.693)/((2e6) + (3e6)) = 538.7nA$$

This is quite small compared to $I_{D1}$ so ignoring this current in part (a) is justified.

c) First, $g_m$ and $r_o$ are calculated:

$$g_m = 2 * I_D/(V_{GS} - V_t) = 2 * (200e-6)/((1.077) - (0.5)) = 692.8\mu A/V$$

$$r_o = L/(\lambda_n' * I_D) = (200e-9)/((50e-9) * (200e-6)) = 20k\Omega$$



Second, using KCL:

$$((v_o - v_{in})/R_2) + (g_m v_{in}) + (v_o/r_o) = 0$$

$$v_o/v_{in} = (1/R_2 - g_m)/(1/R_2 + 1/r_o) = (1/(3e6) - (692.8e-6))/(1/(3e6) + 1/(20e3)) = -13.76V/V$$

$$\boxed{v_o/v_{in} = -13.76V/V}$$

d) For $M_1$ to remain in the active region, we require that $V_{DS} \geq V_{ov}$. We can also write this condition as

$$V_D - V_S \geq V_G - V_S - V_t$$

or equivalently

$$V_D \geq V_G - V_t$$

In other words, the drain voltage must stay higher than the gate voltage minus the threshold voltage for the device to remain in the active region.

Now let us write $V_{G1}$ as $V_G + \Delta V_G$ and $V_{D1}$ as $V_D + \Delta V_D$

where $V_G$ and $V_D$ are the bias voltages for the gate and drain respectively

So we have the requirement

$V_D + \Delta V_D \geq V_G + \Delta V_G - V_t$

Now, define $A_v \equiv v_o/v_{in}$ and from small-signal analysis, $A_v \equiv \Delta V_D/\Delta V_G$ or $\Delta V_G = \Delta V_D/A_v$.

Putting this into the above equation, we have

$V_D + \Delta V_D \geq V_G + (\Delta V_D/A_v) - V_t$

and setting it to equality to find the max $\Delta V_D$ (which is the min $V_{D1}$), we have

$\Delta V_D(1 - 1/A_v) = V_G - V_t - V_D$

From this, we can solve for $\Delta V_D$

$$\Delta V_D = (V_G - V_t - V_D)/(1 - (1/A_v)) = ((1.077) - (0.5) - (2.693))/(1 - (1/(-13.76))) = -1.973$$

This gives the max output peak-to-peak output swing of

$$V_{o,pp} = 2 * |\Delta V_D| = 2 * |(-1.973)| = 3.945V$$

$$V_{o,min} = V_D + \Delta V_D = (2.693) + (-1.973) = 0.7207V$$

$$V_{o,max} = V_D - \Delta V_D = (2.693) - (-1.973) = 4.666V$$

e) The maximum input swing at the gate is related by:

$$V_{G,pp} = V_{o,pp}/|A_v| = (3.945)/|(-13.76)| = 0.2868V$$

Since the input voltage, $V_G$ is set to a dc bias of $V_{GS} = 1.077V$, the min/max values at the gate are

$$V_{G,min} = V_{GS} - V_{G,pp}/2 = (1.077) - (0.2868)/2 = 0.934V$$

$$V_{G,max} = V_{GS} + V_{G,pp}/2 = (1.077) + (0.2868)/2 = 1.221V$$

## Question 3

In a MOS cascode amplifier, the cascode transistor is required to raise the output resistance by a factor of 40 over that of a non-cascode amplifier. If the transistor is operated at $V_{ov} = 0.2V$, what must its $\lambda_n$ be? If the process technology specifies $\lambda'_n$ as 50nm/V, what channel length must the transistor have?

## Solution

Let $K \equiv 40$

A cascode current source increases the output resistance by a factor of $g_{m2}r_{o2}$ compared to a non-cascode current source. And since $g_m = 2I_D/V_{ov}$ and $r_o = L/(\lambda'_n I_D)$ we have

$$K = g_{m2}r_{o2} = \frac{2L}{\lambda'_n V_{ov}}$$

so

$$\lambda_n = \lambda'_n/L = 2/(KV_{ov})$$

$$\lambda_n = 2/(K * V_{ov}) = 2/((40) * (0.2)) = 0.25V^{-1}$$

and if $\lambda'_n = 50nm/V$, then

$$L = \lambda'_n/\lambda_n = (50nm/V)/(0.25V^{-1}) = 200nm$$

## Question 4

Design the cascode amplifier shown below to obtain $g_{m1} = 1mA/V$ and $R_o = 400k\Omega$. Use a $0.18 - \mu m$ technology for which $V_{tn} = 0.5V$, $\lambda'_n = 200nm/V$ and $\mu_n C_{ox} = 400\mu A/V^2$. Determine $L$, $W/L$, $V_{G1}$, $V_{G2}$, and $I$. Use identical transistors operated at $V_{ov} = 0.2V$, and design for the maximum possible negative signal swing at the output. What is the value of the minimum permitted output voltage?
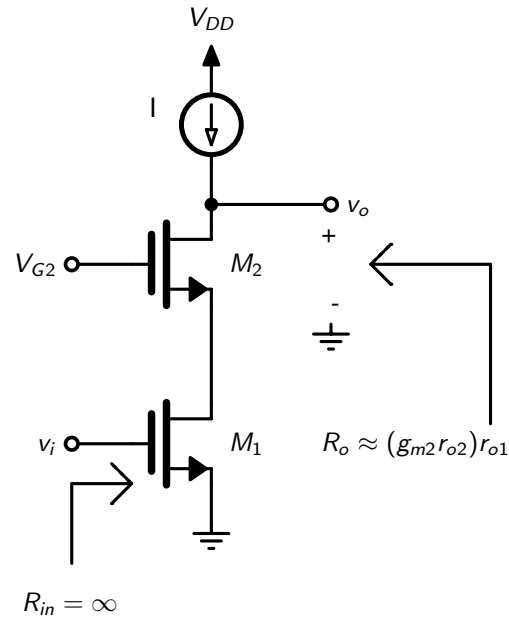
## Solution

$g_{m1} = \frac{2I_D}{V_{ov}}$, so,

$$I = I_D = g_{m1} * V_{ov}/2 = (1e-3)*(0.2)/2 = 100\mu A$$

$$R_o = (g_{m2}r_{o2})r_{o1}$$

However, if we make $g_{m2} = g_{m1} = g_m$ and $r_{o1} = r_{o2} = r_o$, we can say that:

$$r_o = sqrt(R_o/g_{m1}) = sqrt((400e3)/(1e-3)) = 20k\Omega$$

Since $r_o = \frac{L}{\lambda_n' I_D}$, we have

$$L = \lambda_n' * I_D * r_o = (200e-9)*(100e-6)*(20e3) = 400nm$$

$g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$ so that

$$W/L = g_m^2/(2*\mu_n C_{ox} * I_D) = (1e-3)^2/(2*(400e-6)*(100e-6)) = 12.5$$

$$W/L = 12.5$$

Since $V_{ov} = 0.2V$ for both transistors, we have

$$V_{G1} = V_{ov} + V_{tn} = (0.2) + (0.5) = 0.7V$$

For $V_{G2}$, we want to bias it such that the drain of $M_1$ is high enough such that $M_1$ remains in the active region which is a value of $V_{ov} = 0.2V$. As a result, we set $V_{G2}$ to

$$V_{G2} = V_{ov} + V_{tn} + V_{ov} = (0.2) + (0.5) + (0.2) = 0.9V$$

As a result, the minimum output voltage will be

$$V_{o,min} = 2 * V_{ov} = 2 * (0.2) = 0.4V$$

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### Question 5

Design the circuit shown below to provide an output of $I_D = 100\mu A$. Use $V_{DD} = 3.3V$, and assume the PMOS transistors to have $\mu_p C_{ox} = 60\mu A/V^2$, $V_{tp} = -0.8V$, $L = 250nm$, and $\lambda'_p = -50nm/V$. The current source is to have the widest possible signal swing at its output. Design for $V_{ov} = 0.2V$, and specify the width, $W$, of the transistors and of $V_{G3}$ and $V_{G4}$. What is the highest allowable voltage at the output? What is the value of output impedance, $R_o$?



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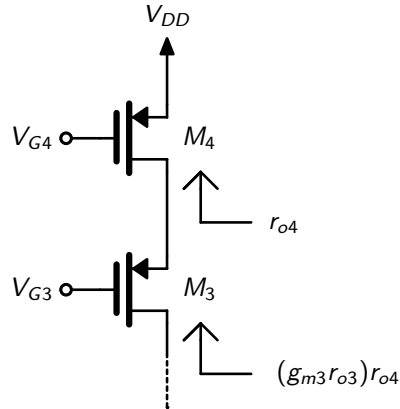
## Solution

$$I_{D3} = I_{D4} = I_D = 0.5\mu_p C_{ox}(W/L)V_{ov}^2$$

$$W = (2 * I_D * L)/(\mu_p C_{ox} * V_{ov}^2) = (2 * (100e-6) * (250e-9))/((60e-6) * (0.2)^2) = 20.83\mu m$$

For $V_{G4}$, we can write

$$V_{SG4} = V_{ov} + |V_{tp}| = (0.2) + |(-0.8)| = 1V$$

$$V_{G4} = V_{DD} - V_{SG4} = (3.3) - (1) = 2.3V$$

For $V_{G3}$ and maximum swing, we want to set the bias voltage of the drain of $M_4$ to be at the edge of the active region, so

$$V_{SD4} = V_{ov} = (0.2) = 0.2V$$

$$V_{D4} = V_{DD} - V_{SD4} = (3.3) - (0.2) = 3.1V$$

$$V_{SG3} = V_{ov} + |V_{tp}| = (0.2) + |(-0.8)| = 1V$$

$$V_{G3} = V_{D4} - V_{SG3} = (3.1) - (1) = 2.1V$$

The highest allowable maximum voltage to keep $M_3$ in the active region is

$$V_{o,max} = V_{DD} - 2 * V_{ov} = (3.3) - 2 * (0.2) = 2.9V$$

To find $R_o$, we have

$$r_{o3} = L/(|\lambda'_p| * I_D) = (250e-9)/(|(-50e-9)| * (100e-6)) = 50k\Omega$$

$$r_{o4} = L/(|\lambda'_p| * I_D) = (250e-9)/(|(-50e-9)| * (100e-6)) = 50k\Omega$$

$$g_{m3} = (2 * I_D)/V_{ov} = (2 * (100e-6))/(0.2) = 1e-3$$

$$R_o = g_{m3} * r_{o3} * r_{o4} = (1e-3) * (50e3) * (50e3) = 2.5M\Omega$$

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### Question 6

For $V_{DD} = 1.8V$ and using $I_{ref} = 100\mu A$, it is required to design the circuit below to obtain an output current whose nominal value is $I_{ref} = 100\mu A$.

a) Find R if $M_1$ and $M_2$ are matched with channel lengths of $L = 500nm$, channel widths of $W = 4\mu m$, $V_{tn} = 0.5V$, and $\mu_n C_{ox} = 400\mu A/V^2$.

b) What is the lowest possible value for $V_o$?

c) Assuming that for this process technology $\lambda'_n = 50nm/V$, find the output resistance of the current source.

d) Find the current change in output current resulting from a +0.5V change in $V_o$



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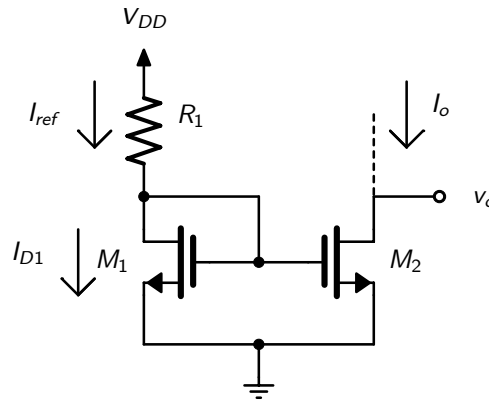
## Solution

a)

$$I_o = I_{D1} = I_{ref}$$

$$I_{D1} = 0.5\mu_n C_{ox}(W/L)V_{ov}^2$$

$$V_{ov} = sqrt((2 * I_{D1})/(\mu_n C_{ox} * (W/L))) = 0.25V$$

$$V_{DS1} = V_{GS1} = V_{ov} + V_{tn} = (0.25) + (0.5) = 0.75V$$

$$R = (V_{DD} - V_{GS1})/I_{ref} = ((1.8) - (0.75))/(100e-6) = 10.5k\Omega$$

b) The lowest $V_o$ will be when

$$V_{o,min} = V_{ov} = 0.25V$$

c) The output resistance is $r_o 3$

$$r_{o3} = L/(\lambda'_n * I_o) = (500e-9)/((50e-9) * (100e-6)) = 100k\Omega$$

d)

$$\Delta I_D = \Delta V_o / r_{o3} = (0.5)/(100e3) = 5\mu A$$