General approach to implementing analogue Viterbi decoders

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Indexing terms: Viterbi decoding, Magnetic recording

Commercial realisations of analogue Viterbi decoders are available for magnetic read channels. However, these implementations are restricted to a particular coding scheme. The authors present a general approach to the implementation of analogue Viterbi decoders having arbitrary coding schemes. The proposed method exploits the ability of simple analogue circuits to perform the required mathematical functions. Simulation results are presented for a 0.8μm BiCMOS process.

Introduction: The Viterbi algorithm is an iterative method for estimating the state sequence of a discrete-time finite-state Markov process contaminated by memory-less noise [1]. In the field of digital communications, optimum decoding of convolutional codes and maximum-likelihood sequence estimation in the presence of intersymbol interference are generally considered to be the most important uses of this algorithm.

Although Viterbi detectors have traditionally been realised using digital circuitry together with A/D converters, analogue implementations have been reported in an effort to increase the speed and reduce the power consumption due to power-hungry flash A/D converters [2, 3]. However, integrated analogue Viterbi decoders reported so far have been restricted to partial-response class-IV signalling (also called PR4) mainly because a PR4 decoder can be partitioned into two time-interleaved dicode decoders having simple analogue realisations [2, 4]. The purpose of this correspondence is to extend the idea of analogue Viterbi decoders to more complicated partial-response signalling (PRS) schemes (for example those in [5]).

Although realising higher density magnetic recording systems is the main motivation for this work, other applications can be considered as well. The quaternary-PR4 signalling proposed for high-speed data transmission over unshielded twisted-pair cables [6] is an example in which the present implementation for decoding a multilevel signal without a significant increase in complexity seems promising

Finally, the approach presented here is not restricted to level-coding schemes and can also be used in convolutional coding systems.

Proposed implementation: To exploit the redundancy introduced by coding, an optimum detector determines the most-likely transmitted sequence having the minimum distance from the received signal as compared to all other possibly-transmitted sequences. In the case of additive Gaussian white noise, the criterion is based on minimising the squared-Euclidean distance.

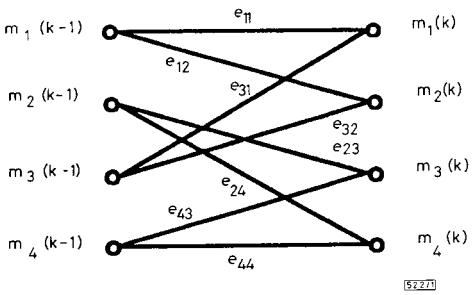

Fig. 1 *Trellis diagram for N = 4 and M = 2*

In an algorithmic realisation of maximum-likelihood sequence detection, the metric assigned to each state of the trellis is updated using the previous state metrics and the branch metrics. Each branch in the trellis corresponds to a transition between two states with its metric representing the distance of the received symbol from the signal resulting in that transition. The update mechanism takes place such that the accumulative error (distance) of the estimated sequence for each state is minimised. In a trellis with N states, there are M transitions initiating from or ending at each state where M is the size of the alphabet and N is a power of M [Note 1]. For example, Fig. 1 shows the trellis diagram for $N = 4$ and $M = 2$.

Mathematically, the Viterbi decoder performs the following state-metric updates:

$$m_i(k) = \max_j \{m_j(k-1) - e_{ji}(k)\} \qquad (1)$$

$$i = 1, 2, ..., N \quad j = 1, 2, ..., M$$

Here, $m_j(k)$ is the state metric of the ith state at time k and $e_{ji}(k)$ is the branch metric (error signal) of the branch connecting state j at time k–1 to state i at time k. Although the branch metrics are of quadratic forms, they can be reduced to linear forms by dropping the common quadratic terms.

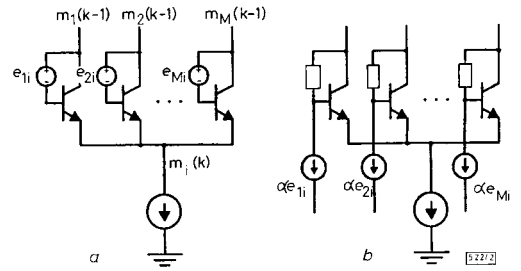

Fig. 2 *ACS function employing the generalised differential stage*

a Realisation of ACS
b Circuit implementation

From eqn. 1, it can be seen that the mathematics involved in a Viterbi decoder is of the form of add-compare-select (ACS). The circuit approach presented here is based on introducing a generalised differential stage and utilising its capability in performing the ACS operation by means of simple resistive feedbacks fed by error current signals. Fig. 2 shows the circuit. The key feature of using this configuration is that in addition to comparing the signals, the maximum signal (with a v_{BE} drop) will appear on the common emitter node, performing the combination of compare and select functions. In Fig. 2*a* the previous state metrics, $m_j(k-1)$, are low-impedance nodes while e_{ji} are floating voltage sources which are proportional to branch metrics. These voltage sources are realised by resistors and controlled current sources as illustrated in Fig. 2*b*. Having this configuration for each state, the new state metrics are now calculated and are ready to be fed back for the next iteration. The ability of this simple stage to perform the relatively complex ACS function should be appreciated when other reported analogue realisations or the equivalent digital counterpart are considered.

To avoid any destructive effects on the stored metrics when feeding the new metrics back, the use of sample-and-holds (S/Hs) is necessary. Although master-slave S/Hs can be used, ping-pong S/Hs are recommended which have the potential of doubling the speed. The latter point is of particular importance as the speed of operation is mainly limited by the S/Hs.

As seen from eqn. 1, the Viterbi algorithm inherently has the problem of state-metric unbounded growth. Subtracting the minimum metric from all of the state metrics either after a certain number of iterations or before the saturation occurs demands a tradeoff between extra computations and the dynamic range required in internal calculations. Specifically, to minimise the required dynamic range, this subtraction should be performed at the end of each time step. This optimum solution, usually not suitable in the digital domain, is easily applied in our analogue implementation by employing a fast continuous common-mode feedback (CMFB) circuit to maintain a constant common-mode voltage.

Interconnected voltage-to-current converters are used to produce the required error currents, αe_{ji}. The equations for these metrics depend on the coding scheme, and are usually of the form of

Note 1: Although only regular trellises fall into this category, the idea can be easily extended to irregular trellises as well.

linear combinations of two or more signals. One possible circuit realisation uses degenerated differential pairs to convert the input voltages to currents. The advantage of this approach is that it accepts differential voltages and generates differential currents which can then be easily combined to create the required combinations. Extra DC current sources optionally connected to the current summing nodes can control the DC components of the error currents. This reduces the operating-voltage requirement by decreasing the direct-voltage drops across the feedback resistors in Fig. 2*b*.

To obtain the comparison results from the decoder, mirror transistors are employed to replicate the currents of the differential cell transistors. These output currents are used to update the path memory.

Finally, it should be mentioned here that although BJTs have been used in this circuit description, to reduce the cost, a full CMOS realisation is also possible by careful circuit design.

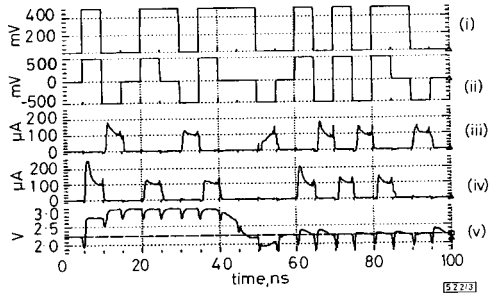

Fig. 3 *Typical dicode-Viterbi decoder waveforms, based on SPICE simulation*

(i) Original data
(ii) Encoded data
(iii) Output current I
(iv) Output current II
(v) Common-mode voltage

– – – – reference level

Simulation results: Using 0.8μm BiCMOS process parameters, a simple two-state dicode Viterbi detector was designed and simulated. Although this special case can be efficiently decoded through a simplified algorithm [4], the approach introduced in this Letter was followed to prove the concept. Ping-pong S/Hs with source-follower buffers were employed, and the CMFB circuit was operating on the DC-level shiftings introduced by these buffers. Low-impedance nodes, described in Fig. 2*a*, were provided by emitter followers. Degenerated differential pairs were used to produce the error current signals. Fig. 3 shows the SPICE-simulation results. The original as well as the encoded data are shown along with the mirrored currents of the differential cell transistors as the comparison results. It can easily be verified that ideal versions of these signals result by applying the nodal equations to the encoded signal. The memory management of the decoder is beyond the scope of this Letter and can be shown to translate the comparison results to the original uncoded data. Also shown in Fig. 3 is the common-mode voltage of the state metrics which settles to the desired value as soon as the start-up transition has been completed.

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Comment

Low-voltage CMOS transductance cell based on parallel operation of triode and saturation transconductors

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Introduction: Recently a new linearity improvement technique for low voltage CMOS transconductors was proposed [1]. The technique is based on the parallel operation of a triode and saturation transconductor. According to the simple square-law MOST model extended with the 'θ-model' for mobility reduction,

$$\mu = \frac{\mu_0}{1 + \theta(V_{GS} - V_T)} \qquad (1)$$

These transconductors have third order distortion terms with opposite sign, enabling third order nonlinearity cancellation. As analysed in [1], the cancellation occurs when the aspect ratios of the triode and saturation converter are chosen according to

$$\frac{(W/L)_{tri}}{(W/L)_{sat}} \simeq \frac{1}{2 \cdot \theta \cdot V_{DS}} \qquad (2)$$

The proposed linearisation technique was evaluated using PSPICE simulations and it was found that a *THD* of –87dB was possible at 800mV peak-to-peak input voltage for a supply voltage as low as 1.5V. In this Letter we want to comment on the significance of these simulation results. Two aspects are discussed: first the model used for distortion prediction and secondly the effect of device mismatch. Measurement results will be presented which indicate that the third order distortion terms of a saturation and triode converter do not have an opposite sign for a low supply voltage as predicted by simulations. As a result the newly proposed linearisation technique will most probably not work in that case. Furthermore inevitable device mismatch easily introduces non-negligible second order distortion which limits the achievable *THD*.

Comment on model used for distortion prediction: In [1], the distortion of a circuit embodying the newly proposed linearisation technique was evaluated by means of PSPICE simulations. Because θ values are mentioned in [1], presumably the level 3 model [2] was used, which uses eqn. 1 for mobility reduction modelling (level 4 BSIM [3] mobility modelling is similar though uses different nomenclature). The third order distortion that is found in this way is mainly determined by the third order derivative d^3I_D/dV_{GS}^3 of the level 3 MOS transistor model (at constant V_{DS} and V_{SB}). As discussed in [4], CAD models sometimes even fail to predict the first order derivative of the current of an MOS transistor with adequate accuracy, therefore placing distortion simulations that rely on higher order derivatives under great suspicion. This is especially true for low distortion levels and for circuits in which a nonlinearity cancellation occurs. In the latter case the final result even depends on the difference of the value of the third order