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2V fully-differential SC integrator in standard CMOS

S. Crapanzano and D.A. Johns

Indexing terms: Integrated circuits, Switched current circuits, Integrating circuits, VLSI

A 2V fully-differential SC integrator is developed for a standard double-poly CMOS without the need for clock or supply-voltage multiplication. The common mode at the integrator output is set to maximise the signal swing, and the common mode at the input to the OTA is set at the negative rail, maximising the overdrive on all the switches. Two capacitive common-mode adjustment networks are required to alleviate large leakage currents associated with parasitic junction diodes. A novel CMFB technique is proposed. Simulation results are presented for a 1.2μm CMOS process.

Background and introduction: Recently, work has been directed towards the development of a low-voltage SC integrator in standard-CMOS without the use of clock or supply-voltage multiplication [1, 2]. Crols *et al.* have shown that a single-ended switched-opamp can successfully eliminate problematic switches at 1.5V supply [2]. Baschirotto *et al.* have proposed a fully differential low-voltage SC integrator with optimal swing and maximum overdrive on all MOS switches [1], thereby possibly achieving lower-voltage operation and/or larger swing. This Letter proposes an addition to the SC integrator schematic in [1]. In addition, a novel CMFB technique is proposed. Finally, transistor level simulations are shown to corroborate the feasibility of the integrator schematic.

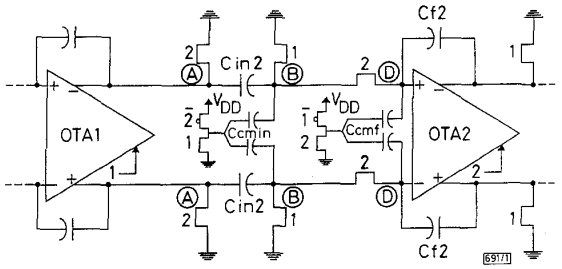

Fig. 1 *Proposed Low-voltage fully-differential SC integrator*

Proposed addition to SC integrator: Fig. 1, shows the outputs of OTA1 driving the proposed SC integrator, as well as two switches at the outputs of OTA2 that are part of the next integrator's input sampling network. This integrator contains an additional capacitive common-mode adjustment network (CCAN), C_{cmf}, connected directly at OTA2's inputs (see Fig. 1). During phase 1, the common mode at nodes A/A' is set to 1.0V for optimal swing [1]. During phase 2 the switches at A/A' initiate charge transfer to OTA2 and also pull the outputs of OTA1 down to GND. Capacitors C_{cmin} are switched to V_{dd} during 2, ensuring the common mode at nodes B/B', D/D' settles to GND [1]. Note that without C_{cmin} the common mode would likely hit –1V at nodes B/B', thus forward-biasing the MOS parasitic junction diodes there and removing differential charges from C_{in2}. Transistor level simulations indicate that the integrator does not function unless the additional CCAN C_{cmf} is added.

As shown in Fig. 1, two switches are connected at OTA2's outputs whose function is identical to those at the output of OTA1. It can be shown that during the off-state of OTA2, a differential and common mode change occurs at the inputs of OTA2 due to the pull-down switches connected at its outputs. For example, during the on-state of OTA2, the positive, negative outputs of the integrator can have values of 0, 2V. Then due to the pull-down switches the positive and negative inputs of OTA2 would likely go to –2V and 0, i.e. a common-mode change of –1V, and a differential voltage of 2V should be stored at the OTA2's inputs. These values could never occur in practical realisations because the MOS switch at OTA2's positive input would turn on. Also, and most importantly, the MOSFET parasitic junction diodes present at the input of the switched-OTA (SWOTA) would become forward-biased and leak. These forward-biased diodes result in large charge leakage from the feedback caps of OTA2. Thus preservation of differential charges would not occur.

The additional common-mode capacitive adjustment network (CCAN), C_{cmf}, connected directly at SWOTA2's inputs, alleviates the above leakage problems (see Fig. 1). C_{cmf} would normally be set to C_{f2}. When OTA2 is switched off, one end of C_{cmf} is switched to 2V. By superposition, the common-mode voltage at the input to OTA2 settles to 0.5V. Furthermore, due to the capacitive divider seen by the differential output of OTA2, a maximum of 1V differential signal is now stored at OTA2's inputs. Thus, neither of OTA2's input nodes will settle below GND. When the output swing of the OTA is not rail-to-rail, smaller values for the C_{cmf} capacitors can be used. Also note that during the charge-transfer phase of the SC integrator, the C_{cmf} network is switched back to 0V, and the input common-mode of the OTA settles back to 0V.

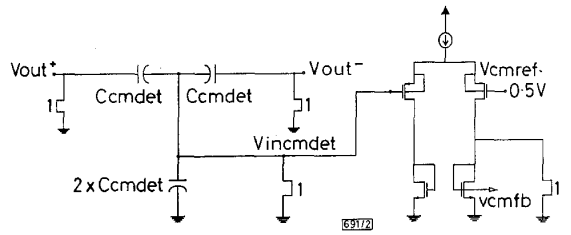

Fig. 2 *Proposed CMFB technique*

Proposed CMFB technique: Fig. 2 presents a novel CMFB technique. The two switches at the outputs of an OTA (V_{out}^+, V_{out}^-) are also connected to the two common-mode detector capacitors C_{cmdet}. Two additional switches are also necessary. The additional current switch at node V_{cmfb} is required to shut off the output stage current sources of OTA [3]. The pull-down switch at the $V_{incmdet}$ node is required to reset the CMFB loop. The CMFB error amplifier (CMFBEA) is comprised of a PMOS input differential pair and diode loads, and is very similar to one described in [4]. However, instead of an output common-mode reference voltage at V_{dd}/2, i.e. 1.0V, it is set at 0.5V for high-speed operation of the CMFBEA at 2.0V. An additional common-mode detector capacitor $2 \times C_{cmdet}$ is also used in Fig. 2. Thus a capacitive voltage divider of 1/2 exists between the two OTA outputs and the V_{cmdet} node. During phase 1, nodes V_{out}^+, V_{out}^- and V_{cmdet} are reset to 0V. During phase 2, all the switches are off, and the CMFB loop and the OTA are reactivated. Since the $V_{incmdet}$ node is forced close to 0.5V by the negative feedback in the CMFB loop, the two outputs will thus be forced to ~1.0V common mode. Note that to help ensure that the speed of common-mode resettling is faster than the differential resettling the tail current source of the CMFBEA is not deactivated.

Simulation results: A single-stage folded-cascode OTA was designed, and tested with >80dB gain at 2V supply [3] and was used in the simulations of the switched-OTA. Its swing is $2.4V_{pp}$

differential, and all transistors are operated in the strong-inversion saturation region. The choice of a folded-cascode input stage facilitates high-speed operation with an input common mode near the negative rail [5]. The reduction in the supply voltage was limited by ensuring proper operation of the bias circuit, the OTA, and the

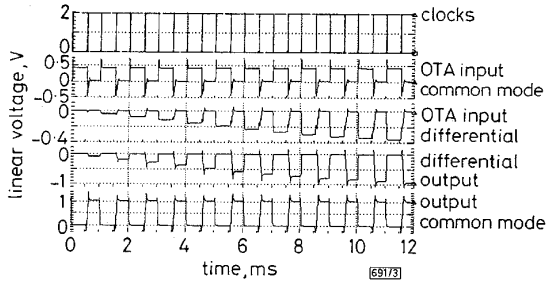

Fig. 3 *Integrator transistor level simulations*

CMFBEA under V_t process variations. Simulation results are illustrated in Fig. 3, where an integrator gain of 1 was used. An arbitrary 100mV input is placed at the input to the integrator containing OTA2 in Fig. 2. Fig. 3 indicates that the output common-mode voltage settles to within 50mV of 1.0V. Charge injection from the switches has a slight effect on the accuracy of the final common mode. The input common mode of the OTA stays at 0V during the charge-transfer phase 2, and is increased to 400mV during the charge-storage phase 1. This slight error is due to the parasitic capacitance at the OTA's input, and to any additional common-mode charges injected at the OTA's input due to the finite difference in time to shut off the NMOS, PMOS output stage currents sources of the OTA [2]. However, this slight error is not a problem because the swing for the OTAs is about 1.2V single-ended, and thus the input OTA nodes are still prevented from settling below GND.

Conclusions: In this Letter we have shown that a fully differential SC integrator is possible at the transistor level with a supply voltage of 2 V. No clock or supply voltage multiplication was necessary in a standard CMOS process [5, 6]. An additional common-mode adjustment network was required in the SC integrator to reduce large leakage charges due to parasitic junction diodes at the input to the OTA. Transistor-level simulations were used to support this work. Further work can be directed towards a lower-voltage fully differential OTA in standard CMOS [7], and the implementation of a fully differential prototype [2]. Additional work is also necessary to improve the leakage of charges due to the transients during the charge-transfer phase and the charge-storage phase.

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All-digital multipoint adaptive delay compensation circuit for low skew clock distribution

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Indexing terms: Clocks, Integrated circuits

The authors describe an all-digital circuit for automatically controlling skew in the distribution of a clock or data signal over a single line. The circuit derives a compensating delay for any location such that a signal applied at one end emerges at the same global time at all sites. This is an alternative to delay-equalised hierarchical trees for use in large ICs, computers, and digital switches. A 3μm CMOS prototype at eight sites spread over 16m shows adaptive skew control to within +/– 1.5 primitive buffer delays of the process employed. A novel technique for accommodating metastability is involved in the design.

Background: Recently, a scheme for non-hierarchical multipoint skew cancellation was patented using a PLL that locks onto the mid-time of the intervals between pulses which travel down and back on a reference line [1, 2]. Here, we are interested in exploiting the same multipoint interval halving principle in an all-digital form suitable for CMOS processes without linear circuits and VCOs. Fig. 1 shows the system architecture and internal structure of the clock alignment IC (CAIC) that has been developed. The reference line (RL) and reference pulse injector (RPI) are the same as in [1, 2] but a raw clock line (RCL) is added to remove the need for a VCO: instead of PLL-controlling a VCO clock-phase, the raw clock signal at each point is adaptively phase-shifted to align systemwide under control of fully digital pulse interval-halving (PIH) and clock aligner (CA) subcircuits. The Anceau method [3] has some similarity to this scheme but synchronises free-running modules only during communications times on a shared bus whose rate is lower than the internal clock speed of the module. Here we achieve truly synchronous full-speed clocking of all system modules where a CAIC is present.

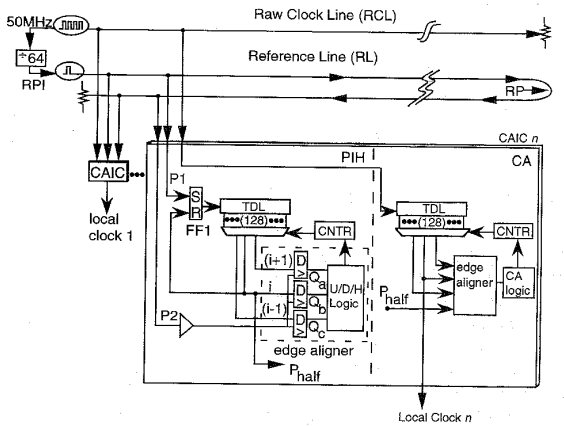

Fig. 1 *System architecture and internal structure of clock aligner IC*