Time-Interleaved Oversampling A/D Converters: Theory and Practice

Ramin Khoini-Poorfard, *Member, IEEE,* Lysander B. Lim, *Member, IEEE,* and David A. Johns, *Senior Member, IEEE*

***Abstract*— In this paper, the design procedure and practical issues regarding the realization of time-interleaved oversampling converters are presented. Using the concept of block digital filtering, it is shown that arbitrary $\Delta\Sigma$ topologies can be converted into corresponding time-interleaved structures. Practical issues such as finite opamp gain, mismatching, and dc offsets are addressed, analyzed, and practical solutions to overcome some of these problems are discussed. To verify the theoretical results, a discrete-component prototype of a second-order time-interleaved $\Delta\Sigma$ analog/digital (A/D) converter has been implemented and the design details as well as experimental results are presented.**

***Index Terms*—Converters, time-interleaved, oversampling.**

I. Introduction

OVERSAMPLING converters have become a popular technique for data conversion [1]. One reason for their popularity is their outstanding linearity which comes from the fact that they usually exploit a 1-b quantizer. Even with a trilevel quantizer, linearity performance up to 20 b has recently been reported [2].

However, there is a price to be paid to achieve this degree of linearity. Due to the nature of oversampling, these converters are much slower than their Nyquist-rate counterparts. For instance, the input bandwidth of the aforementioned 20-b converter is only 400 Hz whereas the sampling rate is 200 kHz. Hence, the application of $\Delta\Sigma$ modulators are usually restricted to low-speed high-linearity applications such as digital audio. Emerging applications have forced designers to seek highly linear converters with broader input bandwidths. One approach is through the use of higher order modulators and lower oversampling ratios. The disadvantage of this approach is that the anti-aliasing filter for the A/D converter (smoothing filter for the D/A converter) becomes more complicated and hence, it diminishes a key feature of oversampling converters—the simplicity of their anti-aliasing filters (smoothing filter for the D/A converter). Similarly, the complexity of the decimation filter (interpolation filter for the D/A) increases with the order of the modulator.

Recently, several authors have utilized the concept of multirate signal processing. In one approach, quadrature-matched-filtering is used with a bank of independent A/D converters to reduce in-band harmonics [3]. In another approach, a Hadamard transform is used to decompose the input spectrum into several subbands which are then applied to separate A/D converters whose outputs are recombined [4]. In this paper, an alternate approach is described which is also based on multirate signal processing concepts. By using M interconnected modulators working in parallel with each running at the same clock, the effective sampling rate becomes M times the clock rate of each modulator. In other words, one can achieve the required sampling rate not by performing more oversampling but by increasing the number of modulators. Hence, the required resolution is obtained without utilizing a faster and more costly fabrication process or using a higher order modulator. The key idea here is to make use of block digital filtering in which a single-input single-output transfer function is realized via an $M \times M$ transfer function matrix along with a commutator at both front and back ends. Using this concept and applying several topological transformations on a given $\Delta\Sigma$ modulator, one can derive the equivalent time-interleaved by M structure which is capable of operating at effectively M times the speed of the given $\Delta\Sigma$ modulator.

The outline of this paper is as follows. In Section II, the concept of block digital filtering is reviewed and a systematic approach is introduced to derive the time-interleaved equivalent structure for an arbitrary $\Delta\Sigma$ converter. The practical issues regarding implementation of these modulators are addressed in Section III. Specifically, the problems of leaky integrators, dc offset, and component mismatch are considered in detail and practical solutions are presented. Section IV deals with an experimental second-order time-interleaved A/D prototype. The design procedure as well as experimental results are discussed thoroughly. Finally, conclusions are given in Section V.

II. Time-Interleaved Modulator (TIM)

In this section, the basic concept of block digital filtering is introduced and is used to develop a technique for realizing time-interleaving converters [5]. A step by step procedure is provided showing how to derive the equivalent time-interleaved version of an arbitrary $\Delta\Sigma$ converter with an arbitrary interleaving number M.

A. Block Digital Filtering

A block digital filter is basically a multirate system in which parallelism is exploited to reduce the speed requirement on each processing element [6]. In this section, the basic concept of these filters are reviewed. Consider the single-input single-output transfer function $Y(z) = H(z)X(z)$. An equivalent

Manuscript received May 16, 1994; revised February 7, 1997. This paper was recommended by Associate Editor V. Gopinathan.

The authors are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ont., Canada M5S 1A4.

Publisher Item Identifier S 1057-7130(97)03649-5.

system with the same input–output transfer function is depicted in Fig. 1 in which $\overline{H}(z)$ is an $M \times M$ transfer function matrix shown in (1) at the bottom of the page, where $\overline{H}_{ij}$ represents the contribution of the jth input to the ith output. The general structure of $\overline{H}(z)$ is shown in (1). The elements of the first row of $\overline{H}(z)$ are type 1 poly-phase components of $H(z)$, or mathematically

$$H(z) = \sum_{l=0}^{M-1} z^{-1} E_l(z^M) \tag{2}$$

where

$$E_l(z) = \sum_{n=-\infty}^{\infty} e_l(n) z^{-n} \qquad 0 \le l \le M-1 \tag{3}$$

$$e_l(n) = h(nM + l) \qquad 0 \le l \le M-1. \tag{4}$$

In other words, $e_l(n)$ is merely the M-fold decimated version of $h(n+l)$. Note that in (1), each row is a circularly shifted version of the row above it except for the elements below the diagonal entries which are delayed as well. Matrices with such characteristics are called *pseudo-circulant*. For an arbitrary transfer function matrix $\overline{H}(z)$ in Fig. 1, $Y(e^{j\omega})$ not only consists of $X(e^{j\omega})$ but also includes its aliased versions, i.e., $X[e^{j(\omega+2k\pi/M)}]$'s. Generally speaking, the structure shown in Fig. 1 is a *linear time-varying* system. The necessary and sufficient condition for the block digital filter structure shown in Fig. 1 in order to represent a single-input single-output *linear time-invariant* (LTI) transfer function is that $\overline{H}(z)$ be pseudo-circulant. In other words, if the pseudo-circulant condition is satisfied then all aliased components ($X[e^{j(\omega+2k\pi/M)}]$'s) will be cancelled perfectly and $Y(e^{j\omega})$ consists of only $X(e^{j\omega})$, resulting in the block digital filter being an LTI system. In summary, an arbitrary transfer function $H(z)$ can be transformed into its corresponding pseudocirculant block digital transfer function matrix $\overline{H}(z)$, but not all $\overline{H}(z)$ can be converted back into an LTI transfer function. The following example clarifies how to derive $\overline{H}(z)$ from $H(z)$.

Example: Consider the following transfer function $H(z) = 1/(1-\sqrt{\alpha}z^{-1})$. To find its corresponding $\overline{H}(z)$ for $M=2$, one should first derive its polyphase decomposition elements.

$$\begin{aligned}\frac{1}{1-\sqrt{\alpha}z^{-1}} &= \frac{1+\sqrt{\alpha}z^{-1}}{1-\alpha z^{-2}} \\ &= \frac{1}{1-\alpha z^{-2}} + z^{-1} \times \frac{\sqrt{\alpha}}{1-\alpha z^{-2}} \\ &= E_0(z^2) + z^{-1}E_1(z^2).\end{aligned} \tag{5}$$

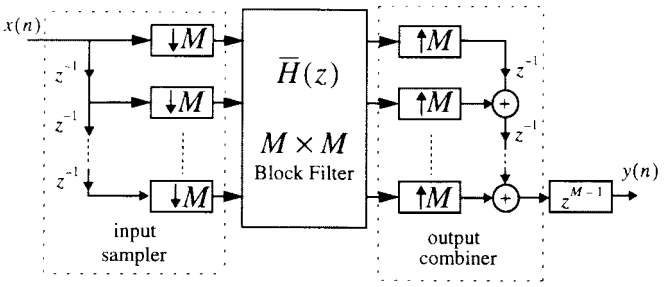


Fig. 1. Equivalent block filtering structure for the single-input single-output transfer-function $H(z)$.

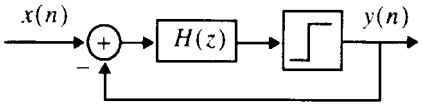


Fig. 2. Interpolative structure.

Hence, $E_0(z) = 1/(1-\alpha z^{-1})$ and $E_1(z) = \sqrt{\alpha}/(1-\alpha z^{-1})$. Therefore,

$$\overline{H}(z) = \begin{bmatrix} \dfrac{1}{1-\alpha z^{-1}} & \dfrac{\sqrt{\alpha}}{1-\alpha z^{-1}} \\ \dfrac{\sqrt{\alpha}z^{-1}}{1-\alpha z^{-1}} & \dfrac{1}{1-\alpha z^{-1}} \end{bmatrix}. \tag{6}$$

B. Derivation of the Structure

Consider the interpolative structure shown in Fig. 2 [7]. Although the interpolative structure does not cover all $\Delta\Sigma$ modulator architectures (such as double-loop or error-feedback topologies), the procedure presented here is general and the above structure is used as an example to clarify the steps involved.

The first step is to put the equivalent block digital filter $\overline{H}(z)$ shown in Fig. 1 in place of $H(z)$ in Fig. 2 resulting in Fig. 3. Note that the quantizer and z^{M-1} blocks have switched locations.

Studying Fig. 3 carefully, one realizes that rather than recombining o_j's into $o(n)$ and quantizing it to derive $y(n)$, one can alternatively quantize each of the o_j's and then recombine them to obtain $y(n)$. In this way, the quantizer block also enjoys the benefit of working at the lower rate. Based on this idea, Fig. 4 is derived where the z^{M-1} block has been transformed into two blocks to facilitate derivation of the remaining step.

The final step is to merge the input adder into the lower-rate section as well. The key point here is to note that $i_0 = u(Mn) - y_0$, $i_1 = u(Mn+1) - y_1$ and so on. In other words, each i_j consists only of its corresponding u and y terms. Hence, Fig. 4 can be modified into Fig. 5. Thus, assuming the

$$\overline{H}(z) = \begin{bmatrix} E_0(z) & E_1(z) & E_2(z) & \cdots & E_{M-1}(z) \\ z^{-1}E_{M-1}(z) & E_0(z) & E_1(z) & \cdots & E_{M-2}(z) \\ z^{-1}E_{M-2}(z) & z^{-1}E_{M-1}(z) & E_0(z) & \cdots & E_{M-3}(z) \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ z^{-1}E_1(z) & z^{-1}E_2(z) & z^{-1}E_3(z) & \cdots & E_0(z) \end{bmatrix}. \tag{1}$$

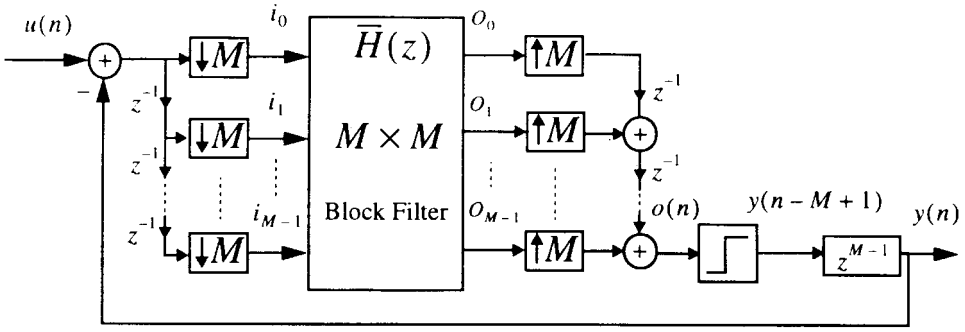


Fig. 3. Oversampling converter with a block digital filter.

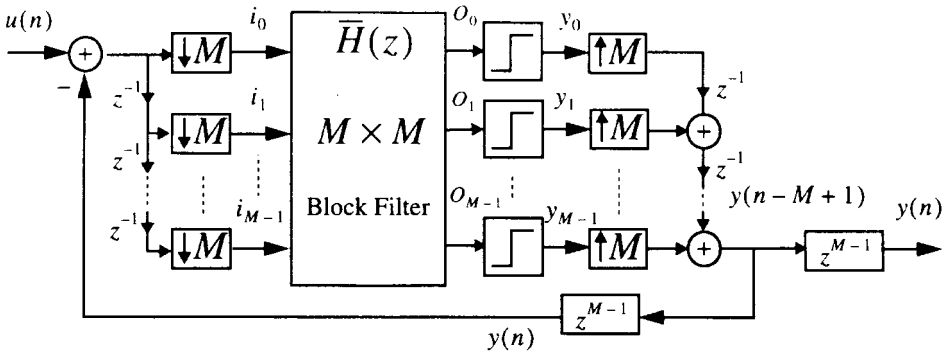


Fig. 4. Oversampling converter with block digital filter and quantizers at the lower-rate side.

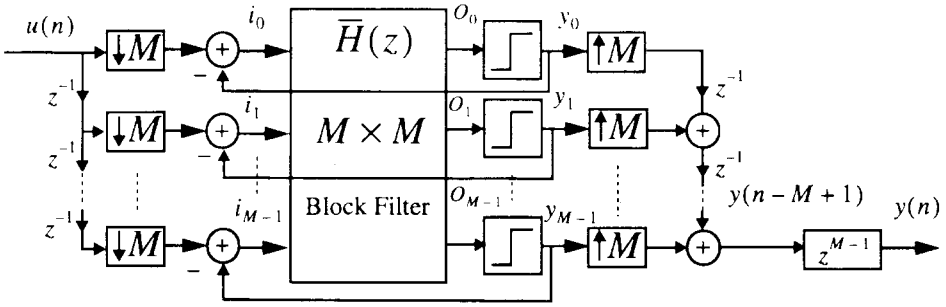


Fig. 5. TIM oversampling converter.

same initial conditions, Fig. 5 is equivalent to Fig. 2 from an input-output point of view.

Note that the noncausal component z^{M-1} can be disregarded and thus the final structure will have $M-1$ delays more than the structure illustrated in Fig. 2. Finally, as mentioned earlier, the aforementioned procedure is general and applicable to arbitrary $\Delta\Sigma$ architectures. In fact, a double-loop topology was chosen in the next section to illustrate the concept.

C. Simulations

Consider the second-order $\Delta\Sigma$ A/D converter, taken from [8], as shown in Fig. 6(a). The equivalent block digital filter for $H(z) = 0.5z^{-1}/(1 - z^{-1})$ assuming $M = 2$ is

$$\overline{H}(z) = \begin{bmatrix} z^{-1} & 1 \\ z^{-1} & z^{-1} \end{bmatrix} \times \frac{0.5}{1 - z^{-1}}. \tag{7}$$

Hence, the equivalent TIM structure for $M = 2$ can be derived based on a similar procedure as depicted in Fig. 6(b)–(e).

Based on this example, simulations were carried out to verify the theoretical results. Throughout these simulations, it is assumed that both structures in Fig. 6(a) and (e) are clocked at the same frequency (also referred to as internal clock frequency) except for the input sampler and output combiner in the TIM structure which are operated at twice the rate of the rest of the structure. The quantizer output levels are ± 3 and the input is a sinusoid with an amplitude of 0.5 and a frequency of 1 kHz. The internal clock frequency (f_s) is 100 kHz which leads to an effective clock rate ($f_{s,\text{eff}}$) of 200 kHz. The output spectrum of both structures is illustrated in Fig. 7. The spectrums were generated using the fast Fourier transform (FFT) algorithm. Specifically, the Welch method of power spectrum estimation [9] with 50% overlapping and Hanning windowing was used. The size of the periodogram for the conventional modulator was set at 32k while the time-interleaved modulator at 64k. Thus, the spectrums for the conventional modulator were obtained by averaging sixteen

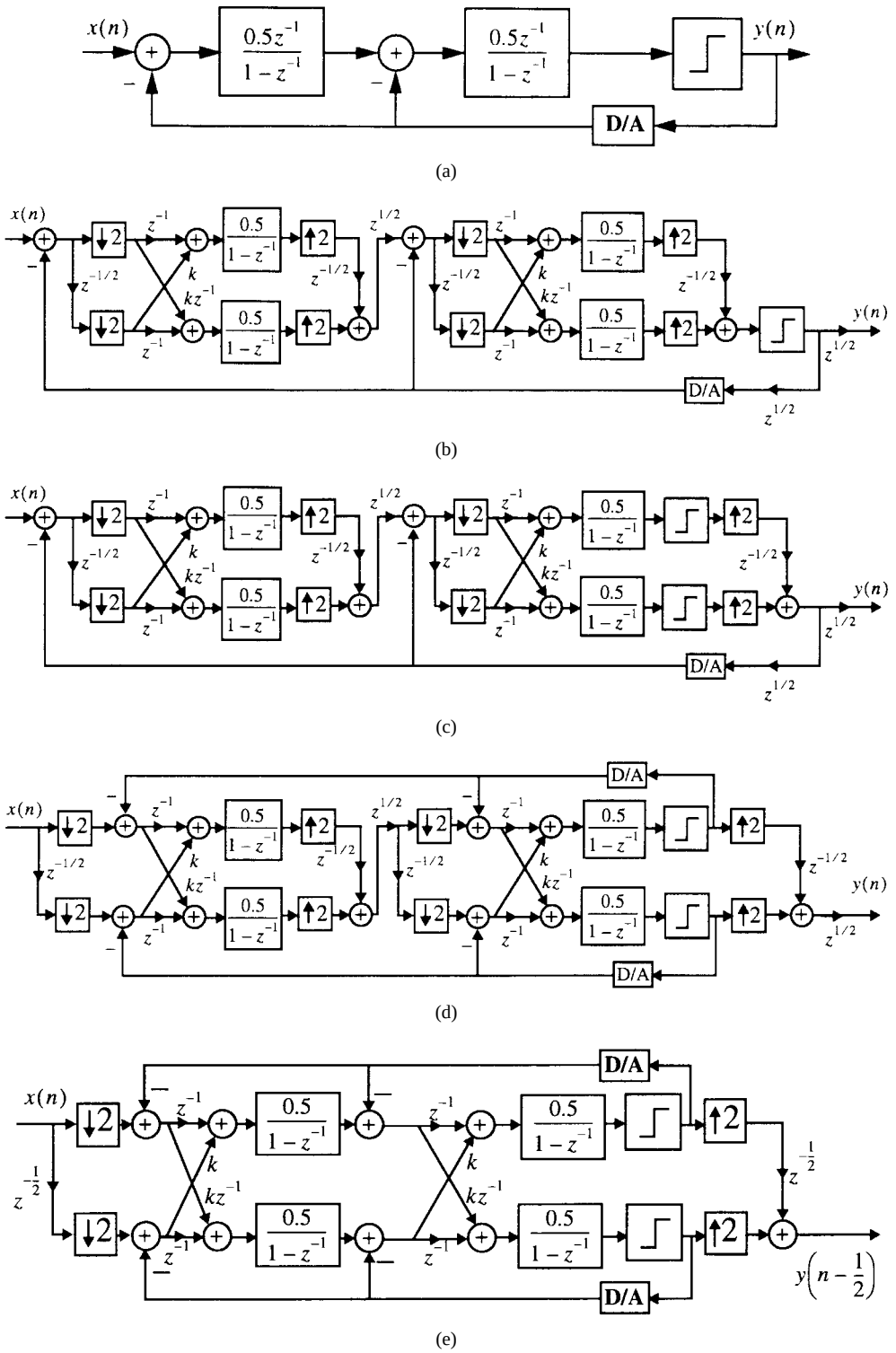


Fig. 6. Second-order $\Delta\Sigma$ modulator. (a) Conventional. (b) With block digital equivalent filters. (c) With quantizers in the lower-rate section. (d) With D/A's in the lower-rate section. (e) Final TIM structure. Note that $k = 1$.

32k-point FFT's whereas the TIM spectrums were averages of sixteen 64k-point FFT's. The difference in the size of the periodogram used to calculate the two types of spectrums was a result of the effective clock-rate of the TIM which was double that of the conventional modulator. In order to have the same resolution per bin in the frequency domain, the number of FFT points for the TIM must be double that of the conventional modulator.

To make the comparison of the two spectrums easier, it was decided to make them spurious free by adding the same amount of dithering to the 1-b quantizer inputs of both structures.

Simulation results reveal that the TIM structure has a 15 dB better signal-to-noise ratio (SNR) as predicted by theory. In other words, though both structures have the same internal clock frequency, the time-interleaved structure has an overall

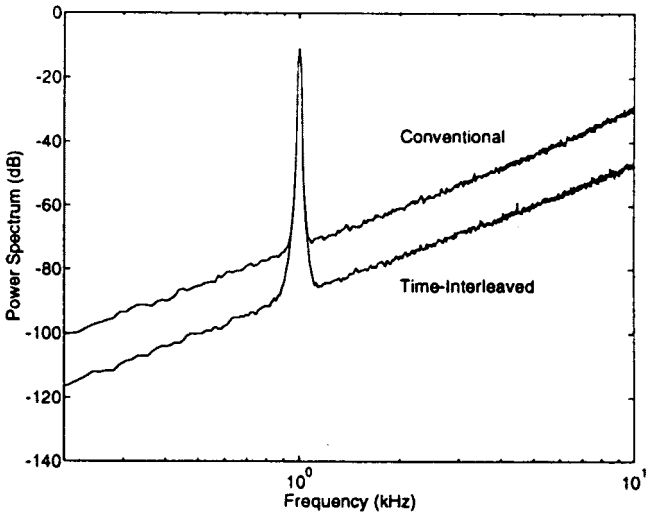


Fig. 7. Output spectrums of second-order conventional and time-interleaved structures being clocked at the same rate.

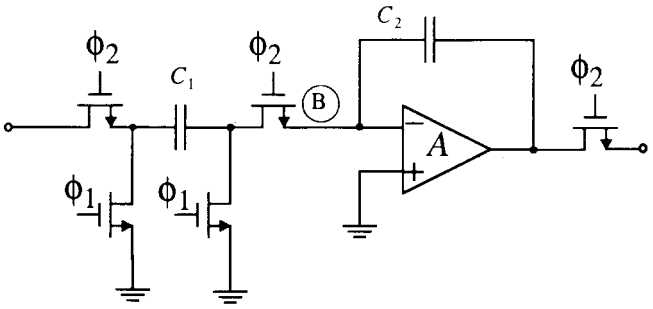


Fig. 8. Inverting nondelayed SC integrator.

performance equivalent to one octave higher oversampling ratio (OSR). In summary, the two modulators inside the TIM of Fig. 6(e) are equivalent to one modulator clocked at twice the rate.

III. Practical Issues

So far, a general procedure was presented to derive a TIM equivalent of an arbitrary $\Delta\Sigma$ structure. In this section, practical issues regarding circuit implementation of TIM architectures are discussed. Specifically, circuit nonidealities such as finite opamp gain, component mismatch, and dc offset are addressed and their effects on the overall performance are analyzed. Simulation results are given to verify theoretical discussions in all these cases. Also, an approach is proposed to simplify the implementation of the decimation stage.

A. Leaky Integrators

One of the major building blocks in switched-capacitor (SC) implementations of $\Delta\Sigma$ modulators are SC integrators. Fig. 8 illustrates an inverting nondelayed SC integrator whose transfer function is $(-C_1/C_2)/(1-z^{-1})$ assuming an ideal opamp. However, in practical realizations, the finite dc gain of the opamp violates the virtual ground concept at node B. Hence, not all of the charge of the input capacitor C_1 will be dumped onto the integrating capacitor C_2 resulting in a leaky integrator. It can be shown that the transfer function for this leaky integrator is as follows [10]:

$$H(z)=\frac{\dfrac{-C_1}{C_2\left[1+\dfrac{1}{A}+\dfrac{C_1}{C_2A}\right]}}{1-\dfrac{1+\dfrac{1}{A}}{1+\dfrac{1+\dfrac{C_1}{C_2}}{A}}z^{-1}}. \tag{8}$$

Assuming A is large and after some algebraic manipulations, (8) can be approximated by

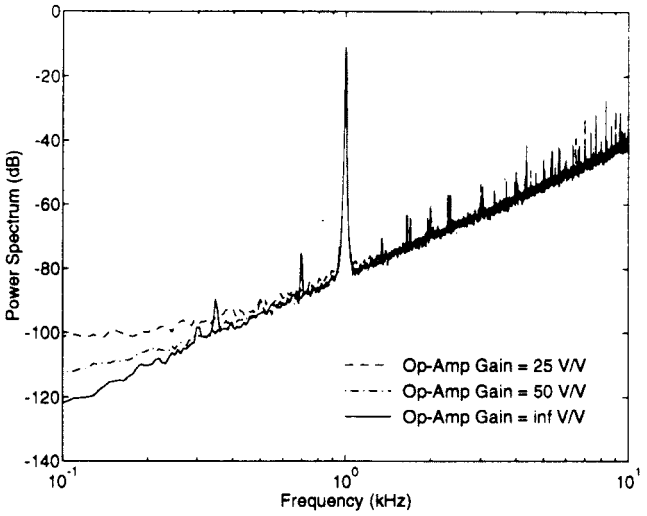
$$\begin{aligned}H(z)&\approx\frac{\dfrac{-C_1}{C_2\left[1+\dfrac{1}{A}+\dfrac{C_1}{C_2A}\right]}}{1-\left(1-\dfrac{C_1}{C_2A}\right)z^{-1}}\\&\equiv\frac{g}{1-\alpha z^{-1}}.\end{aligned} \tag{9}$$

The further away α is from unity, the more nonideal the integrator becomes. In the context of $\Delta\Sigma$ modulators, this nonideality reflects into a displacement of the noise transfer function zeros from their ideal locations and hence noise shaping is degraded. In [8], it was noted that for a second-order modulator, the minimum opamp gain (in V/V) before noise-shaping degradation is noticeable is around a value equal to the OSR. In [7], a fourth-order modulator was studied and according to simulation, a minimum gain of 200 V/V was required when using an OSR = 48. In summary, for $\Delta\Sigma$ structures, there is a critical opamp gain below which noise shaping deterioration becomes noticeable.

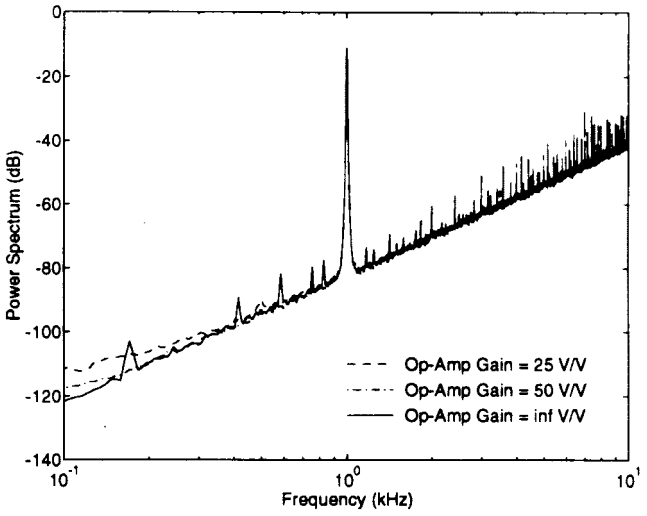
The above statement is also true for TIM structures. However, we show here that the critical opamp gain in a TIM structure is $1/M$ times that of a conventional modulator. In other words, the critical opamp gain can be M times smaller in a time-interleaved structure. To illustrate this result, consider the conventional and TIM structures shown in Fig. 6(a) and (e) and assume that both structures are built out of leaky integrators with transfer functions $1/(1-\alpha z^{-1})$. Based on (6), the equivalent $H(z)$ for the TIM structure is $1/(1-\sqrt{\alpha}z^{-1})$ whereas $H(z)$ for conventional modulator is $1/(1-\alpha z^{-1})$. Hence, α_{eff} is $\sqrt{\alpha}$ for TIM which is closer to unity resulting in a better overall performance. Also, recall that $\alpha=1-C_1/(C_2A)$ (9), hence

$$\begin{aligned}\alpha_{\text{eff}}&=\sqrt{\alpha}\\&=\sqrt{1-\frac{C_1}{C_2A}}\\&\approx 1-\frac{C_1}{2C_2A}\\&=1-\frac{C_1}{C_2A_{\text{eff}}}.\end{aligned} \tag{10}$$

Therefore, $A_{eff}=2A$. A similar argument is valid for the general case in which the equivalent single-input single-output transfer function would be $1/(1-\sqrt[M]{\alpha}z^{-1})$ resulting in $A_{\text{eff}}=MA$.



(a)



(b)

Fig. 9. Output spectrums for modulators with leaky integrators. (a) Conventional. (b) TIM.

To verify the results for $M = 2$, simulations were run for the second-order modulators introduced in Section II-C. The output spectrum for both modulators are illustrated in Fig. 9(a) and (b) for different opamp gains (C_1 is assumed to be equal to C_2). Here, TIM is clocked at half the rate of the conventional modulator so that the noise floors of both modulators are the same when using opamp gains of infinity. Note that the conventional modulator is sensitive to gain variation whereas TIM is more robust. Also, notice that around dc, the performance of TIM with opamp gain of 25 V/V is nearly the same as that of the conventional modulator with opamp gain of 50 V/V as predicted.

Before leaving this section, it should be noted that leaky integrators pose another problem as well. Specifically, they also cause the zeros of the NTF to move *inside* the unit circle and hence dead-band and limit-cycles are generated [11], [12]. Since a TIM structure has the benefit of having the NTF zeros closer to $z = 1$ for a given leaky integrator, it is also less prone to limit cycles. In summary, TIM's are less sensitive to leaky integrators and hence can use lower opamp gains as compared to conventional modulators.

B. DC Offsets

DC offsets of integrators do not typically pose any problem in conventional $\Delta\Sigma$ modulators since they only cause an offset-error in the overall dc characteristic function of the converter [1]. Also, the output of the integrators stay in the nonclipping range due to feedback. To clarify the latter point, consider the first-order conventional modulator illustrated in Fig. 10(a). Assuming a zero input signal [$x(n) = 0$] and a positive offset [$m(n) > 0$], the output of integrator $u(n)$, starts accumulating since $w(n) > 0$. Eventually, $y(n)$ becomes L and the negative feedback of the modulator forces the integrator output to go back down. Thus, the negative feedback of the modulator keeps the integrator output from saturating even in the presence of dc offsets.

The effect of offsets on a TIM structure is not quite the same. Consider the equivalent first-order TIM depicted in Fig. 10(b) and assume that the cross-coupling coefficients $k = 1$. Also assuming $x(n) = 0$, $m_1(n) > 0$, and $m_2(n) < 0$, we see that $u_1(n)$ starts increasing and $u_2(n)$ starts decreasing. Eventually, $y_1(n)$ and $y_2(n)$ will become L and $-L$, respectively. In contrast to the conventional modulator, $w_1(n)$ and $w_2(n)$ will not change signs since $y_2(n)$ cancels $y_1(n)$ in the top branch and visa versa in the bottom branch. Hence, $u_1(n)$ keeps increasing and $u_2(n)$ keeps decreasing, eventually causing the integrators to clip as well as the quantizers to overload thereby degrading noise-shaping performance. Even if both offsets have the same sign, this phenomena occurs except that the modulator with the larger offset will become unbounded whereas the other one stays bounded. The only situation where saturation would not occur would be if the offsets are precisely the same which is highly improbable.

Fortunately, if $k < 1$, then each branch has more control on its own feedback as compared to the cross-coupling branch. If $m_1(n)$ and $m_2(n)$ are small enough, the total feedback $L \times (1 - k)$ is capable of cancelling the effect of the offsets. In other words, if

$$\max\left(|m_i|\right)_{i=1,2} < L \times (1 - k) \tag{11}$$

then the effect of offsets is cancelled by negative feedback the same way as in a conventional $\Delta\Sigma$ modulator. Note that the deviation of k from unity does not cause aliasing since the pseudocirculant condition is still satisfied and hence the structure remains time-invariant. However, the poles and zeros of the STF and NTF are displaced. Performing linear analysis for Fig. 10(b), one can derive the following input–output relationship:

$$Y(z) = X(z)z^{-1}\,\frac{k + z^{-1}}{1 + kz^{-1}} + E(z)(1 - z^{-1})\,\frac{1 + z^{-1}}{1 + kz^{-1}}. \tag{12}$$

Note that the STF has a new pole-zero pair at $-k$ and $-(1/k)$, respectively, making it an all-pass function and hence, it won't cause amplitude distortion. Since the pole-zero pair is around $z = \pi$ and assuming a high OSR, the phase is quite linear in the band of interest which is around $z = 0$. Also note that

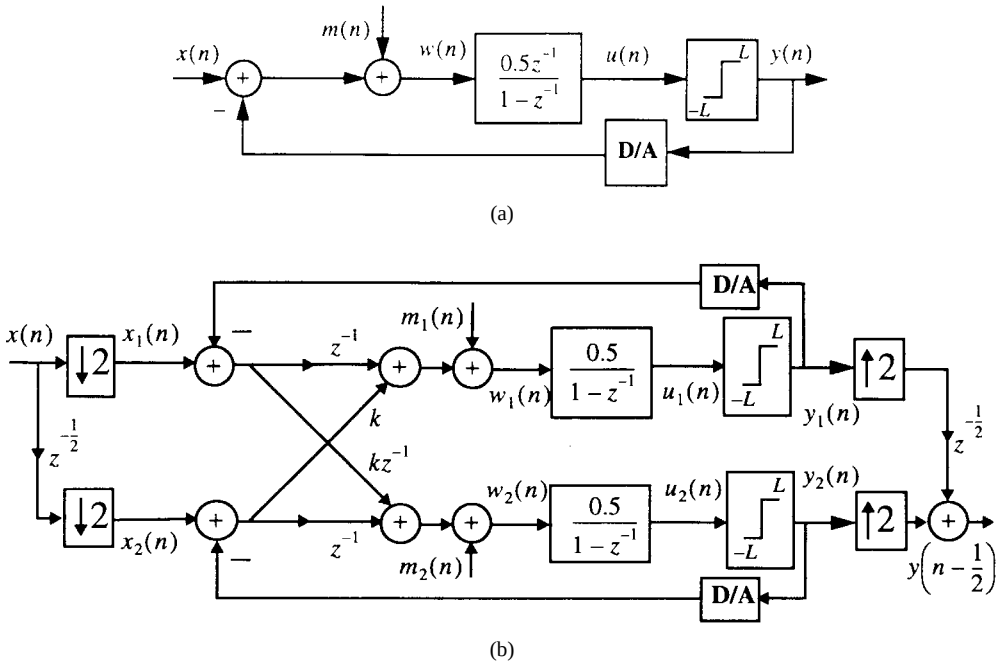


Fig. 10. First-order $\Delta\Sigma$ modulator. (a) Conventional. (b) TIM.

the NTF has a new pole-zero pair at $-k$ and -1 causing a notch at π and a peaking near π. Noting that the total noise energy is constant, a notch in the NTF causes the noise to go elsewhere meaning that the noise floor will rise. A peaking in NTF causes the modulator to have larger integrator outputs which in turn makes the structure more prone to clipping and overloading eventually degrading noise-shaping performance [7]. Hence, there is a tradeoff between the maximum tolerable opamp offset and noise-shaping degradation which leads to an optimum value for k below which clipping effects due to opamp offsets are dominant and above which clipping due to the peaking of NTF would be dominant.

To verify these results, several simulations were carried out for the second-order TIM of Section II-C for $L = 3$ and $m_i(n) = \pm\ 0.015$. The results are depicted in Fig. 11. Note that there is a maximum dynamic range as was discussed and the optimal k in this case is around 0.96. Above this value, the dynamic range quickly deteriorates as integrator outputs saturate.

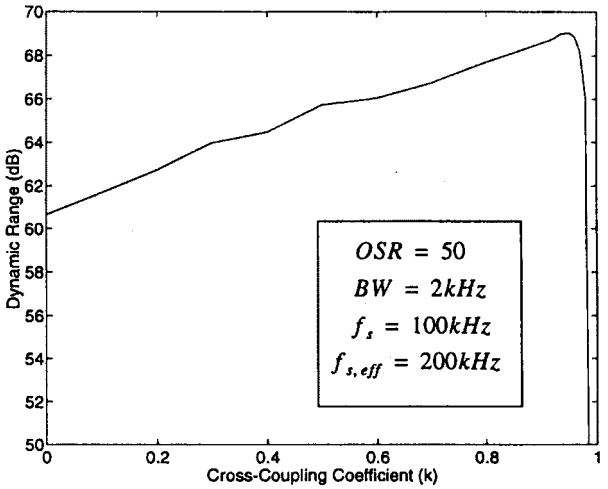


Fig. 11. Dynamic range versus cross-coupling coefficient. $L = 3$ and $m_i(n) = \pm\ 0.015$.

C. Mismatch Effects

In [13], the effect of coefficient mismatch on the performance of a general block digital filter is studied where it is shown that due to mismatches, the overall structure becomes time-varying and hence aliasing is present. It was also emphasized that those portions of the spectrum around $2\pi i/M$ ($i = 1, 2, \cdots, M-1$) would first get attenuated and then folded back into the band of interest. Also, it was shown that the attenuation factor for FIR block filters is proportional to the mismatch ratio.

Unfortunately, the general analysis for mismatch effects in a TIM structure is a difficult problem since one has to deal with a time-varying multirate nonlinear system whose transfer function could be IIR in general. However, simulation results indicates that the overall effect is similar to the mismatch effect in block digital filtering. Specifically, for $M = 2$ and recalling $f_{s,\text{eff}}$ to be the effective clock frequency $2f_s$, noise around $f_{s,\text{eff}}/2$ will be attenuated by a factor (related to mismatch ratio) and then folded back into the band of interest.

Furthermore, $\Delta\Sigma$ modulators tend to generate limit cycles at frequencies of $f_{s,\text{eff}}/2 \pm if_{\text{in}}$ where f_{in} is the input frequency [14]. Due to mismatch, these limit cycles will also fold back into the baseband and cause tones at if_{in} as if they were harmonics of the input frequency f_{in}. Note that these tones are originating from the time-varying nature of the structure rather than its nonlinearity.

Fig. 12 shows the spectrum for a 0.1% coefficient mismatch. Note that aliasing causes a flattening of the noise floor in

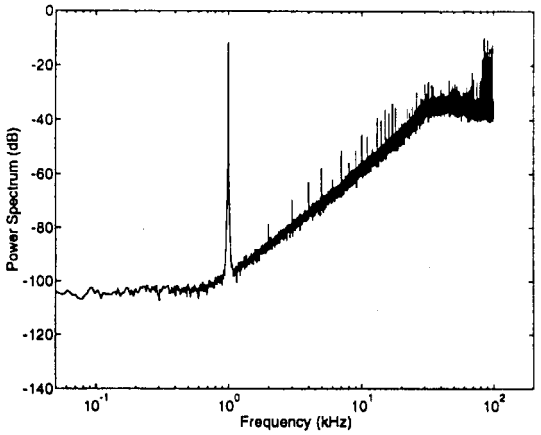


Fig. 12. Output spectrum for TIM with a 0.1% coefficient mismatch for $k = 1$.

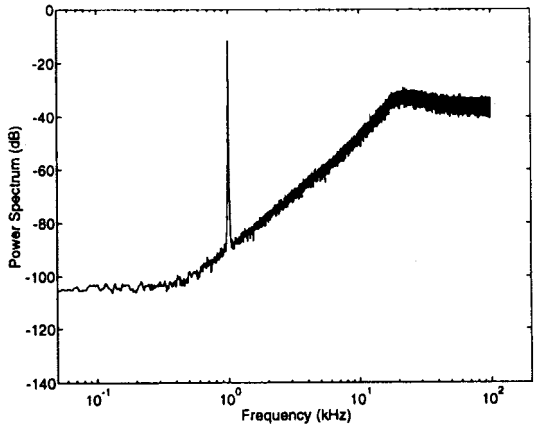


Fig. 13. Output spectrum for TIM with a 0.1% coefficient mismatch for $k = 1$ and dither $= [-L/2,\ L/2]$.

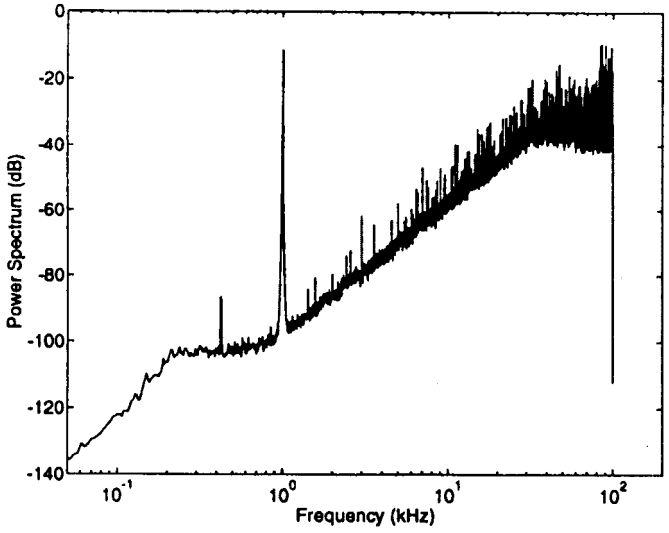
the band of interest sitting around -100 dB. This level is 60 dB $[-20 \log (0.001)]$ below the noise floor at $f_{s,\,\mathrm{eff}}/2$ (neglecting limit cycles). The tones at integer multiples of the input frequency are also caused by aliasing of the limit cycle tones at frequencies of $f_{s,\,\mathrm{eff}}/2 \pm i f_{ir}$.

Limit cycles are a disturbing phenomena in conventional $\Delta\Sigma$ converters and are traditionally removed by introducing dithering at the input of the 1-b-quantizer causing an increase in the noise floor [15]. In TIM structures, dithering not only alleviates the problem of in-band limit cycles but also destroys them elsewhere. By dithering, tones around $f_{s,\,\mathrm{eff}}/2$ disappear. Consequently, in-band harmonics due to aliasing vanish. Fig. 13 shows the output spectrum of the second-order TIM ($M = 2$) with dithering applied to both 1-b-quantizer inputs. The dithering signal is uniformly distributed between $\pm(L/2)$ where L is the output level. Note that tones around $f_{s,\,\mathrm{eff}}/2$ are completely removed at the expense of an increase in noise floor. It should be noted that the effect of this amount of dithering on TIM is comparable to that of a conventional modulator.

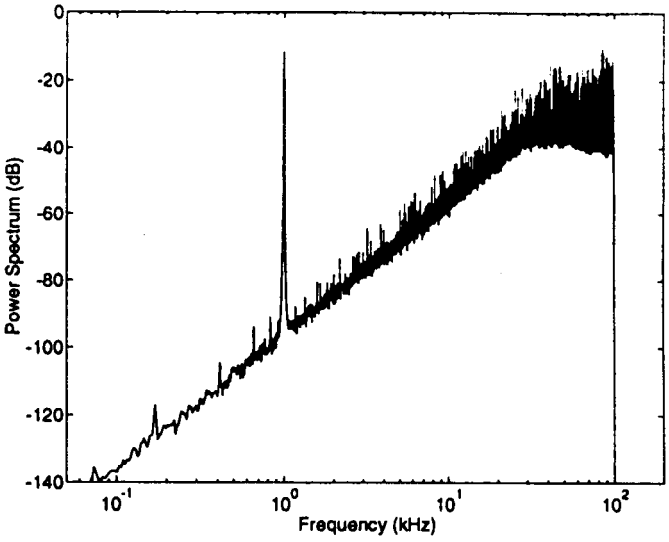
Adding dithering will remove the idle tones but aliased noise, if not corrected, will limit the amount of resolution that a TIM can achieve. For low values of OSR, the in-band noise is dominated by the *unaliased* noise floor (that which would occur in a conventional modulator operating at $f_{s,\,\mathrm{eff}}$). Hence for low values of OSR, mismatching should not cause any degradation in SNR. For high values of OSR, the in-band noise is dominated by aliasing. However, there exists a way to reduce this aliasing effect. As discussed in Section III-B, reducing k has the effect of generating a notch at $f_{s,\,\mathrm{eff}}/2$ for a first-order TIM. The same is true for a second-order TIM as verified by the following equation:

$$Y(z) = X(z)z^{-2}\,\frac{(k+z^{-1})^2}{(1+kz^{-1})^2} + E(z)(1-z^{-1})^2\,\frac{(1+z^{-1})^2}{(1+kz^{-1})^2}. \tag{13}$$

Note that the noise floor around $f_{s,\,\mathrm{eff}}/2$, which will be aliased back due to mismatching, is first attenuated by the two new zeroes generated at π. Fig. 14(a) and (b) shows the output



(a)



(b)

Fig. 14. Output spectrum for second-order TIM with a 0.1% mismatch and no dithering for (a) $k = 1$ and (b) $k = 0.90$.

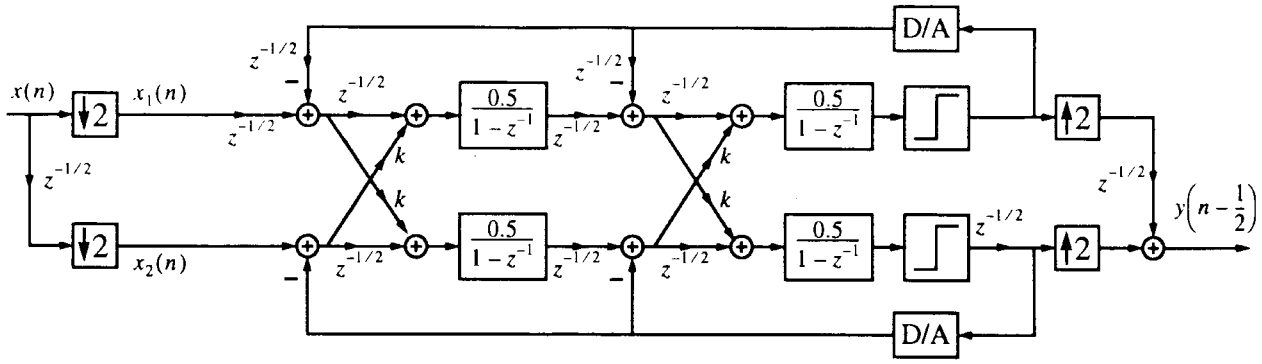


Fig. 15. Block diagram of a second-order time-interleaved $\Delta\Sigma$ modulator after delay redistribution.

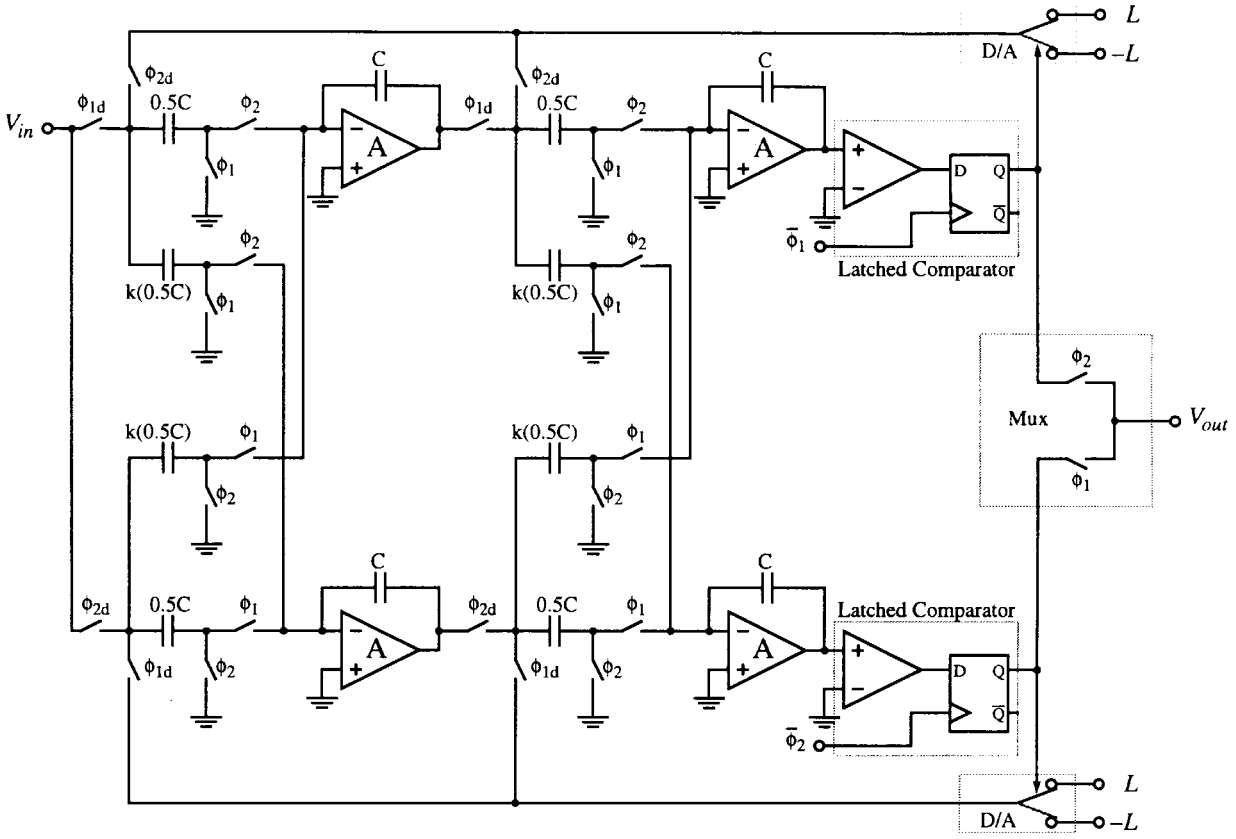


Fig. 16. Single-ended SC circuit for second-order TIM. $C = 3.8$ nF, $k = 0.96$, $L = 3$ V, and 100 kHz clock frequency.

spectrums for a second-order TIM with a 0.1% coefficient mismatch and no dithering for $k = 0.98$ and $k = 0.90$, respectively. Notice that in Fig. 14(a), the noise floor in the baseband shows an improvement over Fig. 12 due to the existence of a notch at $f_{s,\text{eff}}/2$. Reducing k to 0.90 effectively increases the notch width at $f_{s,\text{eff}}/2$ resulting in the spectrum of Fig. 14(b) in which the aliased component is not noticeable. However, as was mentioned in Section III-B, creating a notch at $f_{s,\text{eff}}/2$ has the effect of increasing the overall noise floor. Table I summarizes the effect of reducing k on the dynamic range value for bandwidths (BW) of 2 kHz and 500 Hz with an internal clock frequency of 100 kHz. For comparison, the dynamic range values for a conventional modulator clocked at the same rate are also given. Note that for a mismatch ratio of 0.1% and BW $= 2$ kHz, decreasing k deteriorates the dynamic range as aliasing is not the dominant component of the in-band noise and reducing k only makes the unaliased noise floor worse. However, for BW $= 500$ Hz, decreasing k significantly improves the dynamic range since the in-band noise is dominated by aliasing.

The k-factor technique is also applicable to the interpolative as well as the double-loop topologies with $M > 2$ [16]. However, the practical realization of time-interleaved modulators with $M > 2$, would be a challenging task. In fact, more SNR have to be traded away to keep the loops operating properly for $M > 2$.

TABLE I
DYNAMIC RANGE AS A FUNCTION OF k FOR A 0.1% COEFFICIENT MISMATCH AND NO DITHERING

	k	Dynamic Range (dB)	
		$BW = 2kHz$ $f_s = 100kHz$	$BW = 500Hz$ $f_s = 100kHz$
TIM	1.00	71.15	88.31
	0.98	70.49	89.65
	0.95	70.35	98.10
	0.90	68.89	99.47
Conventional Modulator		58.02	87.50

IV. EXPERIMENTAL RESULTS

A second-order time-interleaved $\Delta\Sigma$ modulator was derived from a conventional A/D modulator by using the block filtering theory discussed above. A single-ended switch capacitor version was realized using discrete components and the results are presented here.

A. TIM SC Circuit

A second-order double-loop structure taken from [8] and shown in Fig. 6(a) is used as the starting point. From this structure, a second-order time-interleaved by 2 ($M = 2$) counterpart is derived as shown in Fig. 6(e). Before this block diagram can be implemented in a single-ended SC version, delay redistribution must be done since only noninverting delayed and inverting nondelayed parasitic insensitive integrators (similar in structure to that shown in Fig. 8) are to be used. It should be noted that even though stray-compensated inverting delayed integrators are realizable, they are more complicated and rely on capacitance matching for stray insensitivity [10]. We start the rearrangement of delays by splitting one delay into two half delays. The objective of this procedure is to remove the cross-coupling branches that have a gain of 1 and no delays. Also, it is desired to have a half delay at the output of the comparators to make available the use of latched comparators. For chip design, this modification is important as latched comparators are typically faster than their unlatched counterparts. The result of the delay rearrangement is shown in Fig. 15.

Note that the diagram in Fig. 15 still has one path that requires a positive nondelaying integrator. This path is from $x_2(n)$ to the top-left integrator. The solution to this problem lies in the presence of a half delay in the input sampler which should sample $x(t)$ and a half-delayed replica of it before feeding them into $x_1(n)$ and $x_2(n)$ simultaneously. Instead of doing so, the operation of the TIM blocks are staggered, meaning that the two halves of the modulator are out of synchronization by half a delay. There is therefore an implicit half-delay when traversing a cross-coupling path. It should be noted that in a fully differential design, noninverting nondelayed integrators are available and thus, there is no need for staggering the two halves.

The single-ended SC circuit is shown as Fig. 16. The 1-b output can be obtained by sampling the top latched comparator output during ϕ_2 and the bottom latched comparator output during ϕ_1. For this experiment, a clock of 100 kHz was used with a 1 kHz input resulting in $f_{s,\text{eff}} = 200$ kHz. An added feature of the board was the ability to turn off the cross coupling connection thereby degenerating the time-interleaved circuit into a conventional second-order modulator. This feature was added to measure the results for the conventional case and is important because a comparison of the time-interleaved A/D with published results for conventional second-order modulators is inaccurate due to dissimilar circuit nonidealities. Measuring the results using one board guarantees the same amount of circuit nonidealities for both the time-interleaved and the conventional case.

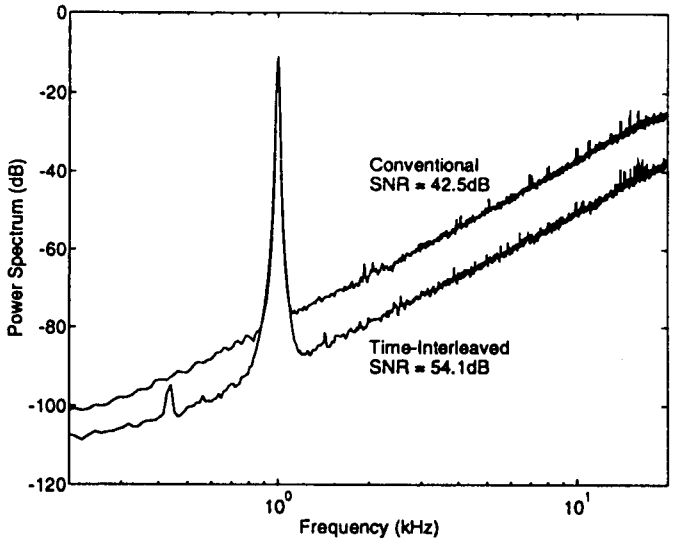


Fig. 17. Experimental results for conventional versus second-order TIM for $k = 0.96$.

Some of the circuit component characteristics are as follows: 1) the switches (ADG201HS) inject 50 pC when turned off; 2) the opamps (AD843) have an open-loop gain of 80 dB and an offset of around 1 mV; 3) the Polystyrene capacitors are accurate to 0.3% (limited by the capacitance meter used), and d) the comparators (LM361) have a 20 ns response time. The capacitance C was chosen to be 3.8 nF. A smaller capacitance increased the effect of charge injection whereas a larger value prevented the outputs of the integrators to settle within 5 μs (defined here as the time from 10–90% of final output value). Therefore, the charge injection of the switches caused a 13 mV change in the integrating capacitor voltage. This clock-feedthrough effect is similar to dc offset and therefore has to be included in the calculation of the amount of mismatch needed to stabilize the system. According to Fig. 11, the optimal for such an offset is 0.96.

B. Output Spectrum

A memory board was built to capture 256k consecutive samples from each of the latch outputs and store them into a file allowing digital signal processing (DSP) programs to calculate the FFT and generate an accurate spectrum of the digital signal. The combining of the latch outputs into a 1-b signal is done inside the DSP program. Care should be

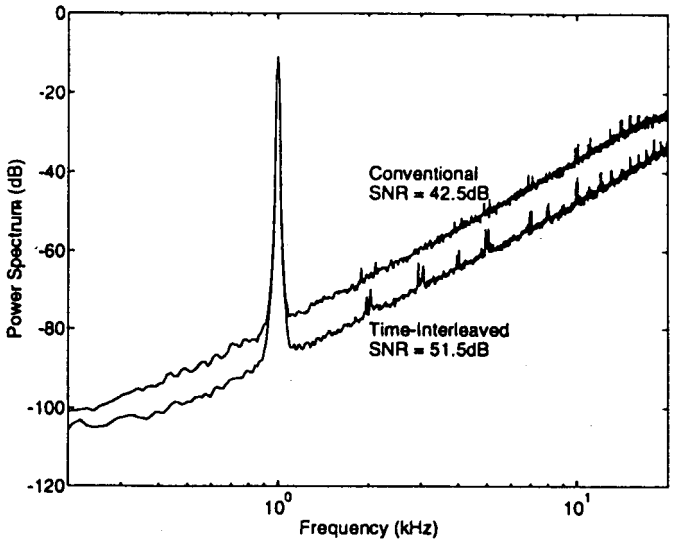


Fig. 18. Experimental results for conventional versus second-order TIM for $k = 0.99$.

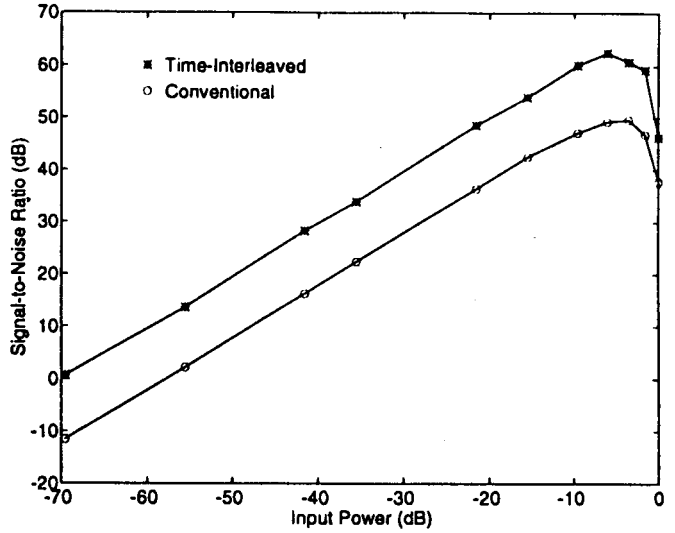


Fig. 19. Measured SNR for $f_s = 100$ kHz, $f_{\rm in} = 1$ kHz, BW = 2 kHz, and $k = 0.96$.

taken when combining the outputs. The order of the output combining is the same as the order of the input sampling.

Fig. 17 shows the spectrums for the conventional versus the TIM for a 1 kHz input with an amplitude of 0.5 V_p (15 dB below full-scale) and $k = 0.96$. The SNR values shown are calculated for a bandwidth of 2 kHz. The SNR of the time-interleaved version is seen to be 12 dB better than that of the conventional modulator as opposed to a potential 15 dB improvement. The discrepancy arises because of the reduction of the cross-coupling capacitors ($k < 1$) and dc offsets which raise the noise floor.

Fig. 18 shows the result when $k = 0.99$. Note that there is a 2.5 dB degradation in SNR for the time-interleaved case as compared to results of Fig. 17. Furthermore, the observed nonlinearity is a result of the clipping of integrator outputs as their dc levels increased since was approaching unity.

Fig. 19 shows the measured SNR for a variety of input amplitudes. On average, the SNR of the time-interleaved modulator is 12 dB better than that of the conventional modulator clocked at the same frequency.

V. Conclusions

The concept of time-interleaving has been extended to $\Delta\Sigma$ modulators. Utilizing block digital filtering, a general procedure for deriving the time-interleaved equivalent of arbitrary $\Delta\Sigma$ converters was presented. Practical issues regarding implementation of these time-interleaved converters were also addressed. Specifically, problems such as finite opamp gain, dc offset, and component mismatch were discussed and analyzed. Practical solutions were suggested to overcome some of these effects and several tradeoffs were introduced. Finally, a second-order time-interleaved by two $\Delta\Sigma$ A/D converter was implemented with discrete components. Experimental results show that the time-interleaved modulator has a 12 dB better signal-to-noise ratio than that of a conventional one operating at the same clock-rate. Thus, resolution was improved by two bits without increasing the clock frequency.

References

[1] J. Candy and G. Temes, "Oversampling methods for A/D and D/A conversion," in *Oversampling Delta-Sigma Data Converters*, J. C. Candy and G. C. Temes, Eds. New York: IEEE Press, 1991.
[2] D. A. Kerth, "A 120 dB linear switched-capacitor Delta–Sigma modulator," in *ISSCC*, Feb. 1994, pp. 196–197.
[3] A. Petragalia and S. K. Mitra, "High speed A/D conversion incorporating a QMF bank," *IEEE Trans. Instrum. Meas.*, vol. 41, pp. 427–431, June 1992.
[4] I. Galton and H. T. Jensen, "Oversampling parallel delta-sigma modulation A/D conversion," *IEEE Trans. Circuits Syst. II*, vol. 43, pp. 801–810, Dec. 1996.
[5] R. Khoini-Poorfard and D. A. Johns, "Time-interleaved oversampling convertors," *Inst. Elect. Eng. Electron. Lett.*, vol. 29, no. 19, pp. 1673–1674, Sept. 1993.
[6] P. P. Vaidyanathan, *Multirate Systems and Filter Banks.* Englewood Cliffs, NJ: Prentice-Hall, 1993.
[7] K. C.-H. Chao, S. Nadeem, W. L. Lee, and C. G. Sodini, "A higher order topology for interpolative modulators for oversampling A/D converters," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 309–318, Mar. 1990.
[8] B. E. Boser and B. A. Wooley, "The design of Sigma-Delta modulation analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1298–1308, Dec. 1988.
[9] P. D. Welch, "The use of fast Fourier transform for the estimation of power spectra," *IEEE Trans. Audio Electroacoust.*, vol. AU-15, pp. 70–73, June 1970.
[10] R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing.* New York: Wiley, 1986.
[11] R. Schreier, "On the use of chaos to reduce idle-channel tones in Delta-Sigma modulators," *IEEE Trans. Circuits Syst. I*, vol. 41, pp. 539–547, Aug. 1994.
[12] O. Feely and L. O. Chua, "The effect of integrator leak in Δ-Σ modulation," *IEEE Trans. Circuits Syst.*, vol. 38, pp. 1293–1305, Nov. 1991.
[13] R. Khoini-Poorfard and D. A. Johns, "Mismatch effects in time-interleaved oversampling converters," in *IEEE Int. Symp. Circuits Syst.*, London, England, May 1994, pp. 5.429–5.432.
[14] S. Harris, "How to achieve optimum performance from Delta-Sigma A/D and D/A converters," in *Proc. 93rd AES Convention*, Oct. 1992, preprint #3417.
[15] S. R. Norsworthy, "Effective dithering of Sigma-Delta modulators," in *IEEE Proc. ISCAS'92*, May 1992, vol. 3, pp. 1304–1307.
[16] R. Khoini-Poorfard, "Analysis methods and time-interleaving architectures for oversampling modulators," Ph.D. dissertation, Univ. Toronto, Toronto, Ont. Canada, 1995.

Ramin Khoini-Poorfard (S'90–M'95) was born in Tehran, Iran, on July 31, 1965. He received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Tehran in 1987 and 1989, respectively, and the Ph.D. degree in electrical engineering from the University of Toronto, Toronto, Ont., Canada, in 1995.

He was a research and teaching assistant since September 1990 with the University of Toronto. Upon completion of his doctoral work, he joined Lucent Technologies (formerly AT&T Bell Laboratories) where, as a member of technical staff, he is involved with analog circuit design for mobile communication chip-sets. His research interests include analog circuit design, analog, and digital signal processing for telecommunication systems, delta-sigma modulators, and adaptive systems.

Dr. Poorfard was a recipient of the University of Toronto Open Doctoral Fellowship in 1991 and the Ontario Graduate Scholarship from 1992 to 1994.

Lysander B. Lim (S'90–M'94) received the B.A.Sc. (Hons.) and M.A.Sc. degrees in electrical engineering from the University of Toronto, Toronto, Ont., Canada, in 1992 and 1994, respectively.

From 1992 to 1994, he worked on BiCMOS integrated circuits design for analog applications. Since 1994, he has been with Lucent Technologies (formerly AT&T Bell Laboratories), Allentown, PA, where he has been engaged in the design of high-performance mixed-signal CMOS integrated circuits for wireless applications.

Mr. Lim is the recipient of the Natural Sciences and Engineering Research Council of Canada (NSERC) from 1992 to 1994. His research interests include signal processing and integrated circuits design.

David A. Johns (M'88–SM'96) received the B.A.Sc., M.A.Sc., and Ph.D. degrees from the University of Toronto, Canada, in 1980, 1983, and 1989, respectively.

From 1980 to 1981, he was with Mitel Corp., Ottawa, Canada, and from 1983 to 1985 he was an analog IC designer at Pacific Microcircuits Ltd., Vancouver, Canada. His doctoral work focused on analog and digital adaptive filters including the development of an orthonormal structure for analog filters. In 1988, he joined the University of Toronto where he is currently an Associate Professor. He has on-going research programs in the areas of analog integrated circuits, oversampling, and digital communication circuits resulting in more than 40 publications and one textbook. He has been involved in numerous industrial short courses and has just completed a one-year research leave with Brooktree Corp., San Diego, CA, in the area of high-speed digital communications.

Dr. Johns is a past and present Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS.