A Differential 160-MHz Self-Terminating Adaptive CMOS Line Driver

Rajeevan Mahadevan and David A. Johns

***Abstract*—A wide-band differential line driver is presented for transformer-coupled cables integrated in standard 0.35-μm CMOS. It achieves 160-MHz bandwidth and no loss in implementing the cable termination. While operating from a 3.3-V supply, the driver dissipates 155 mW and exhibits a −47.5-dB THD for a 2-V_{pp} signal across a 75-Ω load. Automatically tuned termination and a voltage gain independent of process and load impedance variation are provided by the architecture.**

***Index Terms*—Adaptive circuits, CMOS, line driver, self-termination.**

I. Introduction

THERE IS GREAT interest in transmitting high-speed data over coaxial and twisted-pair cables due to their availability and low-cost. The proliferation of computer networks, for example, has placed increased demands for higher speed and more efficient use of existing cable infrastructure. To meet these demands transmission schemes have been developed that require sophisticated transceiver circuits. These demands have created challenges and obstacles for the circuit designer, especially in the case of the analog front-end circuits such as line drivers and analog-to-digital converters. This paper focuses on the line driver design and presents a circuit that addresses some of these challenges. The circuit is a differential current-mode line driver suitable for transformer-coupled channels with no loss in termination, automatically tuned output impedance and a voltage gain that is independent of process and load impedance variations. The target application for this particular design is the full-duplex transmission of up to 622 Mb/s over 300 m of coaxial cable using a multilevel modulation scheme. However, the concept can also be applied for use in other wired data communication applications.

In Section II, the basic requirements of a line driver in a full-duplex application are outlined. In Section III, a line driver circuit that meets these requirements is presented. In Section IV, experimental results are given and conclusions are drawn.

II. Line Driver Requirements

Fig. 1 shows the block diagram of a generic full-duplex transceiver. A line driver is a key component of this architecture since it provides the necessary power gain to transmit the modulated signal over the low characteristic impedance of a cable. For coax this impedance is typically 75 Ω, while in the case of a twisted-pair it is roughly 100 ohms. For a fully integrated transceiver, the line driver must be designed using CMOS technology. While the supply voltage for modern deep-submicron CMOS processes has continued to shrink, the output voltage signal swing has remained the same or increased due to the multilevel modulation schemes used to achieve higher bit rate. For example, typically 2-V peak-to-peak output from a 3.3 or 2.5-V supply is required. In order to generate this signal across 75 Ω, large currents are required from the driver. The full-duplex nature of the system also means that echo cancellation is an integral part of the transceiver. Fully digital echo cancellation techniques require a linear echo path and this imposes a linearity constraint on the line driver. This linearity must be achieved in the presence of the received far-end signal. Hence, in addition to generating the transmit signal, the driver must have headroom for the far-end signal which can be as large as the transmit signal. Cable termination, characterized by the return loss, is also important due to the bidirectional transmission. A poorly terminated line produces reflections which appear as echo and hence complicate the echo removal process. Best return loss performance is provided by a tunable line driver output impedance that automatically tracks the cable to cable characteristic impedance variation. For twisted-pair this variation can be as high as ±15% while for coaxial it is typically ±2%. This cable variation combined with the process variation can cause the transmit voltage to vary significantly for a current-mode output stage. It is, however, desirable to have a constant voltage gain over process and cable impedance variation. This is important so as not to overwhelm the near-end receiver and to meet the transmit templates of standards.

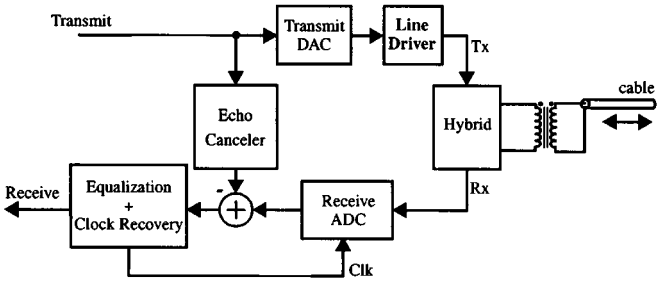

Fig. 1. The main blocks of a transceiver.

The design of an efficient driver that satisfies all these constraints is a challenging one in modern low supply voltage CMOS processes. In traditional architectures, there is a 6-dB signal loss incurred in the external resistors that implement cable termination which adds to the inefficiency of the driver. An approach that provides integrated termination with no signal loss in the termination is also a desirable feature for line drivers.

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R. Mahadevan is with Snowbush Inc., Toronto, ON M5S 2T9, Canada.

D. A. Johns is with the Department of Electric and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada.

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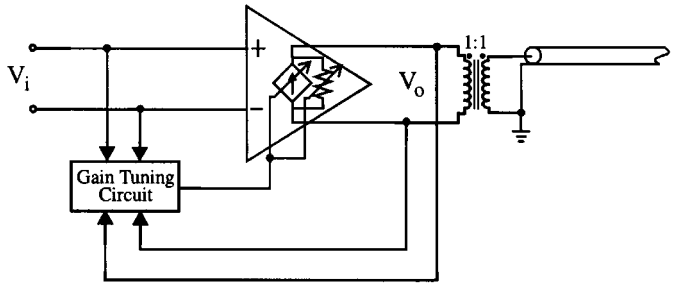


Fig. 2. Proposed line driver topology block diagram.

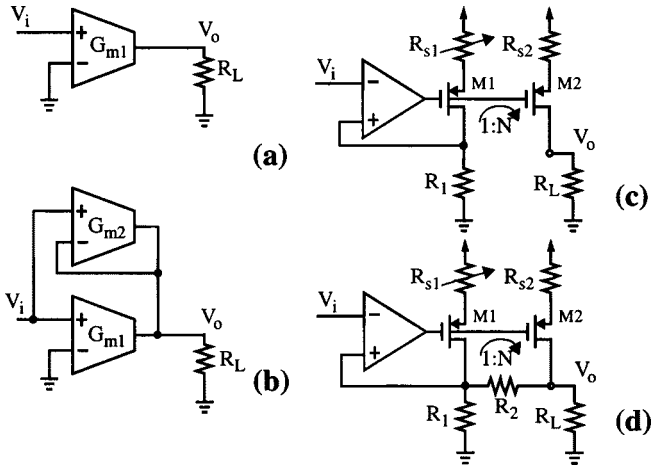


Fig. 3. Circuit for driving low resistive loads.

III. Circuit Architecture

Fig. 2 shows the block diagram of the proposed line driver topology. This topology uses an adaptable current-mode output stage along with a gain tuning circuit to meet the requirements outlined in Section II. An external parallel termination resistor is not used as the output stage provides self-termination with no signal loss in the termination. The gain tuning circuit ensures the voltage gain is unity independent of process and cable impedance variation. It also ensures the output impedance is set correctly to equal the cable impedance for optimum return loss performance.

The current-mode output stage builds upon an approach proposed in [1] for driving low resistive loads. This is shown conceptually in Fig. 3. In Fig. 3(a), an ideal transconductance cell, G_{m1}, is used to drive a resistive load to obtain a voltage gain and output impedance given by

$$\frac{V_o}{V_i} = R_L G_{m1} \quad Z_{\text{out}} = \infty. \tag{1}$$

If a second transconductance cell, G_{m2}, configured as an active resistor is placed as shown in Fig. 3(b), then

$$\frac{V_o}{V_i} = \frac{(G_{m1}+G_{m2})R_L}{1+G_{m2}R_L} \quad Z_{\text{out}} = \frac{1}{G_{m2}}. \tag{2}$$

If G_{m1} and G_{m2} are tunable and are set to $G_{m1} = G_{m2} = 1/R_L$, then

$$\frac{V_o}{V_i} = 1 \quad Z_{\text{out}} = R_L. \tag{3}$$

Since the voltage gain is unity, the differential input voltage to the G_{m2}-cell is nominally zero and it produces no output signal current in realizing the termination. As a result, termination has been achieved without incurring any loss and a tunable output impedance is obtained.

In terms of the circuit realization, the transconductor without G_{m2} can be implemented as shown in Fig. 3(c). The input voltage is copied across R_1 using an opamp. The resulting current is amplified by the current amplification factor, N, and produced at the output. N and hence the transconductance of the circuit is tuned by varying R_{s1} which can be a transistor operating in triode. If N is chosen to be large (around 40), then the power consumption of the supporting circuitry can be minimized and most of the power will be consumed at the output consisting of M2 and the load. The addition of G_{m2} is equivalent to placing R_2 as shown in Fig. 3(d). In the ideal case, the output impedance is given by

$$Z_{\text{out}} = \frac{R_2}{N+1}. \tag{4}$$

In the design process, R_1 and R_2 are chosen to be

$$R_1 = N_{\text{nom}} R_{L\text{nom}} \quad R_2 = (N_{\text{nom}}+1)R_{L\text{nom}} \tag{5}$$

where N_{nom} and $R_{L\text{nom}}$ are the nominal values of N and R_L respectively. A tuning circuit is then used to force $V_o = V_i$ by changing N to account for the variation in R_1 and R_L. Although this tuning accounts only for the variation in R_1 and R_L, the output impedance will also be set correctly to equal R_L since the variation in R_2 tracks that of R_1 due to the good matching of on-chip resistors.

The approach as presented in Fig. 3 is unsuited for use in many high-speed wired data communication applications. It is a single-ended circuit that requires a dc-coupled load. In this circuit, the key requirement for no loss in the termination is that the node voltages across R_2 are identical. Since the input voltage is copied across resistor R_1 to generate a current and this current is mirrored to the output, the output voltage can only equal the input voltage as long as the load impedance seen by the circuit is also resistive (no frequency dependence). However, many wired channels are ac-coupled using a transformer to avoid ground loops and reject common-mode signals. For a transformer-coupled load, the dc and ac impedances are not identical and hence the circuit approach can not be used directly. In addition, the driver topology must be differential to obtain the best dynamic range and noise immunity. Modern transceivers have a small analog front-end along with a large digital back-end with the potential for large logic sections to switch simultaneously. This can lead to significant substrate and supply noise injection which must be rejected by the sensitive analog blocks. Hence these blocks must be differential. Distortion performance is also improved since even-order harmonics are eliminated in a differential circuit.

The presented approach can be modified for use in a transformer-coupled environment. In Fig. 4, two single-ended half-circuits are used to drive the cable differentially through a transformer. To enable the half-circuits to function properly, resistor

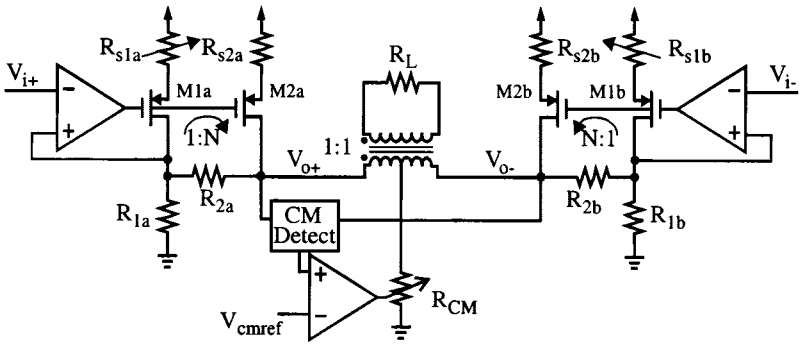


Fig. 4. Transformer-coupled differential driver topology.

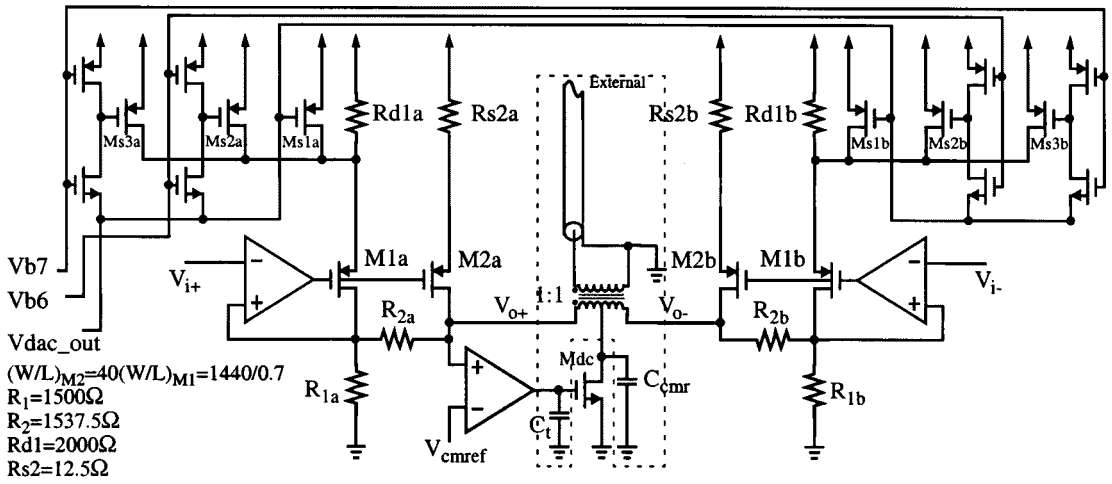


Fig. 5. Complete differential line driver.

R_{CM} is connected at the primary side center tap. For a transformer, the dc and common-mode input signals of the primary side see the impedance connected to the center tap while the differential primary input signals see the impedance transformed from the secondary side. By choosing an appropriate R_{CM}, both these impedances can be made identical allowing each half-circuit to see the same dc and ac impedance. However, a fixed R_{CM} cannot be used since the exact value of R_L is unknown ahead of time. Instead a variable resistor along with a common-mode tuning loop is used. The output common-mode is determined and forced equal to a reference common-mode, V_{cmref}, by varying R_{CM}. If the input to the driver also has its common-mode equal to V_{cmref}, the dc voltages across R_2 will be identical. Once this is established, N can be tuned to set the output differential voltage equal to the input differential voltage ensuring no signal loss across R_2.

The complete driver schematic is shown in Fig. 5. The variable resistor at the center tap is implemented by Mdc, a transistor operating in triode. Tuning of this resistor is performed by the opamp and tuning capacitor C_{t}. Instead of using a common-mode detection circuit, the opamp directly samples the output node because a passband modulation scheme is being used where the input differential signal to the line driver has negligible frequency content below 1 MHz. As long as the loop bandwidth is well below the signal frequency (1 MHz), the common-mode tuning loop functions properly. In applications where there is significant low frequency content, a common-mode detection circuit can be used or the center tap voltage can be sampled. However, the disadvantage of using the center tap voltage as the common-mode is that any resistive voltage drops in the transformer and the package are not compensated for. Gain tuning, by varying N, is achieved using triode transistors Ms1, Ms2, and Ms3, whose gate voltage is set by a 5-bit digital-to-analog converter (DAC). The required tuning range is determined by the variation in R_1 over the process corners and by the expected cable to cable characteristic impedance variation. For the coaxial application and the CMOS process being used, a tuning range of $\pm 30\%$ is required. This wide tuning range necessitates the use of three triode transistors. Ms2 and Ms3 are successively added in parallel to Ms1 to extend the range. This is handled by the additional circuitry associated with these transistors. Overlap between the tuning ranges is ensured to avoid misconvergence in the tuning algorithm. In this circuit, all opamps use the current-mirror topology and the DAC uses a thermometer code topology [5].

A gain tuning circuit is required to set $V_o = V_i$ for this line driver to function properly. A simple gain-forcing approach can not be used to force the output voltage to equal the input since in full-duplex application, the output node voltage has the far-end signal superimposed on it. Instead, a correlation-based approach using *sgn-sgn* least-mean-square (SS-LMS) algorithm is used.

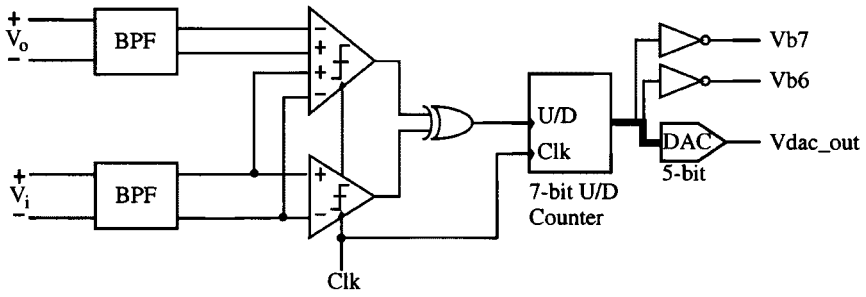


Fig. 6. SS-LMS gain tuning circuit.

SS-LMS is used instead of the other LMS variants due to its robustness to dc offsets and because it is inherently suited for a mostly digital implementation as shown in Fig. 6. The required control voltage is given by

$$V_c = \mu \int_0^t \text{sgn}(V_i(\tau) - V_o(\tau))\ \text{sgn}\ (V_i(\tau))\ d\tau \qquad (6)$$

where μ is the adaptation constant. In the circuit, the differencing and *sgn* operation are performed by clocked comparators. The *sgn* multiplication is performed by the XOR gate while the integration is performed by the 7-bit up/down counter and the 5-bit DAC. It can be shown that the adaptation constant is proportional to the clock frequency [6]. Hence, by changing the clock frequency, the convergence time as well as the excess mean-squared error after convergence can be controlled. Also, due to the use of the digital counter, adaptation does not have to be continuous. The counter can be frozen and updated periodically to account for slight variations over long time periods. The transfer function of the line driver is bandpass in nature due to the transformer zero at low frequency and the magnitude roll-off at high frequency. Since the output and input signals have different high and low frequency content, comparison should be made at mid-frequencies, above the lower corner frequency of the line driver. The bandpass filters shown accomplish this frequency-limiting function. The center frequency and quality factor of the filters do not have to be very accurate since all that is required is to limit the spectrum to mid-frequencies. This further simplifies the design of these circuits. A simple passive network can even be used if it is designed so as not to load the line driver.

IV. Experimental Results

The circuit of Fig. 5 along with the 5-bit gain tuning DAC were integrated in a standard 0.35-μm single-poly triple-metal CMOS process. A discrete implementation of the remaining blocks of the gain tuning circuit (Fig. 6) was used to characterize the line driver. The bandpass filters were implemented using a passive *RC* network. A sampling oscilloscope and some logic were used to construct the rest of the digital circuitry and control the on-chip DAC. The chip photomicrograph is shown in Fig. 7. The active area of the driver including the DAC is 0.21 mm^2. All measurements described below have been taken after the convergence of the gain tuning loop and using a surface-mount signal transformer like those used in Fast and Gigabit Ethernet. For this particular process batch, R_1 and R_2 were 22% higher than their nominal value. However, the gain tuning loop was able to successfully compensate for this variation as it was designed to handle $\pm$30% variation.

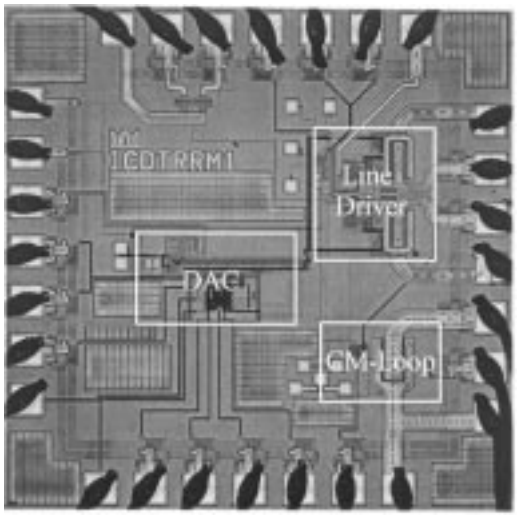


Fig. 7. Chip photomicrograph.

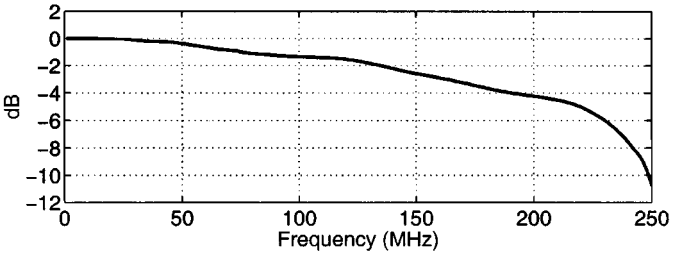
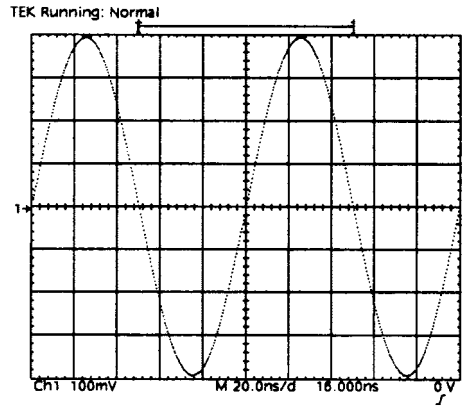
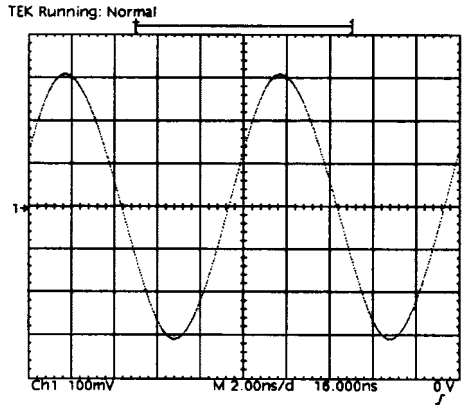


Fig. 8. Line driver frequency response: $f_{-3\text{dB}} = 160$ MHz.

The power consumption of the driver is 155 mW. The supporting circuitry including the opamps and the DAC consume 14 mW. The remainder is dissipated at the output branches consisting of M2 and the load. Due to the class-A nature of the driver, the output quiescent current must at least be equal to the peak signal current. The presence of the far-end signal at the output further increases the required quiescent current and this dictates the power consumption of the driver. The measured frequency response of the driver is depicted in Fig. 8. When driving a 75-Ω load through the transformer, the driver's $-$3-dB bandwidth extends to 160 MHz. The achievable bandwidth is limited by the need to maintain a good phase margin for the opamp based feedback loop while driving the large capacitive load presented by the output transistors. In addition, the limited band-



(a)



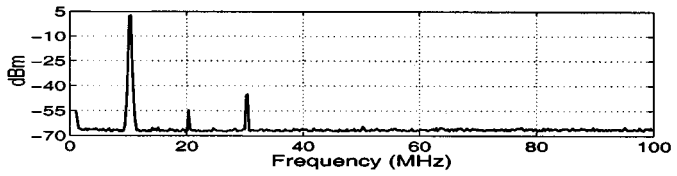
(b)

Fig. 9. Output signal. (a) At 10 MHz. (b) At 100 MHz.

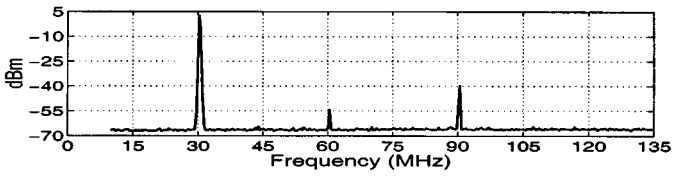
width provided by many surface-mount signal transformers further reduces the overall frequency response of the driver.

Some sinusoidal large signal waveforms when driving a 2-V_{pp} signal across 75-Ω load is shown in Fig. 9. Since the driver requires a 75-Ω load and all the test equipment are 50-Ω systems, a 75-to-50 Ω converter was used. It had about 7.5 dB of attenuation, and thus the shown wave-forms are all about 7.5 dB larger at the output of the driver. The output's harmonic contents for a 2-V_{pp} 10 and 30-MHz sinusoid are shown in Fig. 10. The main factors influencing the achievable total harmonic distortion of this circuit are the gain of the opamp and the peak signal current to quiescent current ratio in the output transistors, M1 and M2. Increasing the quiescent current in these transistors improves distortion performance at the expense of increased power dissipation. In pseudo-differential circuits, mismatches between the two halves leads to increased even-order harmonic components. In Fig. 10, the even-order components are around -60 dB from the fundamental and this indicates good matching between the two halves. The wideband signal response when driving a 62.5 and 100-MHz pn-sequence is shown in Fig. 11.

The output impedance was measured with a network analyzer. Fig. 12 illustrates the return loss of the driver including the signal transformer. Due to the on-chip adaptable termination, the return loss approaches -30 dB at low frequencies and degrades at higher frequencies mainly due to the parasitics of the transformer. A plot of the gain deviation is shown in Fig. 13. Gain deviation measures the deviation of the voltage gain of the

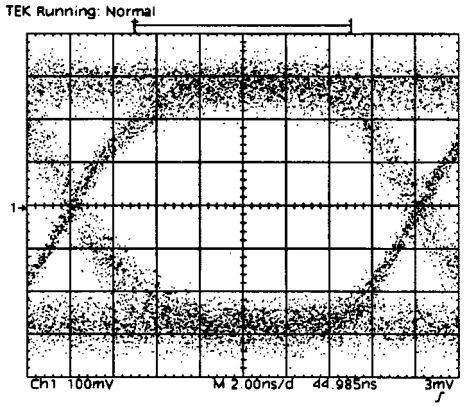


(a)

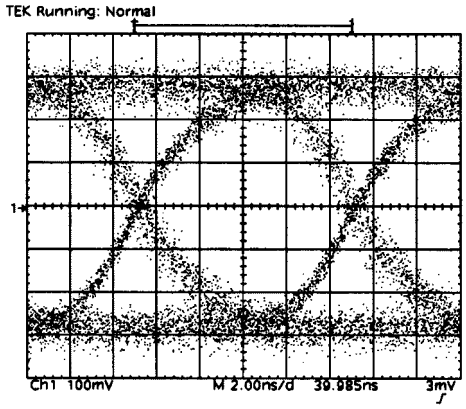


(b)

Fig. 10. Distortion for 2 V_{pp} across 75 Ω. (a) At 10 MHz where THD $=$ -47.5 dB. (b) At 30 MHz where THD $=$ -42 dB.



(a)



(b)

Fig. 11. Output eye pattern. (a) 62.5-MHz pn-sequence. (b) 100-MHz pn-sequence.

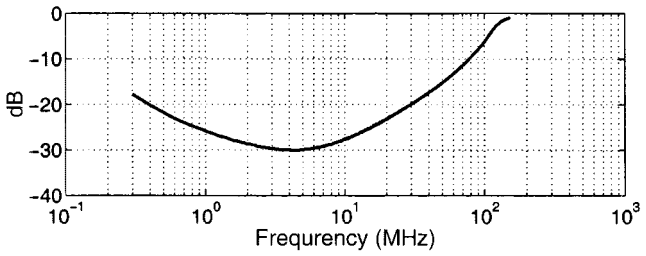


Fig. 12. Return loss performance including transformer.

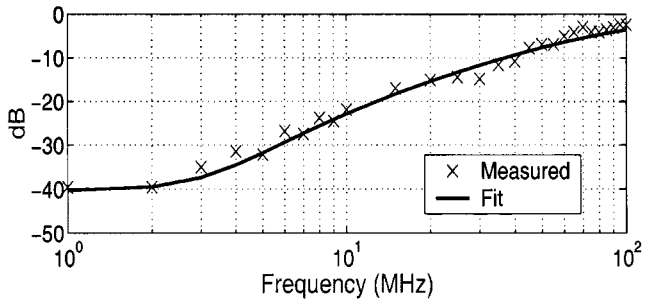


Fig. 13. Gain deviation: dB $(V_0/V_i - 1)$.

TABLE I
PERFORMANCE SUMMARY

Parameter	Value
Supply Voltage (Vdd)	3.3V
Output Voltage, 75Ω	$2V_{pp}$
-3dB Bandwidth	160MHz
THD $1.6V_{pp}$, 10MHz, 75Ω	-50.8dB
$1.6V_{pp}$, 30MHz, 75Ω	-46.0dB
$2V_{pp}$, 10MHz, 75Ω	-47.5dB
$2V_{pp}$, 30MHz, 75Ω	-42.0dB
Return Loss	-27.6dB@10MHz
	-10dB@80MHz
Power Dissipation	155mW
Noise (0.2-100MHz)	$62\mu V_{rms}$
Dynamic Range	81dB
Supply Rejection	33dB@1MHz
Active Area	$0.210mm^2$
Technology	0.35μm CMOS, 3AL, 1PS

driver from unity in decibels. The presence of the gain tuning loop ensures the voltage gain is very close to unity at low frequencies regardless of process and cable impedance variation. The gain deviates from unity at higher frequencies due to the magnitude roll-off and phase shift of the circuit. This figure indicates that a simple difference between the input and output of the line driver can provide significant reduction of near-end echo. This is an added benefit of using this line driver architecture.

Table I summarizes the experimental results.

V. CONCLUSION

A differential current-mode line driver suitable for transformer-coupled systems with 160-MHz bandwidth and better than −47.5-dB total harmonic distortion has been presented. This topology addresses some of the requirements of modern transceivers by providing integrated termination without incurring signal loss. Due to the presence of the automatic tuning loop, it provides robust performance regardless of variations. These performance improvements have been achieved at the cost of increased complexity of the line driver circuit.

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