A Time-Interleaved Continuous-Time $\Delta\Sigma$ Modulator With 20-MHz Signal Bandwidth

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***Abstract*—This paper presents the first implementation results for a time-interleaved continuous-time $\Delta\Sigma$ modulator. The derivation of the time-interleaved continuous-time $\Delta\Sigma$ modulator from a discrete-time $\Delta\Sigma$ modulator is presented. With various simplifications, the resulting modulator has only a single path of integrators, making it robust to DC offsets. A time-interleaved by 2 continuous-time third-order low-pass $\Delta\Sigma$ modulator is designed in a 0.18-μm CMOS technology with an oversampling ratio of 5 at sampling frequencies of 100 and 200 MHz. Experimental results show that a signal-to-noise-plus-distortion ratio (SNDR) of 57 dB and a dynamic range of 60 dB are obtained with an input bandwidth of 10 MHz, and an SNDR of 49 dB with a dynamic range of 55 dB is attained with an input bandwidth of 20 MHz. The power consumption is 101 and 103 mW, respectively.**

***Index Terms*—Analog-to-digital conversion, continuous-time, delta-sigma modulation, oversampling, time-interleaving.**

I. Introduction

DATA CONVERSION is an important operation that finds applications in many circuits. Delta-sigma ($\Delta\Sigma$) modulation is a relatively simple low-cost means of performing high-accuracy data conversion. Since $\Delta\Sigma$ modulators oversample the data, the signal bandwidth is limited by the sampling frequency and the oversampling ratio (OSR). Two methods of increasing the signal bandwidth include using continuous-time filters, and time-interleaving. This paper presents the combination of these two techniques by introducing a method of time-interleaving continuous-time $\Delta\Sigma$ modulators [1].

Typically, continuous-time $\Delta\Sigma$ modulators are able to operate two to four times faster than their discrete-time counterparts, but with lower accuracy and linearity [2]. Since no sampling is performed within the filters, the restriction of a maximum sampling frequency is only dependent on the regeneration time of the quantizer and the update rate of the DAC [2]. They also have the benefit of an inherent anti-aliasing filter in their signal transfer function (STF). One method of finding equivalence between a continuous-time and a discrete-time modulator is to recognize that an implicit sampling occurs in the quantizer of the continuous-time modulator [3]. Referring to Fig. 1, if the open-loop modulators are analyzed, the two modulators are equivalent as long as the outputs are equal at the sampling instants. Specifically, if $w[n] = w(t)|_{t=nT}$ for all n, then the loop filters are equivalent. The resulting condition for the two filters $B(z)$ and $B(s)$ to be equivalent is [4]

$$Z^{-1}\{B(z)\} = L^{-1}\{R(s)\cdot B(s)\}|_{t=nT}. \tag{1}$$

This transformation is known as the impulse-invariant transformation [5], where Z^{-1} represents the inverse z-transform, L^{-1} represents the inverse Laplace transform, and $R(s)$ represents the DAC pulse.

One of the major difficulties with continuous-time $\Delta\Sigma$ modulators is excess loop delay [3], which is the small delay that exists between the quantizer clock and the DAC pulses due to the nonzero switching time of the transistors. When excess loop delay in a continuous-time modulator is modeled in the discrete-time domain, the order of the discrete-time model increases, resulting in reduced stability when the pulse is temporally extended into the adjacent clock period [3]. To alleviate this problem, a return-to-zero (RZ) DAC pulse may be used so that it does not enter the adjacent clock period after the delay. The small delay between the quantizer and DAC can be taken into account by purposely clocking the DAC pulse a known time after the quantization occurs. To properly account for the adjusted length of the DAC pulse, $R(s)$ is represented by [3]

$$R(s) = \frac{e^{-\alpha s} - e^{-\beta s}}{sT}. \tag{2}$$

This assumes that the pulse is rectangular and has a magnitude of one, lasting from $t = \alpha$ to $t = \beta$. The time domain representation of this DAC impulse response is

$$r(t) = \begin{cases} 1, & \alpha \le t < \beta,\ 0 \le \alpha < \beta \le T \\ 0, & \text{otherwise.} \end{cases} \tag{3}$$

Block digital filtering can be used to time-interleave $\Delta\Sigma$ modulators [6], however this is a discrete-time technique that can only be applied to discrete-time $\Delta\Sigma$ modulators. A block digital filter is a system in which parallelism is used to reduce the speed requirement on each processing element. In [6], a method of time-interleaving two (or more) $\Delta\Sigma$ modulators is illustrated using this technique. When the appropriate block digital filter is used for M parallel $\Delta\Sigma$ modulators, it was shown that both the feedback and the quantizer can be done within each of the parallel branches. Thus, the digital filters, the ADCs and the DACs in each parallel branch operate at $1/M$

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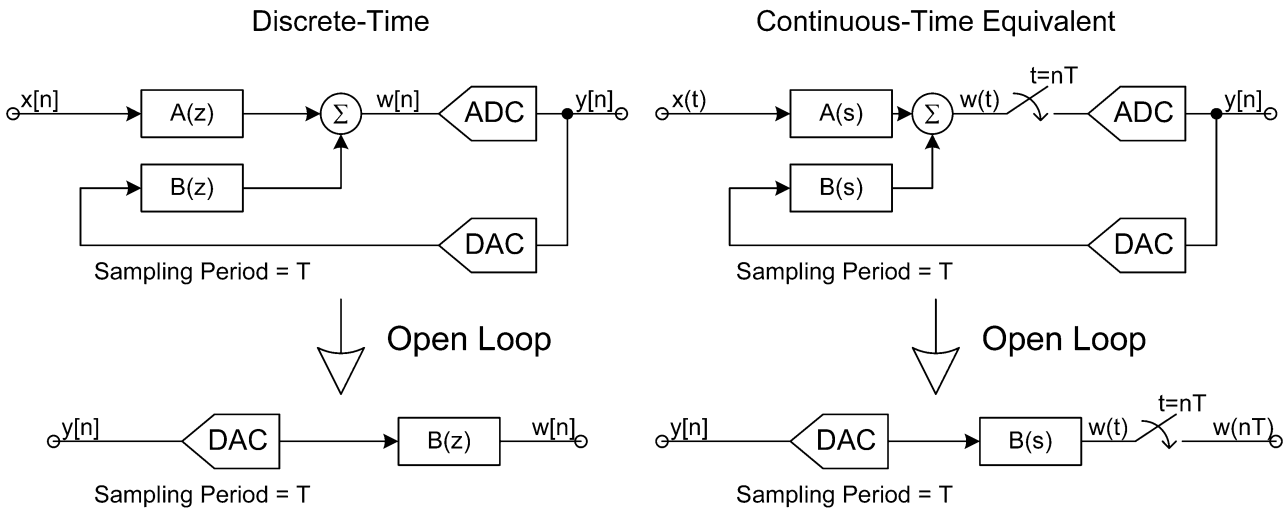

Fig. 1. Open-loop comparison of discrete-time and continuous-time loop filters.

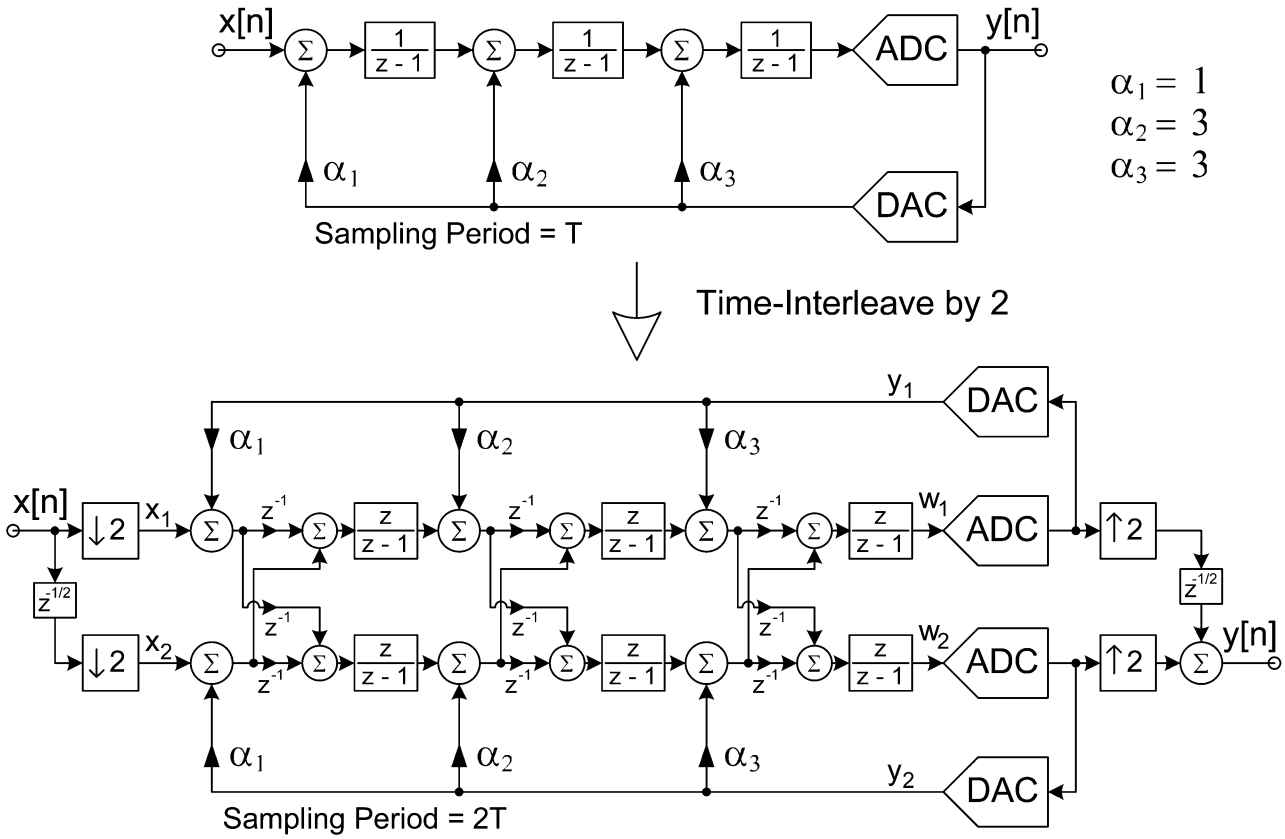

Fig. 2. Discrete-time to time-interleaved discrete-time modulator transform.

of the original rate. The effective OSR of the time-interleaved configuration is

$$\text{OSR}_{\text{eff}} = M \times \text{OSR} = \frac{M f_S}{2 f_O} = \frac{f_{S,eff}}{2 f_O}. \tag{4}$$

where $f_{S,eff}$ is the effective sampling frequency. Time-interleaving provides a method of effectively increasing the sampling frequency (and thus OSR) to achieve a higher signal-to-noise ratio (SNR) without having to operate the circuit components at higher frequencies. Alternatively, for a desired input signal bandwidth and resolution, the sampling frequency can be decreased in a time-interleaved modulator. The cost of this decreased sampling frequency is an increase in complexity since the circuit size increases by about the same factor that the sampling frequency is decreased. The transformation from a third-order discrete-time ΔΣ modulator to a third-order time-interleaved (by 2) discrete-time (DTTI) ΔΣ modulator is shown in Fig. 2. Additional upsamplers and downsamplers are required in the time-interleaved implementation of the ΔΣ modulator,

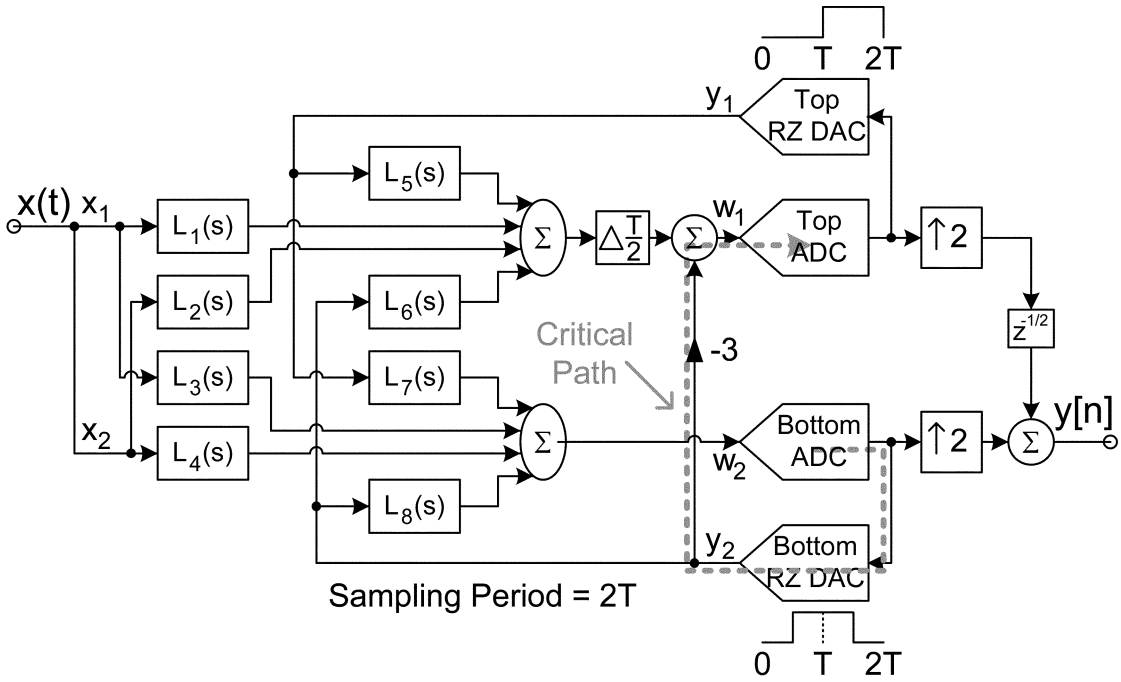

Fig. 3. Continuous-time loop filters with return-to-zero DACs.

as required by the theory of block digital filtering. The downsamplers at the inputs send even and odd samples of the input signal $x[n]$ to their respective branches, while the upsamplers at the output effectively recombine the even and odd samples for the output signal $y[n]$.

Research into DTTI $\Delta\Sigma$ modulators began with the block digital filtering method presented in [6], which was extended in [7] and [8] where a reduction in hardware complexity for more efficient architectures was presented. [9] presented a time-interleaved modulator that moved the critical path to the digital domain instead of performing this critical operation in the analog domain. Until [1], time-interleaving had yet to be investigated for continuous-time $\Delta\Sigma$ modulators.

The outline of this paper is as follows. In Section II, the application of block digital filtering followed by the discrete-to-continuous transform is demonstrated on a third-order discrete-time $\Delta\Sigma$ modulator to derive the resulting continuous-time time-interleaved (CTTI) $\Delta\Sigma$ modulator. Section III addresses the circuit design of the prototype, and Section IV presents the measured results from a prototype fabricated in 0.18-μm CMOS. A potential improvement to the modulator structure is investigated in Section V, followed by the conclusions in Section VI.

II. Time-Interleaved Continuous-Time $\Delta\Sigma$ Modulator Derivation

This section details how the new architecture, a time-interleaved continuous-time $\Delta\Sigma$ modulator, can be derived from a discrete-time $\Delta\Sigma$ modulator. The derivation is verified by system level simulations of the modulator with practical nonidealities added. The modulator is designed to achieve 10-bit resolution with an input bandwidth of either 10 or 20 MHz.

A. Time-Interleaved Discrete-Time $\Delta\Sigma$ Modulator

The $\Delta\Sigma$ Toolbox [10] is used to design a discrete-time third-order $\Delta\Sigma$ modulator that attains the desired 10 bits of resolution. The low-pass $\Delta\Sigma$ modulator of Fig. 2 achieves a signal-to-quantization-noise ratio of 70.5 dB with a 4-bit quantizer at an OSR of 10, resulting in a very reasonable sampling frequency of 100 and 200 MHz for signal bandwidths of 10 and 20 MHz (when time-interleaved by 2, the OSR is effectively 10, even though an OSR of 5 is actually used, resulting in the corresponding input bandwidth of 10 and 20 MHz). The noise transfer function (NTF) is $H(z) = (1 - z^{-1})^3$, while the STF is $G(z) = z^{-3}$. This modulator can be transformed into its time-interleaved by 2 equivalent modulator using the techniques presented in [6], as shown in Fig. 2. The DACs, ADCs, and filters of this DTTI modulator operate at half the frequency of the regular discrete-time modulator (i.e., with a sampling period of $2T$ instead of T), while the input downsamplers and output upsamplers operate at the full rate of the original discrete-time modulator.

B. Conversion to Continuous-Time $\Delta\Sigma$ Modulator

To find a continuous-time equivalent of this modulator, the discrete-time loop filters of the modulator must be found and then transformed to their equivalent continuous-time filters using the impulse-invariant transformation of (1). In this modulator, loop filters exist from x_1 to w_1, x_1 to w_2, x_2 to w_1, x_2 to w_2, y_1 to w_1, y_1 to w_2, y_2 to w_1, and y_2 to w_2. The resulting modulator with the loop filters transformed to their continuous-time equivalents is shown in Fig. 3, where the eight loop filters have been denoted $L_1(s)$ to $L_8(s)$. Two notable features of this figure will be discussed, specifically the critical path from y_2 to w_1, and the removal of the input downsamplers.

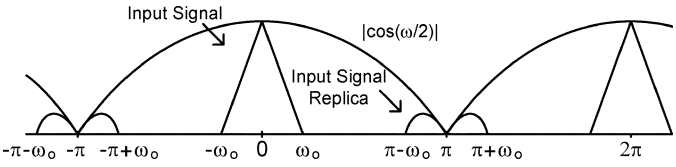

Fig. 4. Input signal and replica signal modulated by $|\cos(\omega/2)|$.

The downsamplers on the input of the discrete-time modulator have been eliminated in the continuous-time modulator since they cannot be used in a continuous-time system. This alters the STF slightly as the continuous-time modulator is no longer mathematically equivalent. As a result, similar to [8], a replica of the input signal occurs at $f_S/2 - f_O$ for a sampling frequency f_S and an input frequency f_O, and in general, $M-1$ replicas occur for a modulator time-interleaved by M. Furthermore, this replica signal (as well as the input signal) is attenuated by [11]

$$\frac{1}{M}\sum_{n=0}^{M-1} e^{jn\omega} = \frac{1}{M} + \frac{e^{j\omega}}{M} + \frac{e^{j2\omega}}{M} + \cdots + \frac{e^{j(M-1)\omega}}{M}. \quad (5)$$

Fortunately, at a high OSR, this degradation of the input signal is negligible (even at an OSR of 10, the attenuation of the input signal for a time-interleaved by 2 modulator is less than 0.11 dB). An input signal with its replica is shown in Fig. 4 for a time-interleaved by 2 modulator. When the input signal is out of the signal band, lying between $f_S/2M$ and $f_S/2$, a replica occurs in the signal band. In the continuous-time modulator with an anti-aliasing STF, this replica is attenuated in the signal band according to Fig. 5, and the modulator preserves its anti-aliasing qualities despite the additional replica signal (for an OSR of 10, the anti-aliasing filter is better than 60 dB for out-of-band interferers folding back into the signal band). Fig. 5 plots both the STF of the time-interleaved by 2 continuous-time modulator, as well as the replica transfer function. The x axis represents the frequency of the input signal, and the y axis represents the magnitude of the input signal and its replica at the output. Note that for an input frequency f_O, the graph plots the magnitude of the output signal as well as the magnitude of the replica signal. However, the frequency of the replica signal is not at the same input frequency; it is at $f_S/2 - f_{O,aliased}$, where $f_{O,aliased}$ is the aliased frequency of the input signal.

The transfer function from y_2 to w_1 contains a delay-free path with a gain of -3. This is the critical path of the modulator and the corresponding loop filter has been separated in Fig. 3 into the delayed path $L_6(s)$ and the delay-free path. This critical path results from the DTTI modulator shown in Fig. 2 where a path exists from the bottom quantizer to the top quantizer with no delay. Practically, this cannot be realized since it involves the instantaneous quantization of the signal in the bottom quantizer, and the instantaneous transmission of this quantized signal to the top quantizer, which is then quantized at the same instant. In the discrete-time approach realized by [6], the two phases of the sampling clock allow both quantizers to be sampled on alternate clock phases, eliminating this problem. In the continuous-time case, the entire pulse fed back by the DAC is integrated, and

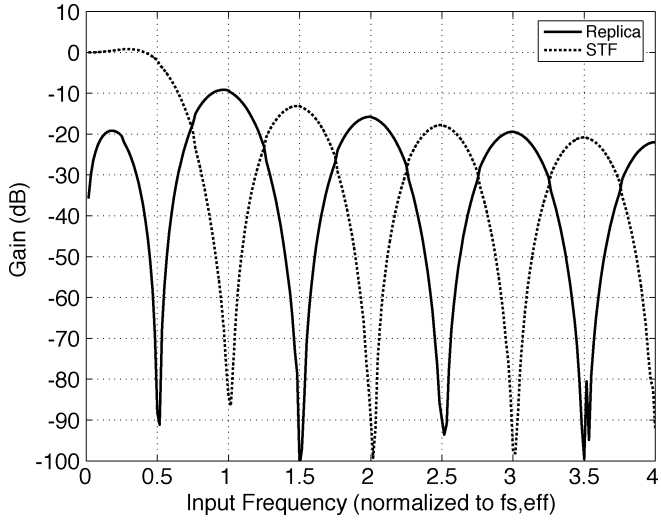

Fig. 5. Signal transfer function and replica transfer function.

thus the clocking of the feedback pulse must be adjusted. This is accomplished by reducing the width of the DAC pulse using RZ DACs, and clocking the ADCs at different times with corresponding offset RZ DACs. This allows the bottom ADC to quantize its input, and then send it to the summer at the input of the top ADC, which then quantizes its value slightly after the quantization in the bottom ADC. Following this, the top DAC then outputs its signal with a RZ pulse. The zero-delay path problem can be eliminated as long as enough time between the two clocks of the two quantizers is given for the bottom ADC to quantize its value, the bottom DAC to convert its signal, and for the summer to add the bottom RZ DAC signal to the top modulator signal. The timing for this solution is shown in Fig. 6 where the clocks of the quantizers are offset by $T/2$ seconds (where $2T$ is the sampling period of the time-interleaved modulator), while their respective DACs feedback the signals for a duration of T seconds, waiting $T/2$ seconds after their respective quantization is performed (to eliminate any excess loop delay). The symbol Q in Fig. 6 represents when the quantization is performed in the respective top and bottom branches. The loop filters $L_1(s)$ to $L_8(s)$ must accommodate the shape of the RZ feedback pulses. Referring to Fig. 3 and Fig. 6, the top DAC pulse is nonzero from T to $2T$ with the top ADC quantizing at $T/2$, $5T/2$, $9T/2$, etc., and the bottom DAC pulse is nonzero from $T/2$ to $3T/2$ with the bottom ADC quantizing at 0, $2T$, $4T$, etc. Since the top ADC is operating $T/2$ seconds after it normally would, an extra delay block of $T/2$ seconds has been added to the signal entering the top ADC (represented by $\Delta T/2$ in Fig. 3).

C. Final CTTI ΔΣ Modulator Structure

To complete the derivation of the CTTI $\Delta\Sigma$ modulator, the modulator of Fig. 3 must be modified to a more practical structure. The modulator can be manipulated to a structure similar to that of Fig. 2 as a cascade-of-integrators feedback (CIFB) structure with 6 continuous-time integrators (this can be accomplished where each order of the modulator is replaced with a structure similar to the left side of Fig. 7, where each integrator also includes a bypassing gain coefficient which is the general

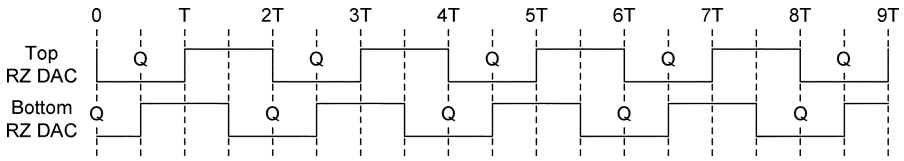

Fig. 6. Return-to-zero DAC clocking scheme.

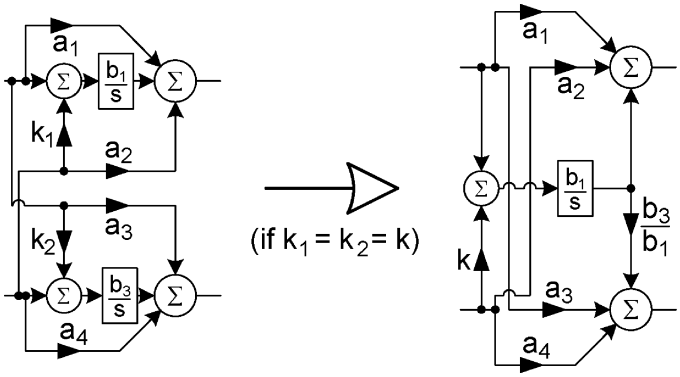

Fig. 7. Equivalency for integrator reduction.

form of the continuous-time equivalent of a delayed or nondelayed discrete-time integrator). However, a few simplifications have led to an even simpler modulator structure. Only two distinct paths exist from the input of the modulator to the input of both the top and bottom ADCs, and so filters $L_1(s)$ and $L_2(s)$ as well as filters $L_3(s)$ and $L_4(s)$ can be combined to reduce the complexity of the input loop filters. Furthermore, the equivalence shown in Fig. 7 can be used for each order of the modulator to reduce the number of integrators by two. Each bypassing gain coefficient in the integrators can be collected at the input of a preceding integrator to eliminate these gains. After manipulation of the modulator structure of Fig. 3, the modulator shown in Fig. 8 is obtained where only a single path of integrators remain. This simpler modulator structure is equivalent to that of Fig. 3, and it demonstrates that time-interleaving in the continuous-time domain does not necessarily require the doubling of complexity that the original DTTI $\Delta\Sigma$ modulator required. There only exists one integrator for each order of the modulator, as opposed to two integrators per order in the DTTI modulator. However, an extra $T/2$ second delay circuit and summation circuit (after the $T/2$ second delay) are required at the input of the top ADC, increasing the complexity slightly, but far less than doubling the number of integrators. The effects of DC offsets are mitigated by the single remaining path of integrators, a shortcoming in the DTTI design that used two parallel paths [6]. The final CTTI $\Delta\Sigma$ modulator has DACs and ADCs that operate at half the sampling frequency of the original discrete-time $\Delta\Sigma$ modulator of Fig. 2, while performing equally well.

Note that despite its appearance, this modulator is not just a conventional $\Delta\Sigma$ modulator with time-interleaved ADCs and DACs that quantize opposing samples. The bandwidth requirements on the integrators as well as the allowable DAC clock jitter are improved by almost a factor of 2 when compared to a conventional $\Delta\Sigma$ modulator because almost twice as much time $(2T)$ is allowed for the integrators to obtain their output values for both the top ADC and the bottom ADC. Even though only a single path of integrators remain through simplifications of the architecture, this modulator is superior to one that only time-interleaves the ADCs and DACs since it has this improved tolerance when operated at high speeds.

D. System Level Simulations of the CTTI $\Delta\Sigma$ Modulator

The new CTTI $\Delta\Sigma$ modulator can be compared to a conventional continuous-time $\Delta\Sigma$ modulator on the basis of several nonidealities, such as finite operational amplifier (opamp) gain, integrator coefficient mismatch, DAC mismatch, DAC feedback path mismatch and integrator DC offsets, as well as the high-speed considerations such as finite opamp bandwidth and DAC clock jitter. These nonidealities were modeled and simulated in the Matlab models of both the CTTI $\Delta\Sigma$ modulator and the conventional continuous-time $\Delta\Sigma$ modulator.

The CTTI $\Delta\Sigma$ modulator requires a DAC feedback path matching of at least 0.5% to obtain the desired 10-bit resolution, and the opamp DC gain must also be higher than in a conventional $\Delta\Sigma$ modulator due to this required matching. The DAC feedback path matching can be attained with proper layout. Similar integrator coefficient matching and DAC current cell matching is required in both the time-interleaved and conventional $\Delta\Sigma$ modulators. The CTTI $\Delta\Sigma$ modulator is more resilient than the DTTI modulator to DC offsets, but a regular continuous-time $\Delta\Sigma$ modulator is even more robust [11].

The CTTI modulator is superior to a conventional continuous-time $\Delta\Sigma$ modulator when operated at higher speeds. For the same input signal bandwidth (assuming similarly shaped RZ DAC pulses), the CTTI modulator obtains a signal-to-noise and distortion ratio (SNDR) of 64.0 dB with 3 ps RMS of DAC clock jitter, while the conventional continuous-time modulator has an SNDR of 60.0 dB with the same DAC clock jitter (DAC clock jitter is the dominant source of clock jitter in a continuous-time $\Delta\Sigma$ modulator since the ADC clock jitter is shaped by the NTF). The improved performance of the CTTI modulator occurs since the DAC clock jitter comprises half as much of the total period of the DAC pulse. Furthermore, in the presence of only finite opamp bandwidth, the CTTI modulator is more stable at higher sampling frequencies. With a unity-gain frequency of 1.5 GHz, the CTTI modulator can maintain 10-bit resolution up to an effective sampling frequency of 1 GHz, while the conventional continuous-time modulator is unstable beyond a sampling frequency of only 500 MHz. Also, the out of band peaking of the conventional modulator is much greater than that of the CTTI modulator, and as a result the CTTI modulator has improved resilience to out of band interferers that can cause the modulator to go unstable [11].

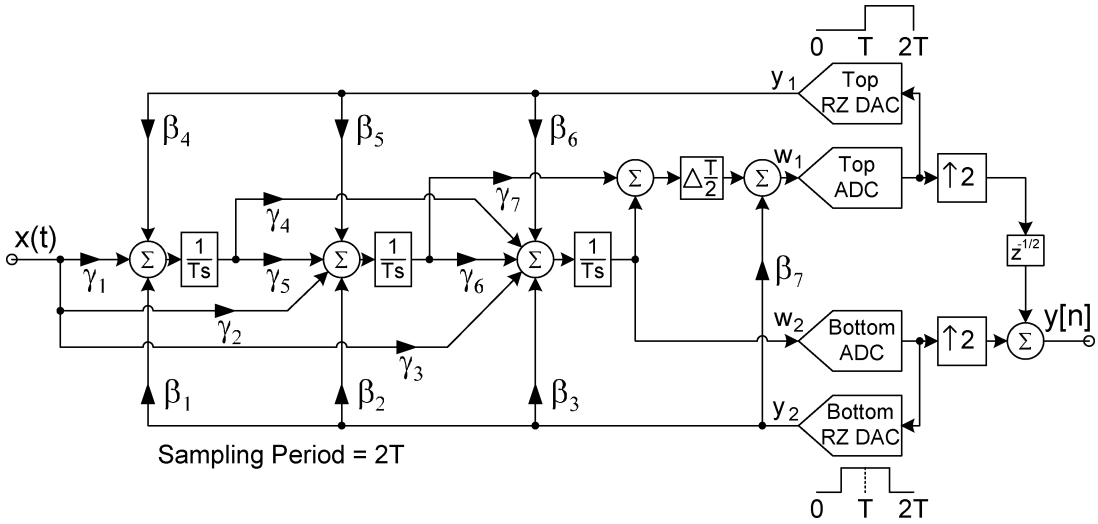

Fig. 8. Final time-interleaved continuous-time ΔΣ modulator.

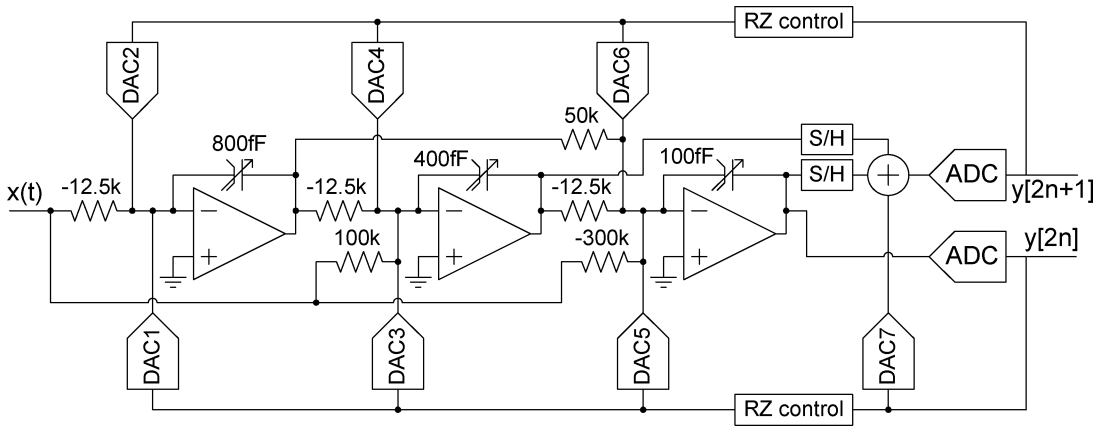

Fig. 9. General modulator circuit structure (capacitor values for 200-MHz operation).

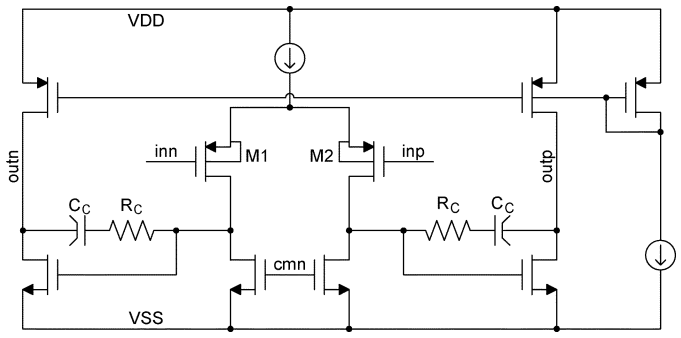

Fig. 10. Two-stage Miller compensated opamp.

III. Circuit Design and Implementation

The general structure of the new CTTI ΔΣ modulator is shown in Fig. 9 (a single-ended schematic is shown for simplicity). Opamps are used for the three active-RC integrators, current-mode DACs are used for the seven DAC feedback paths, 4-bit flash ADCs are used for the two quantizers, and transconductor cells are used in the summation circuit.

A. Integrators

The opamps are designed as Miller compensated two-stage opamps as shown in Fig. 10 with a unity-gain frequency of about 1.9 GHz and a DC gain of about 49 dB, as required by the system level Matlab simulations. The output swing of the opamps is about 1.6 V differentially. Each integrator stage consumes progressively less power since the integrating capacitance decreases as less accuracy is required. The two sampling frequencies of 100 and 200 MHz are made possible by an array of manually tuneable feedback capacitors in the integrators [12], which could be designed with an automatic tuning scheme if desired. Based on system level simulations, the tuning scheme is designed to match the nominal capacitor values to an accuracy of 2% while allowing for process variations of 20%, resulting in a 6-bit control signal for a binary weighted capacitor array. A continuous-time common-mode feedback circuit similar to the one presented in [13] is used where two 20-kΩ resistors sense the output common-mode voltage while negligibly loading the output stage due to the low output impedance of the second stage of the opamp. A reset switch is added across the tuneable capacitor array, and a start-up circuit is required since an undesirable state could occur after resetting the opamps where the output of

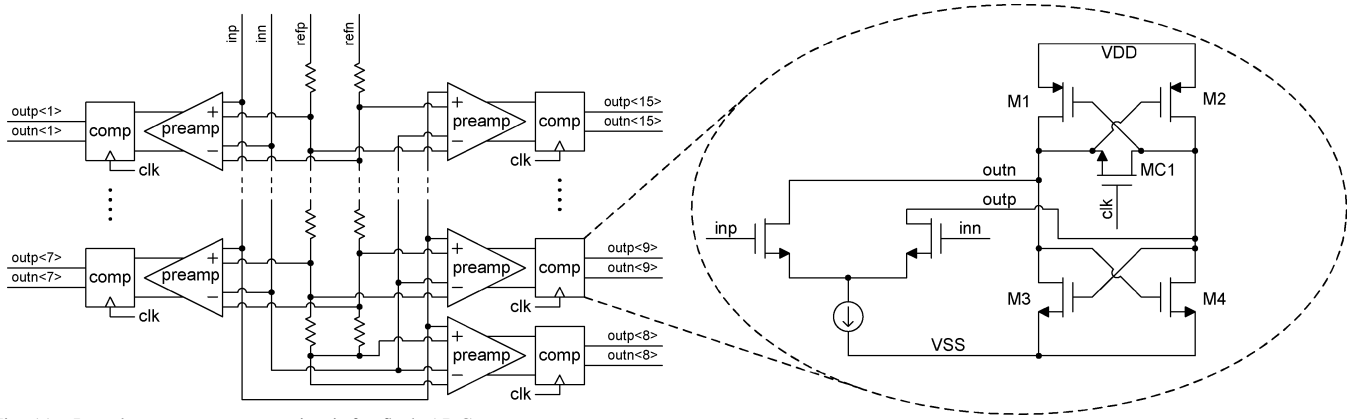

Fig. 11. Low-latency comparator circuit for flash ADC.

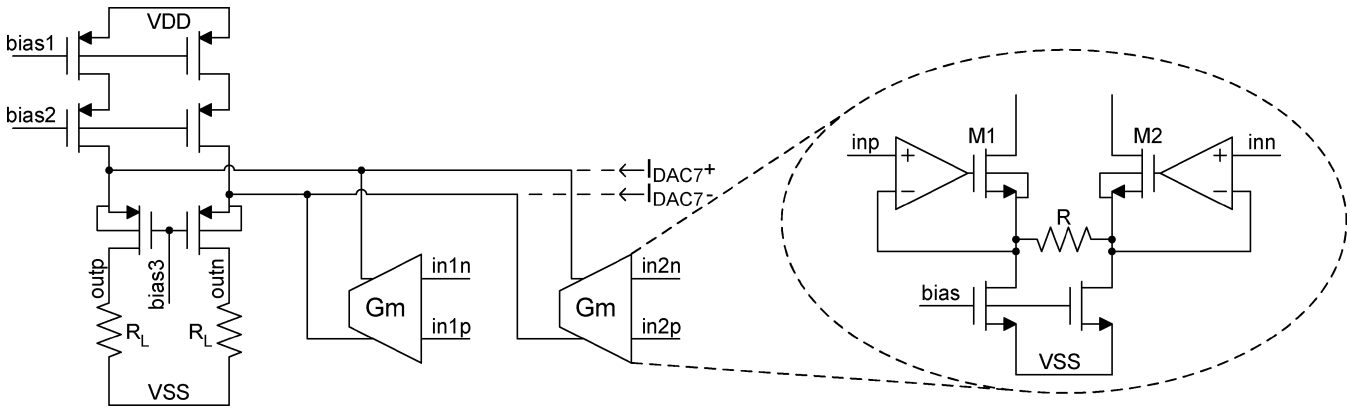

Fig. 12. Transconductor current summation circuit.

the opamp second stage would stay high while the output of the opamp first stage would stay low.

B. Digital-to-Analog Converters

Each DAC is composed of 15 current cells. The first and second current-mode DACs are sized to obtain the required 10-bit linearity in the current summed at the input of the modulator. The linearity requirements were met with sizing as opposed to dynamic element matching since 10-bit linearity can be achieved with reasonably sized transistors (higher linearity requirements would likely require dynamic element matching). The sizes are based on the sizing relationship of each current cell from [14]

$$W \times L = \left(\frac{2 \times A_{VT}}{|V_{GS} - V_t|} + A_\beta\right)^2 \Big/ \left(\frac{\sigma_I}{I}\right)^2 \qquad (6)$$

where V_{GS} is the gate-source voltage of the transistor, V_t is the threshold voltage of the transistor, σ_I/I is the normalized standard deviation of the current in each current cell, A_{VT} and A_β are process mismatch constants, and W and L are the desired width and length of the transistor. For the first and second current-mode DACs, $\sigma_{I1,2}/I_{1,2} = 0.0025$ with a 99% yield having a linearity better than 10 bits. The linearity requirements on each subsequent DAC decreases by about one to two bits. To reduce the required length of the transistors, pMOS current cells are used with a common-centroid layout and a $|V_{GS} - V_t|$ of at least 400 mV.

The zero-phase of the RZ DAC pulses is obtained by turning half of the DAC current cells on while turning the other half off, resulting in a zero net current entering the input of the opamps during the zero phase (note that the 15th current cell is split into two smaller current cells to realize an equal separation).

C. Analog-to-Digital Converters

The flash ADC is in the critical path of the modulator and it must have a very low latency. It is designed with a stage of preamplification followed by a comparator. The low latency is required because only $T/2$ seconds are available between the quantization in the bottom ADC and the quantization in the top ADC. The preamplifier utilizes two cross-coupled pMOS differential pairs with resistive loads to amplify the difference between the input signal and the corresponding reference voltage in the resistive ladder. It is sized based on the relation [15]

$$\sigma_{VT} = A_{VT}/\sqrt{2WL} \qquad (7)$$

where an acceptable standard deviation of the threshold voltage σ_{VT} was found with Matlab simulations to be 6 mV. The comparator in Fig. 11 operates very quickly since the voltage across the nonzero resistance of MC1 is already tipped in the proper direction during the track phase [16]. When the latch phase occurs, the back-to-back inverters (M1–M4) already have

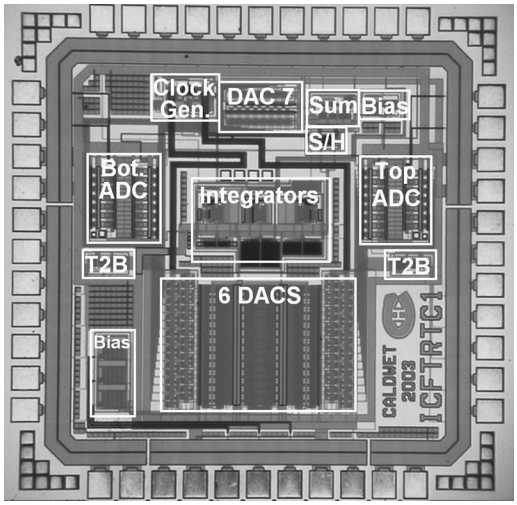

Fig. 13. Chip microphotograph.

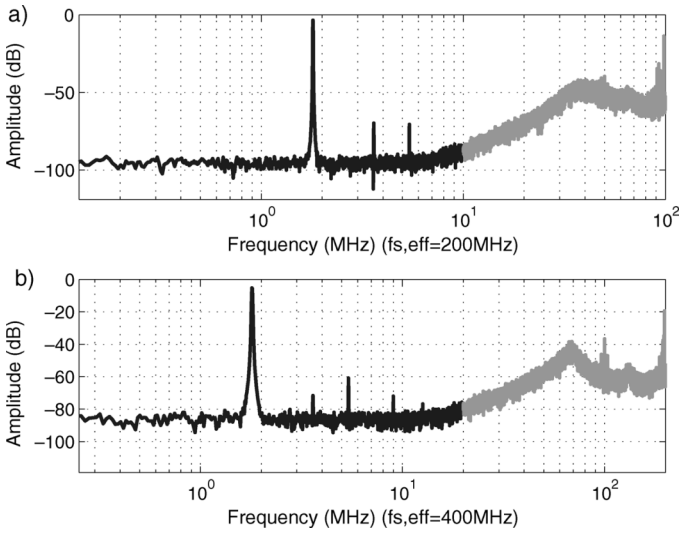

Fig. 14. Output spectra for 1.8-MHz input at sampling frequencies of (a) 100 MHz and (b) 200 MHz.

a starting point and continue to latch in the direction that the voltage is already tipped. The disadvantage of this comparator is that it consumes static power through M1–M4 in the track phase, thus increasing the power consumption of the flash ADC.

D. Summation Circuit

The summation in front of the top flash ADC (see Fig. 8) sums two voltages to one current and is shown in Fig. 12. The two voltages are converted to currents through two resistor degenerated transconductor cells, and they are summed to the DAC current and folded across a pMOS transistor to an output resistor to allow a higher swing in the output voltage, thereby reducing the size of the flash ADC preamplifier input transistors. The linearity of the transconductor is given by the following equation for the distortion of the third harmonic [17]:

$$HD_3 = \frac{1}{32}\left(\frac{1}{1+Ag_{m1,2}R}\right)^2\left(\frac{v_{inp}-v_{inn}}{V_{GS}-V_T}\right)^2 \quad (8)$$

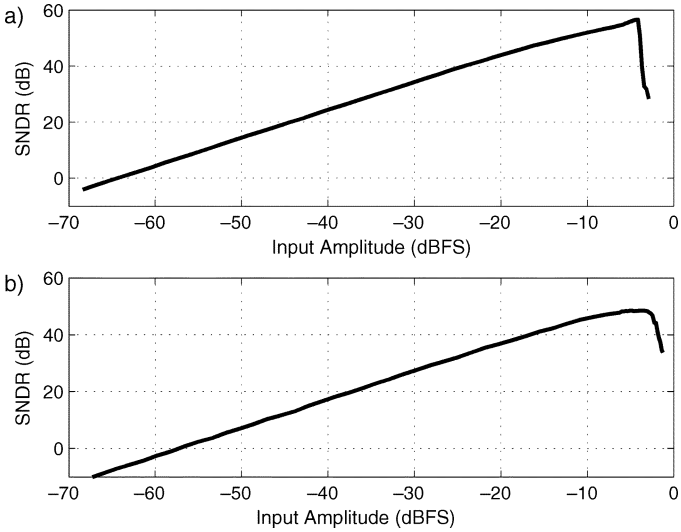

Fig. 15. Dynamic range plot for 1.8-MHz input at sampling frequencies of (a) 100 MHz and (b) 200 MHz.

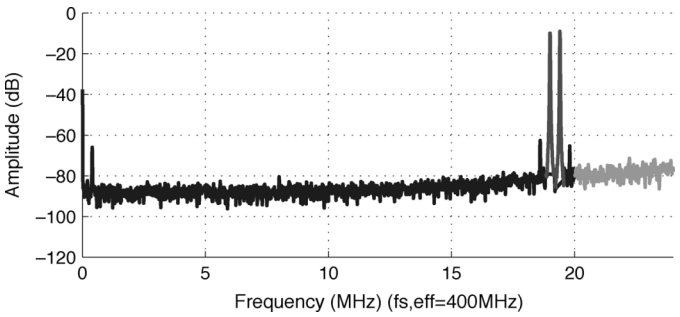

Fig. 16. Two-tone test with a 200-MHz sampling frequency.

where A is the gain of the amplifier, and $v_{inp} - v_{inn}$ is the 0.8-V input voltage swing. For the given transconductor the third harmonic is -50 dB which is more than sufficient at the input of a 4-bit quantizer. A parallel-sampling single transistor sample-and-hold circuit is used on the input of the summation circuit. Since the common-mode voltage is 0.7 V, the 1.8-V supply is sufficient for a 0.8-V peak-to-peak single-ended swing. Using an extra half-size dummy transistor to reduce the effects of charge injection, this circuit is able to achieve more than 5-bits of resolution, sufficient for the input to a 4-bit quantizer.

IV. Experimental Results

The CTTI $\Delta\Sigma$ modulator was designed and fabricated in a 0.18-μm CMOS technology with a 1.8-V supply. A chip microphotograph of the CTTI $\Delta\Sigma$ modulator is shown in Fig. 13. The active area of the chip is 1 mm^2. The SNDR, SNR, and the spurious-free dynamic range (SFDR) of the CTTI modulator were measured at sampling frequencies of both 100 and 200 MHz. Using various input frequencies and amplitudes, the output spectra and dynamic range plots were found.

Sample output spectra plots for both sampling frequencies are shown in Fig. 14 with a 1.8-MHz input signal, while the dynamic range plots are shown in Fig. 15. For the 1.8-MHz

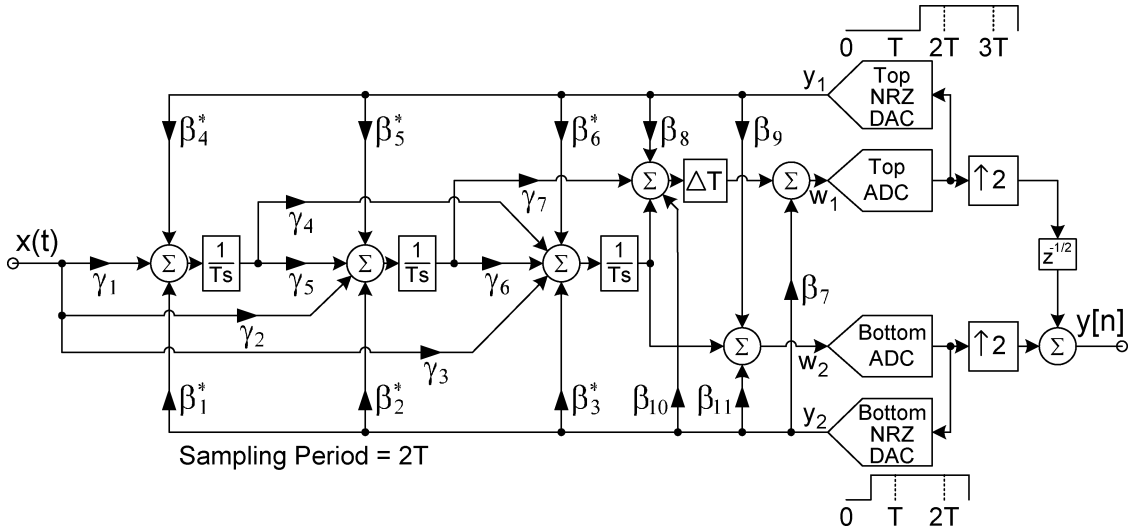

Fig. 17. M-CTTI modulator: CTTI modulator with additional DAC feedback paths.

TABLE I
EXPERIMENTAL RESULTS

Measurement	Sampling Frequency	
	100MHz	200MHz
Input	1.8MHz	1.8MHz
SNDR	57.2dB	48.8dB
SFDR	-66.2dB	-56.9dB
SNR	58.4dB	49.7dB
Dynamic Range	60.8dB	55.2dB
Analog Power	87mW	87mW
Digital Power	14mW	16mW
Power	101mW	103mW
Technology	0.18μm CMOS, 1.8V	
Chip Area	$1mm^2$	

TABLE II
ANALOG POWER BREAKDOWN

Circuit	Power
1st Opamp	14mW
2nd Opamp	10mW
3rd Opamp	8mW
Opamps (Total)	32mW
DACs (7)	2mW
ADCs (2)	36mW
Summer	7mW
Other (Biasing)	10mW
Total	87mW

input, the resulting SNDR was 57.2 dB and the dynamic range was 60.8 dB at 100 MHz, while the SNDR was 48.8 dB and the dynamic range was 55.2 dB at 200 MHz. A two-tone test was performed at a sampling frequency of 200 MHz with input signals at 19 MHz and 19.4 MHz to keep the third-order intermodulation products within the signal band at 18.6 MHz and 19.8 MHz. The output spectrum is shown in Fig. 16 where an SNDR of 48.3 dB was found. For the output spectra plots, the effective sampling frequency $f_{S,eff}$ is twice the actual sampling frequency (since the modulator is time-interleaved by 2). The results are summarized in Table I for an input frequency of 1.8 MHz. The total power consumption of the modulator was 101 mW at a sampling frequency of 100 MHz, and 103 mW at a sampling frequency of 200 MHz, and the analog power breakdown of the modulator is listed in Table II. About 35% of the overall power consumption was from the ADCs due to the low-latency requirements of the critical path.

The results degrade at the higher sampling frequency where more than one bit of resolution is lost. This is due to the critical path between the bottom ADC and the top ADC which must perform an analog-to-digital conversion, a digital-to-analog conversion, and a summation in 1.25 ns ($T/2$ seconds at 200 MHz, where $2T$ is 5 ns). This exposes the shortcoming of the design when trying to operate it at higher sampling frequencies, but a potential solution to this is presented in Section V. The results of this modulator are competitive with recent high-bandwidth $\Delta\Sigma$ modulators. It matches the highest input bandwidth obtained with recently published $\Delta\Sigma$ modulators, and has the potential to operate at a higher sampling frequency, as will be discussed in Section V. Table III summarizes the results of recent $\Delta\Sigma$ modulators with bandwidths of 10 MHz or more. Note that in [18], the results were inferred from the results of two modulators.

V. HIGH-SPEED IMPROVEMENTS

A. Extra Feedback Paths and NRZ DACs

In order to reduce the bandwidth requirements on the critical path as well as the DACs, nonreturn-to-zero (NRZ) DAC pulses are desired. The two DAC pulses could be extended into the adjacent clock period, however they would then change the impulse responses from the outputs of the DACs to the inputs of the ADCs. A technique presented in [22] demonstrates that in a conventional continuous-time $\Delta\Sigma$ modulator, an extra feedback path between the DAC and the ADC can be added to compensate for a DAC pulse that enters the adjacent clock period. Typically, this technique is used to combat excess loop delay in modulators with NRZ DAC pulses. Using this technique, the CTTI $\Delta\Sigma$ modulator can be modified with extra feedback paths that allow the DAC pulse to enter the adjacent clock period. Since this is a time-interleaved modulator, two feedback paths are required to compensate for both the top and bottom NRZ DACs that enter the adjacent clock period. Furthermore, the NRZ pulses can be

TABLE III
COMPARISON TO RECENT HIGH-BANDWIDTH (10 MHz+) ΔΣ MODULATORS

Paper	Technology	Architecture	Sampling Frequency	SNDR	Input Bandwidth	Power
[18]	0.13μm CMOS	1-2 Cascaded, DT	80MHz	50dB	10MHz	60mW
This Work	0.18μm CMOS	3rd Order, CT	100MHz	57dB	10MHz	101mW
[19]	0.18μm CMOS	2-2 Cascaded, CT	160MHz	57dB	10MHz	122mW
[20]	0.18μm CMOS	5th Order, DT	200MHz	72dB	12.5MHz	200mW
[21]	0.13μm CMOS	4th Order, CT	300MHz	64dB	15MHz	70mW
This Work	0.18μm CMOS	3rd Order, CT	200MHz	49dB	20MHz	103mW
[18]	0.13μm CMOS	1-2 Cascaded, DT	160MHz	50dB	20MHz	87mW

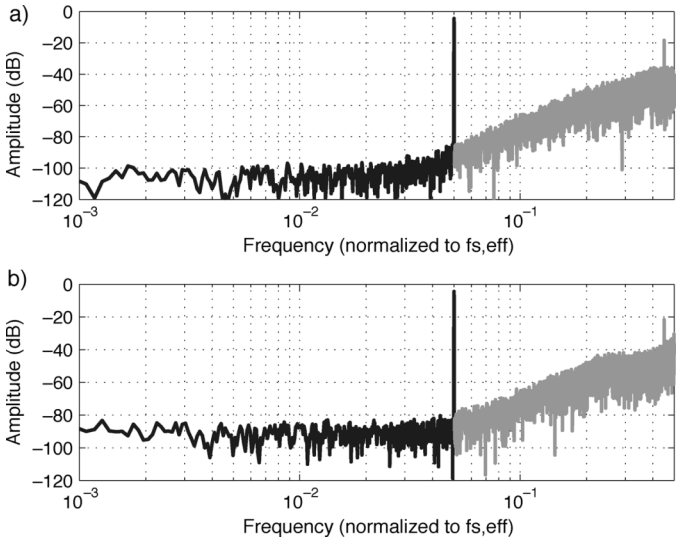

Fig. 18. Output spectra with high-speed nonidealities. (a) M-CTTI modulator of Fig. 17. (b) CTTI modulator of Fig. 8.

offset by T seconds instead of $T/2$ seconds, allowing more time for the critical path to complete its operation. These NRZ DAC pulses also increase the modulator's resilience to DAC clock jitter [23]. The resulting modified continuous-time time-interleaved (M-CTTI) $\Delta\Sigma$ modulator with the extra feedback paths and NRZ pulses is shown in Fig. 17 [24]. It requires an additional summation block and four extra low-linearity DACs, as well as a modification to the feedback coefficients (β_1 to β_6). To a first-order approximation, the new improvement halves the power consumption of the power-hungry flash ADC since the allowed latency of the critical path has been doubled.

B. Performance Comparison

Based on system-level Matlab simulations, the performance results of the modified M-CTTI modulator can be compared to the previous CTTI modulator for typical values. Simulated sample output spectra plots are shown in Fig. 18 where the opamp unity-gain frequency is 1.5 GHz (operating at the higher sampling frequency of 200 MHz), the DC gain is 50 dB, and the DAC clock jitter is 6 ps RMS (these values were chosen as the approximate values of the implemented CTTI $\Delta\Sigma$ modulator). The out of band peaking in the NTF in Fig. 18(b) is due to the finite bandwidth of the opamps, as well as the reduced DC gain, while the increase in the noise floor in the signal band is primarily due to the DAC clock jitter. The M-CTTI modulator has an SNR of 67.7 dB, while the CTTI modulator has an SNR of 59.2 dB [24]. It is clear from this comparison that based on simulations, the new techniques improve upon the CTTI $\Delta\Sigma$ modulator primarily due to the use of NRZ DAC pulses. The resolution of the M-CTTI modulator should be greater than the resolution of the CTTI modulator at the same sampling frequency, or it should achieve the same resolution as the CTTI modulator at double the sampling frequency.

VI. CONCLUSION

In this paper, it has been shown how a time-interleaved discrete-time $\Delta\Sigma$ modulator could be implemented as a continuous-time $\Delta\Sigma$ modulator. The derivation of the CTTI modulator was explained, and the modulator was simplified so that only one path of integrators remained, mitigating the effects of integrator DC offsets. Various nonidealities were investigated and it was concluded that the time-interleaved modulator is able to operate at a higher sampling frequency than a conventional $\Delta\Sigma$ modulator primarily due to its resilience to clock jitter, as well as its greater tolerance of lower bandwidth opamps. A third-order low-pass CTTI $\Delta\Sigma$ modulator with an OSR of 5 was then designed in a 0.18-μm CMOS technology. The modulator attained an SNDR of 57 dB at a sampling frequency of 100 MHz with a 10-MHz bandwidth, and an SNDR of 49 dB while operating at 200 MHz with a 20-MHz bandwidth. The power consumption of the modulator was 101 mW at 100 MHz, and 103 mW at 200 MHz. Improvements in the design have been suggested to enable operation at even higher sampling frequencies.

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