A High Bandwidth Power Scalable Sub-Sampling 10-Bit Pipelined ADC With Embedded Sample and Hold

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***Abstract*—A pipelined ADC architecture for use in sub-sampled systems which is power scalable in relation to its down sampled bandwidth is presented. The ADC uses a technique to eliminate the front-end sample hold, thereby reducing power consumption. The technique allows for a power savings of >20% compared to a previous design. A method to improve the settling behavior of rapid power-on opamps is also presented. Measured results in a 1.8 V 0.18 μm CMOS process verify the removal of the front-end sample and hold does not cause gross MSB errors for input frequencies higher than 267 MHz. With $f_s = 50$ MS/s, for $f_{\rm in} = 79$ MHz the SNDR is 51.5 dB, and with $f_s = 4.55$ MS/s for $f_{\rm in} = 267$ MHz the SNDR is 52.2 dB.**

***Index Terms*—ADC, CMOS, current modulated power scaling (CMPS), current starved, delay cell, pipeline, power reduction, power scalable, rapid power-on opamp, reconfigurable, sample and hold, scalable, sub-sampling.**

I. Introduction

THE growing demand for mobile systems which can provide multi-standard compatibility in a single solution [1] has stimulated much research in systems which allow for multiple design specifications to be met with only one low power design (e.g., [2]–[8]). All mobile communication systems consist of a receive path, in which it is typically required to down-convert a high frequency input down to an IF or baseband frequency. Fig. 1 illustrates a single path of an IQ receiver where an input mixer is used to translate an up-converted input signal down to baseband or a low IF. As the input signal is required to go through the mixer before the ADC, the mixer must have in-band distortion lower than that of the ADC and as a result the mixer can consume a large amount of power. Alternatively, the front-end mixer can be eliminated by connecting the output of the antialiasing filter directly to the ADC as shown in Fig. 2. By using sub-sampling in the ADC, the input bandwidth can be translated to an IF or baseband frequency (assuming the filter preceding the ADC sufficiently attenuates out of band harmonics). However, note that although the power of the mixer is eliminated in the approach of Fig. 2, the required input bandwidth of the ADC is significantly increased.

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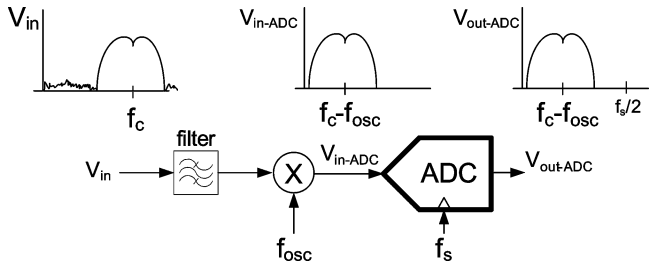

Fig. 1. Down-conversion using an input mixer.

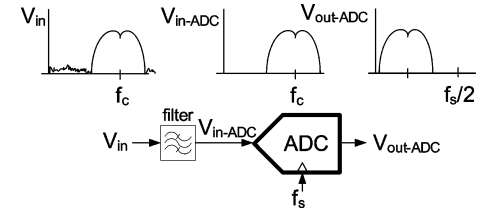

Fig. 2. Down-conversion using a sub-sampled ADC.

Fig. 3 illustrates the first stage of a pipelined ADC with the ADC input connected directly to a high frequency analog source. In a pipelined ADC the analog input is sampled by both the MDAC and sub-ADC, using different sampling circuits. Due to mismatches in the signal paths as well as threshold mismatches in the sampling switches, the analog input sampled by the sub-ADC and MDAC are different [9]. For a difference in effective sampling time between sub-ADC and MDAC of $\Delta_{\rm skew}$, and an input sinusoid with frequency $f_{\rm in}$, and peak voltage $V_{\rm peak}$, the maximum difference in input voltage sampled by the MDAC and sub-ADC is given by

$$V_{\rm skew-max} = 2\pi f_{\rm in} \Delta_{\rm skew} V_{\rm peak}. \quad (1)$$

For very large input frequencies the MDAC and sub-ADC can sample vastly different inputs, resulting in massive harmonic distortion in the ADC output. For example, if an input sinusoid of 270 MHz is applied to a pipelined ADC which has a sampling skew of 140 ps between MDAC and sub-ADC, the difference between inputs sampled by the MDAC and sub-ADC can be as high as a quarter of the full scale voltage.

To ensure the sub-ADC and MDAC see the same input, a front-end Sample and Hold (S/H) is commonly used before the first pipelined stage so as to make the input to the first pipeline stage discrete time, thus independent of input frequency given sufficient settling time. Since a front-end S/H would be required

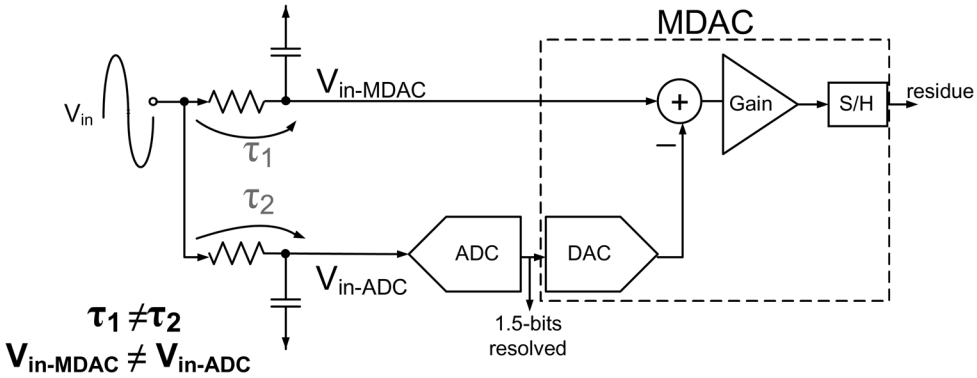

Fig. 3. First pipeline stage driven by input source.

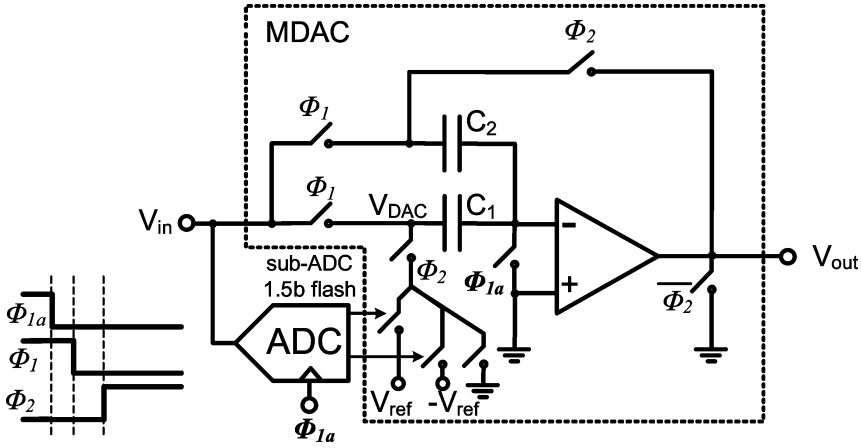

Fig. 4. Conventional 1.5b/stage MDAC.

to have a kT/C noise floor and distortion lower than that of the pipelined ADC following it, the power of the ADC is significantly increased by using a front-end S/H.

To save power, previous publications have eliminated the front-end S/H by relying on the redundancy of the first pipelined stage (e.g., [10]–[12]). In a 1.5-bit/stage architecture the comparator offset in the sub-ADC can be as large as $V_{\rm ref}/4$ (where $V_{\rm ref}$ is the maximum peak voltage of the input). Thus, so long as the difference in input operated on by the MDAC and sub-ADC of Fig. 3 is less than $V_{\rm ref}/4$, the effect of skew appears as an input-referred offset on the sub-ADC comparator, and the effect of the offset is eliminated by the redundancy of the first pipeline stage. Hence, the front-end S/H can be eliminated without any further modification to the ADC. From (1), assuming a sinusoidal input to the ADC with a maximum peak voltage, and assuming no inherent offset in the sub-ADC comparators, the maximum allowable skew time that can be corrected by the redundancy of a 1.5-bit stage is $(8\pi f_{\rm in})^{-1}$. Thus, high frequency inputs require low skew between sub-ADC and MDAC; for $f_{\rm in} = 270$ MHz the maximum skew allowable is 140 ps. The practical allowable skew between sub-ADC and MDAC however must also take into consideration the mismatch of the comparators in the sub-ADC (which in a 1.5-bit stage are typically made large) as well as a design safety margin—with these factors included the skew must be significantly lower than 140 ps. Clearly approaches which rely on the redundancy of the first pipeline stage require a very carefully matched layout [11] if the design is to work over all process corners and device variations.

In this work [13], a power scalable 10-bit ADC optimized for sub-sampled reconfigurable systems with large input bandwidths is proposed. By using a modified architecture for the first pipeline stage which does not require a front-end S/H nor carefully matched signal paths to prevent gross errors in the first stage, the power of the ADC is reduced by >20% compared to that in [3]. This work also presents a technique to improve the settling behavior of rapid power-on opamps which were shown in [3] to be a key building block in achieving power scalability for large sampling rates. Measured results from a prototype fabricated in a 1.8 V 0.18 μm CMOS process show the ADC of this work to have an SNDR of 51.5 dB at $f_{\rm in} = 79$ MHz for $f_s = 50$ MS/s, and SNDR of 52.2 dB at $f_{\rm in} = 267$ MHz for $f_s = 4.55$ MS/s.

The organization of the discussion in this paper is as follows: Section II describes the technique used to eliminate the front-end sample-and-hold, Section III describes how power scalability is achieved in this work, Section IV describes the circuit implementation of the design, Section V presents measurement results, and Section VI concludes the work.

II. Technique to Eliminate Front-End Sample-and-Hold

Fig. 4 illustrates a conventional 1.5-bit stage in a pipelined ADC. During Φ_1 the input is sampled on capacitors C_1 and C_2. During Φ_2 a gain of two is implemented by discharging the

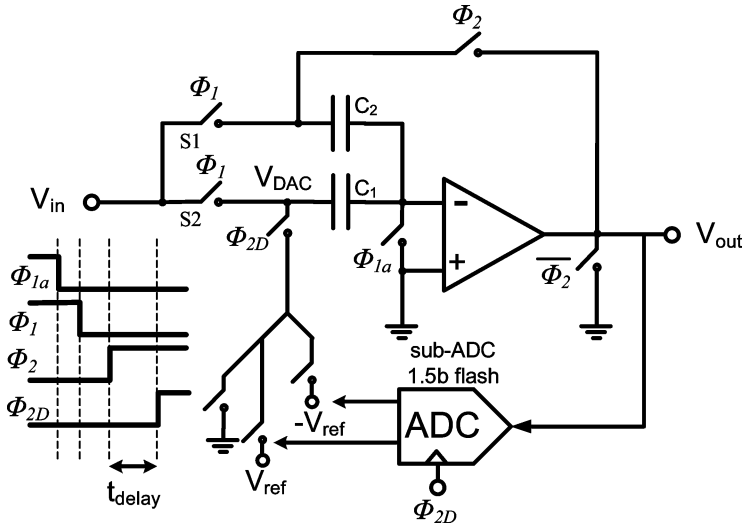

Fig. 5. MDAC of this work which enables elimination of front-end S/H (shown single-ended, but implemented fully differentially).

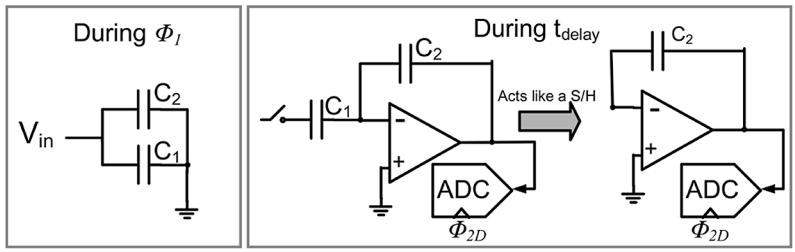

Fig. 6. Detailed illustration of MDAC functionality during $t_{\rm delay}$.

charge stored in C_1 to C_2, and DAC operation by connecting $V_{\rm DAC}$ to a voltage set by the sub-ADC.

In this work the first 1.5-bit pipeline stage is modified and an additional clock phase introduced as shown in Fig. 5. Like the conventional pipeline stage of Fig. 4, during Φ_1 the input is sampled on C_1 and C_2. However in this work, when Φ_2 switches from low to high and Φ_{2D} is low, $V_{\rm DAC}$ is set to a high impedance and C_2 is connected between the output and input of the opamp as shown in Fig. 6. Connecting C_2 around the opamp produces a held value of the sampled analog input, and due to charge conservation at the negative input of the opamp the voltage across C_1 is preserved as shown in Fig. 6. Thus, with the approach of this work, during the time labeled $t_{\rm delay}$ in Fig. 5, the output of the first stage can be connected to a 1.5-bit Flash ADC. When Φ_{2D} subsequently goes high the 1.5-bit Flash ADC resolves its input sets $V_{\rm DAC}$ to the appropriate DAC voltage, and implements a gain of 2x by discharging the charge from C_1 into C_2. Therefore, the first pipeline stage of this work implements the same functionality as a conventional pipeline stage, however is not sensitive to skew at the input as by using the embedded sample-and-hold of the MDAC, the sub-ADC operates on the same input that is sampled by the MDAC regardless of input frequency. Thus, by using the proposed modified first pipeline stage a front-end sample and hold is not required to ensure functionality for high input frequencies, hence allowing for substantial power savings.

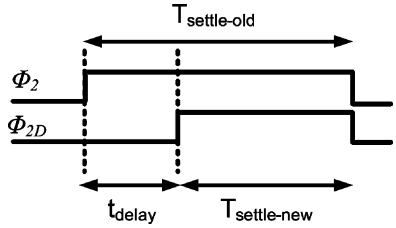

Fig. 7. Comparison of MDAC settling time of this work versus conventional MDAC.

Since the Flash ADC only requires an input that is >1.5-bit accurate, the output of the opamp during $t_{\rm delay}$ is only required to settle to >1.5-bit accuracy to generate the correct outputs from the Flash ADC, hence $t_{\rm delay}$ is only small fraction of the total available settling time as shown in Fig. 7. Although the power of the opamp in the first pipeline stage is slightly increased by the fraction of settling time taken by $t_{\rm delay}$, the overall power of the ADC is significantly reduced as the power hungry front-end S/H is eliminated. The technique to eliminate the front-end S/H could also be applied to multi-bit pipeline stages, noting that prior approaches which relied on redundancy to eliminate the front-end S/H have an even smaller allowable skew thus demand an even more meticulously matched layout than discussed in Section I. It should be noted that the technique to remove the front-end S/H, although independently derived

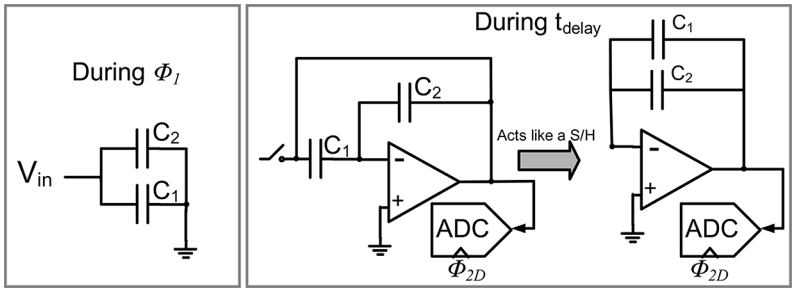

Fig. 8. Alternative configuration of MDAC during $t_{\rm delay}$ without floating capacitors.

for this work, is similar to that recently published in [14]. However the results of this work show: how the S/H removal technique can be applied to a power scalable architecture, a much higher input bandwidth, and a 66% increase in sampling rate.

From Fig. 6 it is noted that during $t_{\rm delay}$ one end of C_1 is floating. Alternatively it is also possible to configure the MDAC such that during $t_{\rm delay}$ node $V_{\rm DAC}$ is also connected to the output of the opamp as shown in Fig. 8. Using the alternative approach the functionality of the MDAC is the same as Fig. 5 however a floating capacitor is avoided. By using the approach of Fig. 8, the feedback factor of the MDAC during $t_{\rm delay}$ is increased, however the load capacitance seen by the opamp is also increased. Depending on the relative size of C_1 compared to the opamp input capacitance, the approach of Fig. 8 could yield a faster or slower solution compared to that in Fig. 6. To evaluate both approaches, a programmable switch was included in this work to allow the ADC to operate as shown in Fig. 6 or as shown in Fig. 8, so that the viability of each approach could be validated.

III. Power Scalability

A. Review of Prior Power-Scaling Techniques

Digital CMOS circuits have a power which explicitly scales with operating frequency according to $1/2fCV^2$. Analog circuits however have a power which by in large does not scale explicitly with sampling rate as static bias currents are used to place analog transistors in the active region. Since ADCs contain primarily analog circuits, the power of an ADC remains approximately fixed for different sampling rates. A common method to achieve a scalable analog power is to adaptively scale transistor bias currents with the sampling rate (e.g., [2], [15]–[17]). Since more settling time is made available for lower sampling rates, transistor bandwidths can be reduced hence bias currents correspondingly reduced. Although bias current scaling can be effective for a small variation of sampling rates, for a very wide variation of sampling rates the bias currents could be forced to vary by orders of magnitude to maintain a reasonable power consumption, thereby driving MOS transistors to be deep in the weak inversion region. As MOS transistors in the weak inversion region are more susceptible to mismatch effects than devices in strong inversion [18], in the interest of yield and sensitivity to external noise sources it is highly desirable to avoid operating deep in the weak inversion region. In [3] a current modulated power scaling (CMPS) technique was proposed which

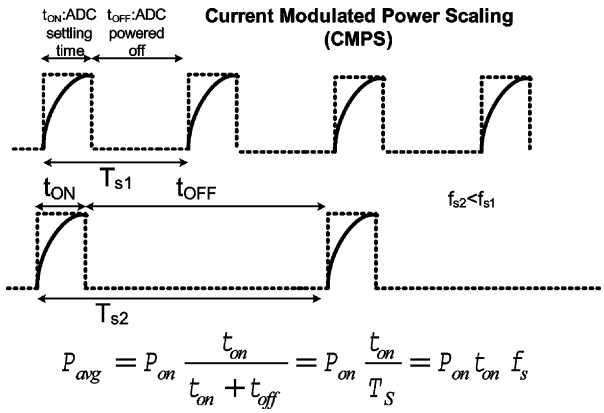

Fig. 9. Illustration of current modulated power scaling (CMPS).

allowed for very wide variations of power with sampling rate without commensurate variations in bias currents. The ADC of this work achieves power scaling using the techniques of [3]. Furthermore many of the circuits from [3] are re-used, where in this work the first pipeline stage is altered using the proposed techniques to allow for the elimination of the front-end sample-and-hold. Thus, the effectiveness of the power reduction techniques proposed can be evaluated by a direct comparison to [3].

B. Review of CMPS

As illustrated in Fig. 9, CMPS achieves power scaling by digitizing the analog input within a fixed time interval $t_{\rm ON}$, then powering off the ADC for $t_{\rm OFF}$ until the next input sample is required to be sampled. Thus, with CMPS, by changing how long the ADC is powered off, different sampling rates with linearly scaled power consumption (due to time averaging) are achieved. The settling times for each pipeline stage $(t_{\rm ON})$, hence bias currents, are thus constant for different sampling rates.

From [3], it is noted that when the pipelined ADC completely powers off its stages are reset, hence when the next analog input is sampled the input is required to be processed by each pipeline stage before a valid digital output can be generated. As a result, when using CMPS in a pipelined ADC the ADC effectively operates as an algorithmic ADC, limiting the maximum sampling rate to $1/t_{\rm lat} = 4.55$ MS/s in this work (where $t_{\rm lat}$ is the total latency of the pipelined ADC). From [3] it is noted that the total latency $(t_{\rm lat})$ includes the delay of the pipeline stages as well as additional clock cycles required to initialize various voltages (e.g., bias, clock generator) before the ADC can process the

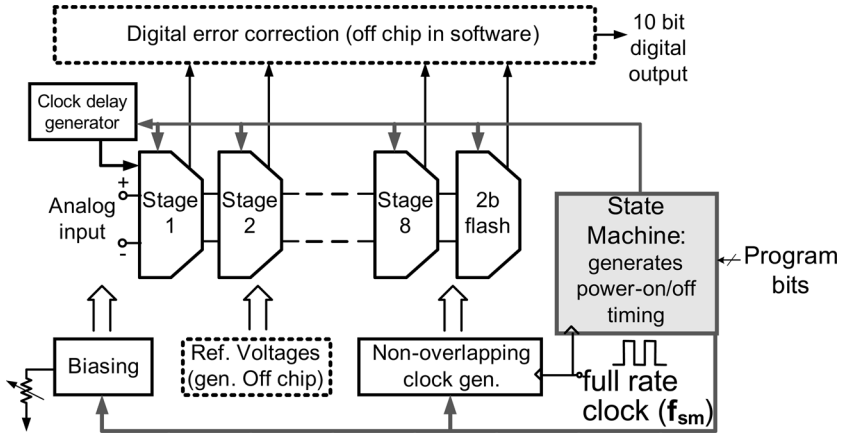

Fig. 10. Architecture of pipelined ADC.

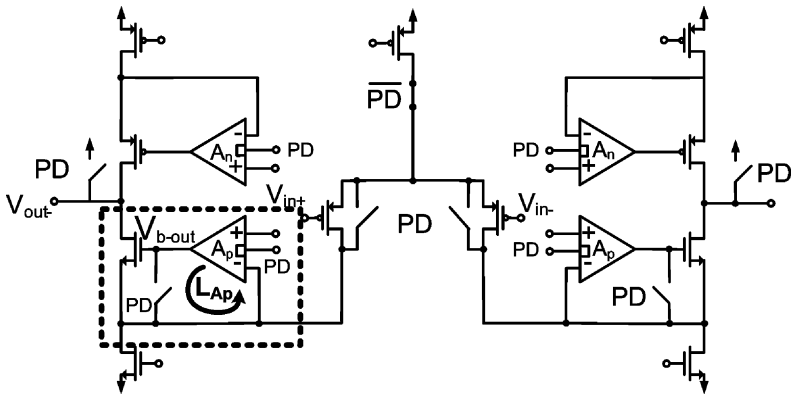

Fig. 11. Rapid power-on opamp.

next sampled input. Current scaling is used to achieve power scalability for sampling rates not covered with CMPS [3], i.e., between 4.55–50 MS/s. By using CMPS in combination with current scaling a very wide power scalable range can be realized without a commensurate variation in bias currents. This is highly desirable in sub-sampled systems as the system could be configured for different standards with widely different specifications, while having the power scale with bandwidth.

From [3] it is noted that to achieve high sampling rates, the ADC is required to rapidly power-on so as to digitize the next analog input. As a result analog circuits which are capable of rapidly powering-on and settling to the full accuracy demanded by the ADC are required. As opamps form the main analog circuit blocks in the pipeline stages of the ADC, rapid power-on opamps are required to enable CMPS at high sampling rates [3].

IV. Circuit Implementation

A. Pipeline Architecture

The architecture of the pipelined ADC of this work is shown in Fig. 10. The first stage is as shown in Fig. 5, and all remaining stages are standard 1.5-bit stages. Stages 3–9 are identical to those used in [3]. Stage 2 is a standard 1.5-bit stage but has the same sized sampling capacitors and opamp as stage 1.

With the front-end S/H removed in this work, the total sampling capacitances of the first two pipelined stages in this work were reduced by 40% compared to [3] (from 940 fF to 580 fF in stages 1, and 2) while maintaining the same input-referred noise as [3]. In this work the opamp of stage 1 was conservatively designed such that $t_{\rm delay}$ was 20% of the total settling time. However $t_{\rm delay}$ was made tunable so that the lowest $t_{\rm delay}$ possible without gross MSB errors could be measured. To meet the same settling accuracy as [3], the opamps of stage 1 and 2 were made 33% smaller than those of [3]. Thus, although less settling time is available in the first pipeline stage, overall power is still reduced without a front-end S/H since the thermal noise floor of the pipeline stages can be made higher (with smaller sampling capacitors) to maintain a fixed input-referred noise floor. To enable a large input bandwidth, bootstrapped switches [19] were used as the input switches S1, S2 in Fig. 5.

B. Rapid Power-on Opamp

A rapid power-on opamp [3] was used in each pipeline stage to realize a power scalable architecture and is shown in Fig. 11. Like conventional gain-boosted opamps, the rapid power-on opamp requires the unity gain frequency of the gain booster opamps (opamps A_p, A_n in Fig. 11) to be higher than the 3 dB frequency of the closed loop but lower than the second pole of the main opamp [20]. Furthermore the loop formed by the gain boosters (labeled L_{Ap} in Fig. 11) is also required to be stable. Rapid power-on opamps power on and completely off each clock cycle, hence the inputs to the gain booster opamps A_p, A_n effectively see a step function every clock cycle. Thus, to

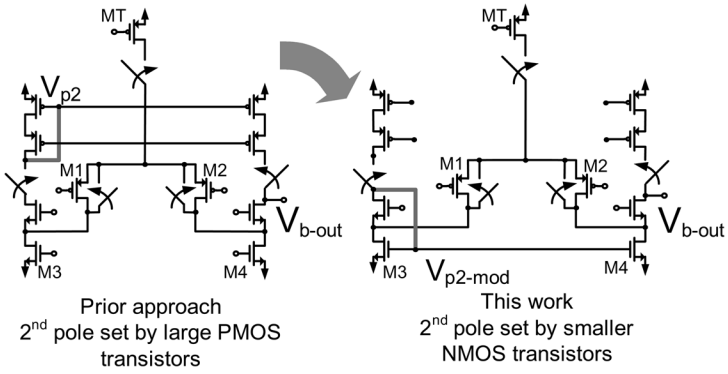

Fig. 12. Gain booster opamp used previously (left), and in this work (right).

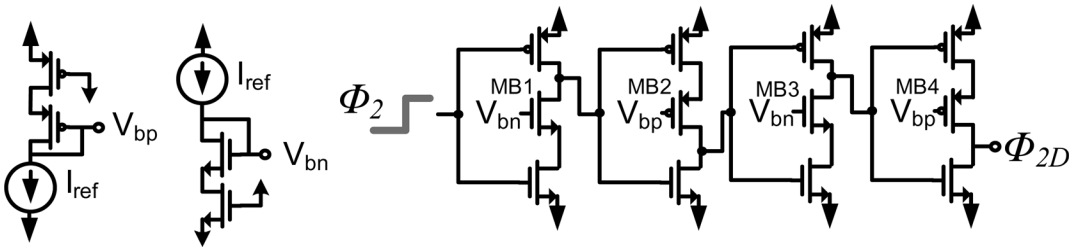

Fig. 13. Clock delay block to generate Φ_{2D} from Φ_2.

ensure good settling, loop L_{Ap} requires a high phase margin. In [3] standard folded cascode PMOS-input opamps as shown in Fig. 12 were used for the gain booster opamps A_p. The phase margin of the loop L_{Ap} is limited by the second pole of the loop which occurs at the pMOS current mirror node labeled V_{p2} in Fig. 12. The same bias voltages used for the main opamp were also used for the gain booster opamps, thus pMOS transistors were sized $\sim$ 5x larger than the nMOS transistors to maintain a similar overdrive voltage as the nMOS transistors for a fixed current density. As such a large parasitic gate-source and gate-drain capacitance exists on node V_{p2} and sets the second pole of the loop to a low frequency which degrades the phase margin of the loop L_{Ap}. To improve the phase margin of loop L_{Ap} the p-input gain booster opamp was modified by implementing the current mirror in the opamp with nMOS transistors instead of pMOS transistors [21] as illustrated in Fig. 12. By performing the mirror operation with nMOS transistors, the capacitance on the mirror node is reduced by $\sim$ 2.5x and the second pole pushed to a much higher frequency—significantly improving the phase margin. Simulation results show that the phase margin of loop L_{Ap} is improved from 56° to 72° by only changing the location of the mirror node. By switching the location of the current mirror node from pMOS to nMOS transistors the slew rate of the gain boosting opamp is reduced by 2x (i.e., when M2 is cutoff, in the prior approach the current through MT is mirrored by the pMOS current mirror to the output node, however in the approach of this work when M2 is cutoff the output current is set by M4 which is biased with half the current of MT). Although a lower slew rate increases the opamp's power-on time, the significant benefit of a more stable power-on transient makes it a favorable trade-off. Also it is noted that since the power-on time of the opamps of this work only require a small percentage of the settling time to power-on, the total available settling time of the opamp is not significantly reduced with a lower slew rate in the gain booster opamps.

C. Generation of Delayed Clock Φ_{2D}

The delayed clock edge Φ_{2D} of Fig. 7 was generated using a chain of four current starved inverters as shown in Fig. 13. Current starved inverters were chosen to allow $t_{\rm delay}$ to be widely tuned for different sampling rates by changing the bias currents. Also by varying the off-chip reference current $I_{\rm ref}$, the dependence of ADC SNDR versus $t_{\rm delay}$ could be measured.

The current starved inverters were designed such that only one clock edge was delayed. Commonly in a current starved inverter, the current sources are connected to the source nodes of the inverters (e.g., [22]–[24]) as shown in Fig. 14. When the input clock switches from low to high in, e.g., the first inverter, the current source initially starts off in triode causing a large drain-source current, which is different than the desired bias current, to flow until the pre-charged output discharges to the point where the current source is biased in the active region as shown in Fig. 14. As a result the discharge rate of the output also becomes a function of the rise time of the input, reducing the control $I_{\rm ref}$ has on the delay of the current starved inverter, hence reducing the range of delay values possible by varying $I_{\rm ref}$.

In this work, the current source transistors were connected between the drains of the pMOS and nMOS inverter transistors as shown in Fig. 14. This was done so that when the input to e.g., the first inverter switches from low to high, the current source transistor MB1 switches from operating in cut-off to the active region, forcing the inverter output to discharge with a rate set by the bias current of MB1. Hence, the discharge rate at the output of the inverter is a strong function of the biasing current of MB1 allowing wide variation in the delay of the inverter.

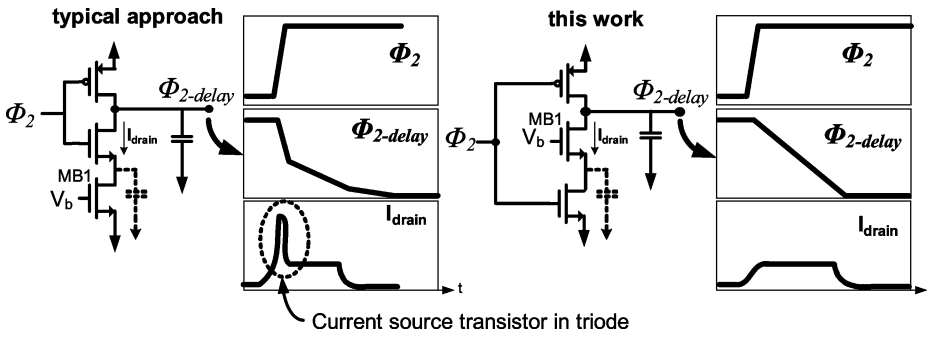

Fig. 14. Comparison of different current starved inverter topologies.

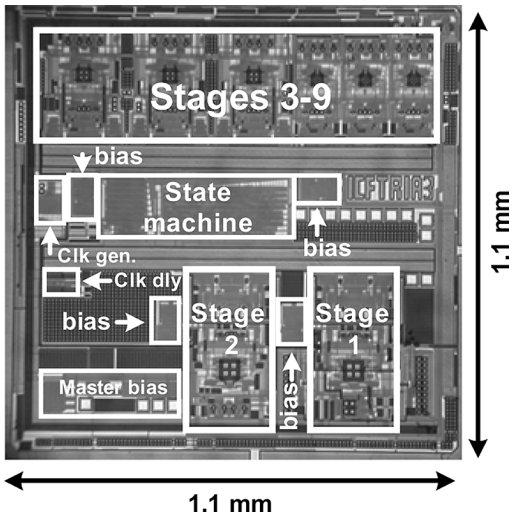

Fig. 15. Micrograph of fabricated chip in 1.8 V, 0.18 μm CMOS.

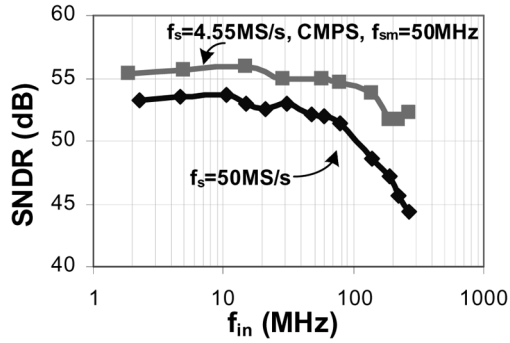

Fig. 16. SNDR versus input frequency for $f_s = 50$ MS/s, 4.55 MS/s.

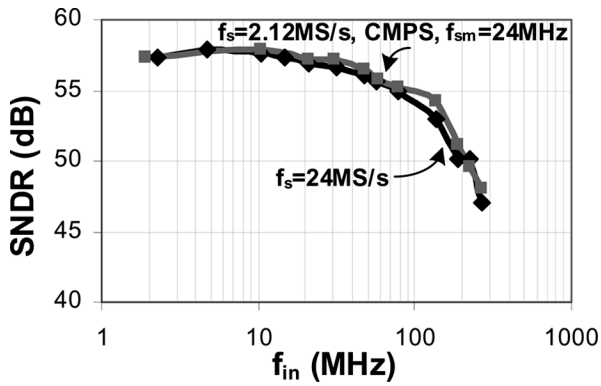

Fig. 17. SNDR versus input frequency for $f_s = 24$ MS/s, 2.12 MS/s.

The value of $t_{\rm delay}$ was set by an off-chip reference current $I_{\rm ref}$. In a practical system for use in industry where a precise definition of the duration of $t_{\rm delay}$ would be required to ensure sufficient settling times for the opamp over process and temperature variations, a DLL can be used to ensure a fixed $t_{\rm delay}$. Given a sufficient settling time, the clock edge of Φ_{2D} can be allowed to have a large amount of jitter without any significant impact on ADC performance. Hence, a potential DLL solution could be implemented with very low power. Furthermore since the most power consuming block of a DLL is typically the delay cell, which is already implemented on-chip in this work, the additional power of a loop filter, charge pump, and phase detector to complete the DLL loop would be relatively small.

V. Measured Results

A prototype of the ADC of this work as shown in Fig. 15 was fabricated in a 1.8 V, 0.18 μm CMOS process. The core area was 1.1 mm $\times$ 1.1 mm, and the maximum input signal swing was 1.6 Vp-p. Figs. 16 and 17 show the SNDR of the ADC versus input frequency for various power scaled sampling rates. The ADC remains fully functional for input frequencies larger than 267 MHz—frequencies which prior techniques using the redundancy of the first pipeline stage would require a very well matched layout ($\ll$ 140 ps skew). For $f_s = 50$ MS/s and $f_{\rm in} = 79$ MHz the SNDR is 51.5 dB. For lower sampling rates the input bandwidth is increased, e.g., for $f_s = 4.55$ MS/s, the SNDR is 52.2 dB for $f_{\rm in} = 267.1$ MHz. Fig. 18 shows the FFT of the ADC output for $f_s = 50$ MS/s and 4.55 MS/s. We note in this work the S/H removal technique is demonstrated for input frequencies $\sim$ 4x larger than in [14]. It is noted that the measurements for $f_s = 4.55$ MS/s are for the case when CMPS is enabled such that the settling time in each opamp as well as $t_{\rm delay}$ is the same as the case when $f_s = 50$ MS/s [3]. Also note that although a single sinusoidal input was used, distortion products are captured in the results due to aliasing from sub-sampling.

Fig. 19 shows the power of the ADC versus sampling rate. The power of the ADC at $f_s = 50$ MS/s was 27 mW, >20% lower than the 35 mW of [3] while maintaining a similar SNDR. It is noted in this work the 27 mW includes an additional bias circuit (1 mW) to improve the robustness of the system, as well

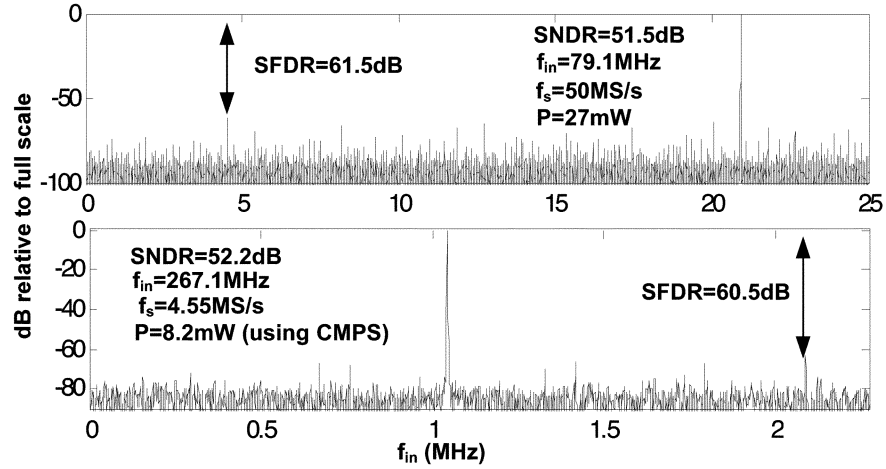

Fig. 18. FFT of ADC output at $f_s = 50$, 4.55 MS/s.

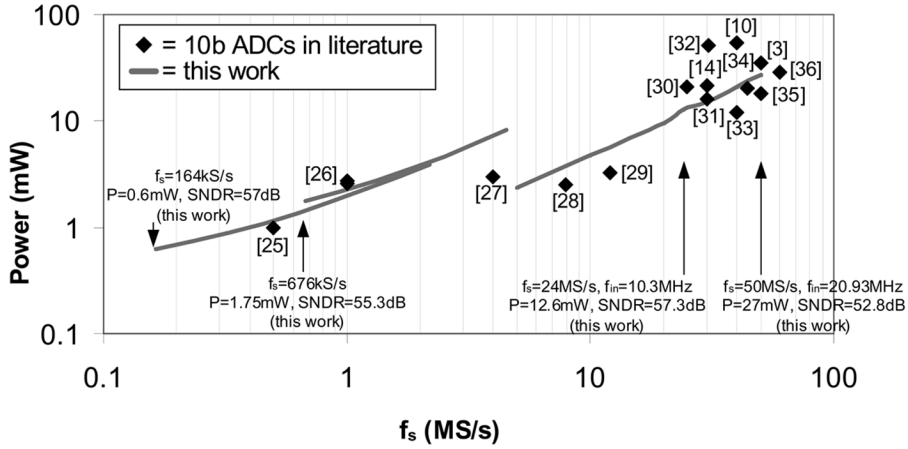

Fig. 19. Power versus sampling rate.

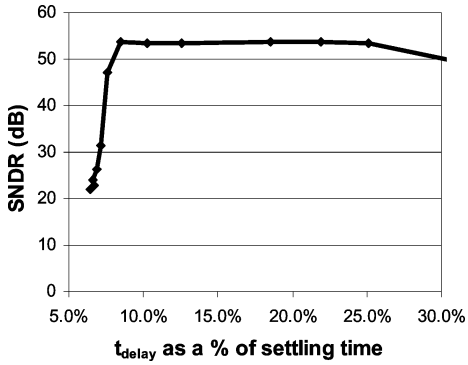

Fig. 20. Variation of ENOB with $t_{\rm delay}$ using approach of Fig. 6.

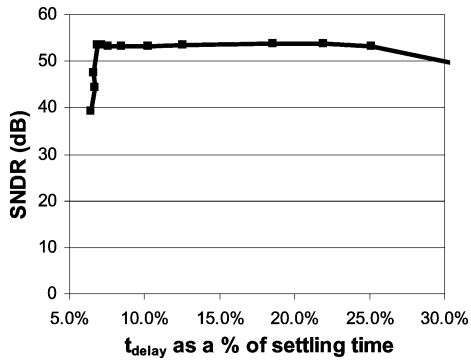

Fig. 21. Variation of ENOB with $t_{\rm delay}$ using approach of Fig. 8.

as clock delay generator (0.5 mW) to generate Φ_{2D}. Lower sampling rates with correspondingly lower power can be realized by increasing $t_{\rm ON}$ while current scaling the ADC [3]. From Fig. 19 the power of the ADC of this work is shown to compare favorably to other recently published 10-bit ADCs [3], [10], [14], [25]–[36] over a wide range of sampling rates.

In Figs. 20 and 21 the SNDR of the ADC is plotted versus the percentage $t_{\rm delay}$ is of the total available settling time when the first pipeline stage is configured using the approach of Figs. 6 and 8, respectively. From both plots it can be concluded that MSB errors only occur when $t_{\rm delay}$ is $<10\%$ of the available settling time. Thus, the technique to remove the front-end sample and hold described in this work does not require the first stage opamp to be significantly increased in power to maintain settling accuracy. Furthermore the fact that the SNDR only degrades for $t_{\rm delay}$ larger than 25% of the settling time indicates the power of the first stage opamp could easily be further reduced. Both approaches exhibit similar performance for different $t_{\rm delay}$, where

TABLE I
SUMMARY OF ADC PERFORMANCE

Technology	1.8V 0.18um CMOS
Sampling rates (fs)	<164kS/s - 50MS/s
Power	<0.6mW - 27mW
SNDR	> 51.5dB for all f_s
SFDR	> 60.5dB for all f_s
input frequency range	0 - 267MHz
Power of [3] @ 50MS/s	35mW
Power of this work @ 50MS/s	27mW

the approach of Fig. 8 shows better performance for slightly smaller values of t_{delay}. This can be attributed to the fact that although the load capacitance of the opamp in the first stage is increased using the approach of Fig. 8, for the opamp used in the first stage of this work, the larger feedback factor ultimately allows for faster settling. Table I summarizes the key measurement results of this work

VI. CONCLUSION

A power scalable ADC for use in sub-sampled systems with a large input bandwidth was described. Using a technique to remove the front-end sample and hold, a power savings of $>20\%$ was realized. A method to improve the settling behavior of rapid power-on opamps was also presented. Measured results from a 1.8 V 0.18 μm CMOS prototype show the ADC to achieve more than 51 dB SNDR for input frequencies larger than 79 MHz for $f_s = 50$ MS/s and 267 MHz for $f_s = 4.55$ MS/s.

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