Incremental Data Converters at Low Oversampling Ratios

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***Abstract*—In this paper the use of incremental A/D converters with low oversampling ratios is investigated. Incremental A/D converters are able to achieve a higher SQNR than delta-sigma modulators at oversampling ratios below 4, allowing them to operate as higher bandwidth converters with medium resolution. The impact of removing the input S/H, as well as analyzing their behaviour at an OSR as low as 1 is explored. An eighth-order cascaded incremental A/D converter is analyzed and shown as an example.**

***Index Terms*—Delta-sigma modulation, incremental analog-digital (A/D) converter, oversampled data conversion, switched capacitor circuits.**

I. Introduction

DELTA-SIGMA ($\Delta\Sigma$) modulation is a relatively simple means of performing data conversion. Since $\Delta\Sigma$ modulators oversample data, the input bandwidth is limited by both the *oversampling ratio* (OSR) and the maximum sampling frequency. The bandwidth of a $\Delta\Sigma$ modulator can be increased by decreasing the OSR, however this reduces the peak *signal-to-quantization noise ratio* (SQNR).

Incremental data converters operate on a similar principle to $\Delta\Sigma$ modulators but are reset periodically. To date, incremental data converters are generally used with a high OSR in applications where a high accuracy and low offset are required [1]–[3], and there has been some work to reduce this OSR with a hybrid architecture [4]. The purpose of this paper is to demonstrate that incremental *analog-to-digital* (A/D) converters can be used for medium resolution data converters with OSRs as low as 3. In this paper, Section II discusses the operation of incremental A/D converters while Section III describes their operation at low OSRs. Section IV presents a brief design example of a high-order low OSR incremental data converter, and Section V concludes the paper.

II. Understanding Incremental Data Converters

Incremental A/D converters are best understood as a combination of $\Delta\Sigma$ modulators and dual-slope A/D converters. They act like dual-slope A/D converters mixed in time, but also have the benefit of utilizing higher order architectures like $\Delta\Sigma$ modulators.

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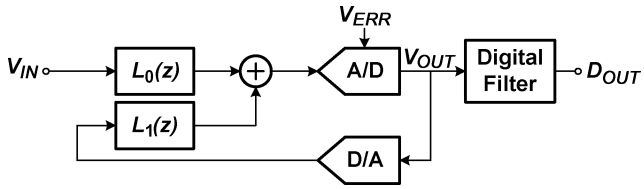


Fig. 1. General architecture of a $\Delta\Sigma$ modulator characterized by the two loop filters $L_0(z)$ and $L_1(z)$.

A. $\Delta\Sigma$ Modulators

$\Delta\Sigma$ modulators employ both oversampling and noise-shaping to improve the accuracy of a low-resolution (as low as 1-bit) internal A/D converter (or quantizer). The feedback loop allows the noise to be filtered using noise-shaping. Only a small portion of the frequency band is kept through filtering (based on the OSR) so very little noise remains within the signal band resulting in a very high-resolution A/D converter at the expense of reduced speeds. The *noise transfer function* (NTF) and the *signal transfer function* (STF) characterize the $\Delta\Sigma$ modulator. Referring to Fig. 1, the NTF is

$$\frac{V_{\rm OUT}}{V_{\rm ERR}} = \frac{1}{1 - L_1(z)} \tag{1}$$

while the STF is

$$\frac{V_{\rm OUT}}{V_{\rm IN}} = \frac{L_0(z)}{1 - L_1(z)}. \tag{2}$$

The order and shape of the transfer functions, the OSR, and the resolution of the internal A/D converter determine the resolution of the $\Delta\Sigma$ modulator.

B. Dual-Slope A/D Converters

Dual-slope (or integrating) A/D converters are useful for high-accuracy, high-linearity conversion with low offset and gain errors [5]. Shown in Fig. 2, the converter integrates the input signal for a fixed time and then subtracts a reference voltage for a counted number of clock periods until the output crosses zero. For an N-bit A/D converter, 2^{N+1} cycles are required for one conversion. For high-resolution A/D converters the conversion time can severely limit the speed at which they operate.

During the first phase when S_1 is on, the input $-V_{\rm IN}$ is integrated. After 2^N clock cycles (the entire S_1 phase), the output of the integrator will be

$$V_{\rm INT} = -\int_{-2^N T_s}^{0} \frac{-V_{\rm IN}}{RC} d\tau = \frac{V_{\rm IN}}{RC} \cdot 2^N T_s. \tag{3}$$

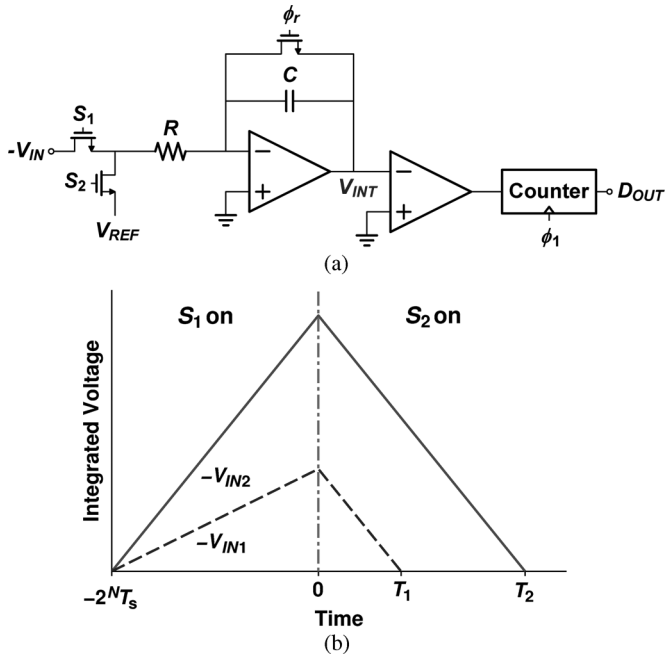


Fig. 2. Dual-slope A/D converter. Two sample input voltages are shown with their respective digital outputs T_1 and T_2. ϕ_1 is operating at the sampling frequency f_s. (a) Architecture. (b) Integrator output.

On the second phase, S_1 is off and S_2 is on. $V_{\rm REF}$ is then integrated until the voltage at $V_{\rm INT}$ goes to zero. The voltage at the output of the integrator during S_2 is

$$V_{\rm INT} = -\int_0^t \frac{V_{\rm REF}}{RC}dt + \frac{V_{\rm IN}}{RC}\cdot 2^N T_s. \tag{4}$$

After t seconds, the voltage is

$$V_{\rm INT} = \frac{V_{\rm IN}\cdot 2^N T_s - V_{\rm REF}\cdot t}{RC}. \tag{5}$$

This voltage is zero when

$$t_X = \frac{V_{\rm IN}}{V_{\rm REF}}\cdot 2^N T_s. \tag{6}$$

It is clear from this equation that the time t_X when $V_{\rm INT}$ crosses zero is proportional to the ratio of $V_{\rm IN}/V_{\rm REF}$ discretized in steps of T_s, where T_s is the time-domain LSB of the N-bit output.

If $V_{\rm IN}$ has a frequency dependent component $V_{{\rm IN},\sim}$ along with a constant input $V_{{\rm IN},-}$, then the output of the first integration phase is

$$\begin{aligned} V_{\rm INT} &= \int_{-2^N T_s}^{0} \frac{V_{\rm IN}}{RC}d\tau \\ &= \int_{-2^N T_s}^{0} \frac{V_{{\rm IN},-} + V_{{\rm IN},\sim}}{RC}d\tau \\ &= \frac{V_{{\rm IN},-}}{RC}\cdot 2^N T_s + \int_{-2^N T_s}^{0} \frac{V_{{\rm IN},\sim}}{RC}d\tau. \end{aligned} \tag{7}$$

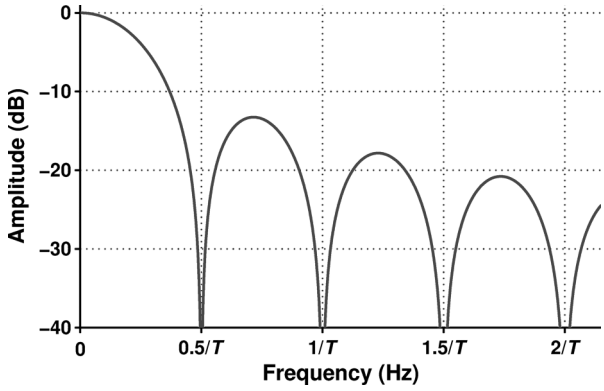


Fig. 3. Function $AT\sin(\omega T)/\omega T$ (the peak amplitude AT is normalized to 0 dB). The spectral nulls are evident at integer multiples of π for the argument ωT. For the dual-slope A/D converter, $T = 2^N T_s$.

The last term in (7) is zero only if the frequency dependent component $V_{{\rm IN},\sim}$ has an integer number of cycles in $2^N T_s$ seconds. Otherwise, some part of $V_{{\rm IN},\sim}$ will alter the desired voltage at $V_{\rm INT}$. This can be seen by assuming one of the frequency dependent components of $V_{{\rm IN}\sim}$ is of the form $A\cos(\omega t)$. The integral of the last term will be

$$\begin{aligned} \int_{-2^N T_s}^{0} \frac{A\cos(\omega t)}{RC}d\tau &= \frac{A\sin(\omega 2^N T_s)}{\omega} \\ &= \frac{A\cdot 2^N T_s \sin(\omega 2^N T_s)}{\omega 2^N T_s}. \end{aligned} \tag{8}$$

This function is plotted in Fig. 3 where the period is $T = 2^N T_s$. When ω is equal to integer multiples of $1/T = 1/2^N T_s$, the frequency dependent signal $V_{{\rm IN}\sim}$ is suppressed by the nulls in the spectrum. For non-integer multiples of $1/2^N T_s$, the signal $V_{{\rm IN}\sim}$ will not be suppressed and will affect the final output of the dual-slope A/D converter. This identical concept will be seen in the incremental A/D converter when the *sample-and-hold* (S/H) is removed.

C. First-Order Incremental A/D Converters

The architecture of an incremental A/D converter is similar to that of a $\Delta\Sigma$ modulator except the integrators are reset after each conversion, the input is held for each conversion,[1] and the decimation filter is different. However, a first-order incremental A/D converter is better understood as operating like a dual-slope A/D converter since the input/output relationship is identical when the S/H is removed. Also, like a dual-slope A/D converter (and similar to a Nyquist-rate A/D converter), input signals that fall between $f_s/(2\cdot OSR)$ and $f_s/2$ alias back into the signal band and are not suppressed by the digital decimation filter as they would be in a $\Delta\Sigma$ modulator.

A first-order incremental A/D converter is shown in Fig. 4. In contrast to a dual-slope A/D converter, the integration and subtraction of the reference signal are mixed in time. This is

[1]It is assumed that the input is held to attain the ideal behaviour of an incremental A/D converter, however this is not necessarily done in practice. Aside from the added power of a S/H, like the dual-slope A/D converter it can be advantageous to introduce spectral nulls at specific frequencies which is accomplished by using a moving input and adjusting the sinc decimation filter [6].

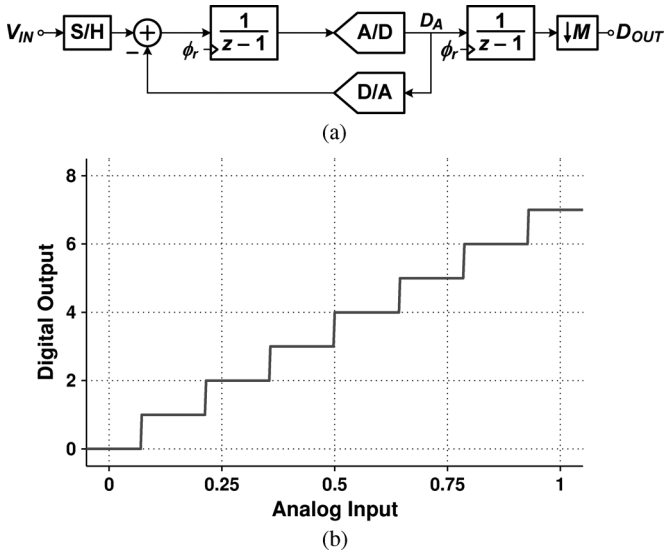


Fig. 4. Operation of a first-order incremental A/D converter with an OSR of 7 and a binary quantizer, resulting in 8 output levels. (a) Architecture. (b) Output versus input plot.

apparent if the 1-bit D/A converter output is either $V_{\rm REF}$ or 0 and the A/D threshold is $V_{\rm REF}$. Assuming a positive unipolar input, the held input is integrated until it is larger than $V_{\rm REF}$. At this point, $V_{\rm REF}$ is subtracted from the input, and the counter is incremented by 1. This continues for $2^N - 1$ clock cycles to obtain a resolution of N bits[2] (this is half as many clock cycles as a dual-slope converter because a 2-phase clock is being used). Once the conversion is performed (after OSR clock cycles), the integrator is reset, and the next sample is converted. An example of the output is shown in Fig. 4 for 7 cycles, resulting in a 3-bit or 8-level output. An added benefit to incremental A/D converters is the simplicity of the decimation filter. It can be as simple as a cascade of L accumulators for an Lth-order converter (as shown in Fig. 4), although more complicated filters can be used [6]–[8].

D. Higher Order Incremental A/D Converters

$\Delta\Sigma$ modulator design techniques can be applied to incremental A/D converters. If the OSR of an incremental A/D converter is defined as the number of cycles in one conversion, then it is clear that an increased OSR will increase the resolution. But unlike dual-slope A/D converters, incremental A/D converters can utilize higher order loop filters to further increase the resolution. Higher order incremental A/D converters can be implemented in either a single-stage structure, or a cascaded or MASH architecture.

1) Single-Stage Incremental A/D Converters: Single-stage architectures suffer from increased signal swings at the integrator outputs [1], but low-distortion input feed-forward architectures [6], [9] can be used to reduce these signal swings. Fig. 5 illustrates a second-order single-stage incremental A/D converter with an NTF of $(1 - z^{-1})^2$ and a bipolar input. The resulting output versus input characteristics are also shown for an OSR of 7, as well as the *differential non-linearity* (DNL) error. The single-stage architecture has 29 output levels, but

[2]An extra bit can be obtained with one extra cycle [1]. At high OSRs one extra clock cycle is insignificant, but for low OSRs the extra clock cycle can be costly.

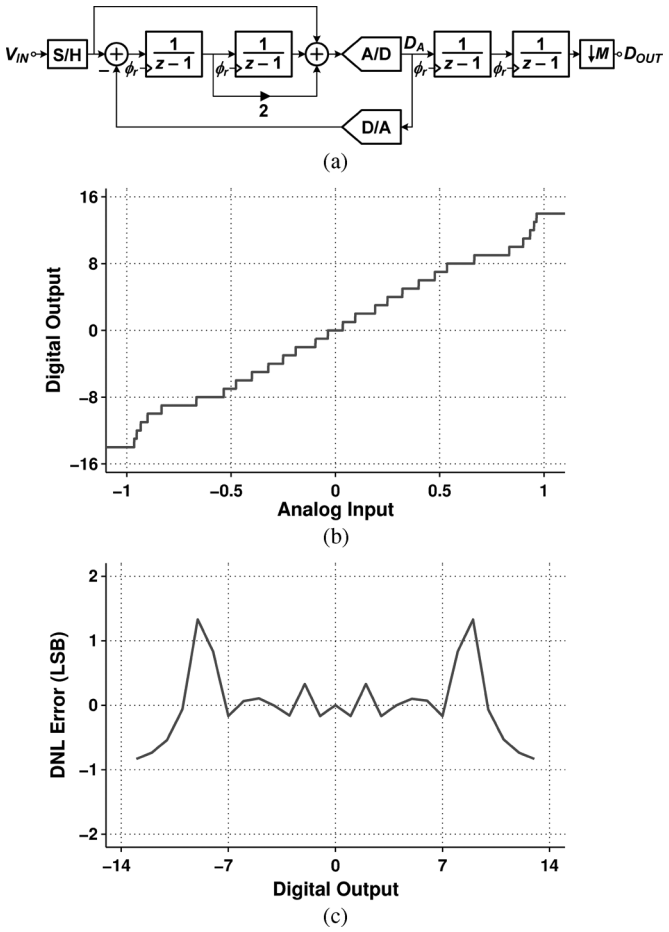


Fig. 5. Operation of a second-order single-stage incremental A/D converter with an OSR of 7 and a binary quantizer, resulting in 29 output levels. (a) Architecture. (b) Output versus input plot. (c) DNL error plot.

these levels are only suitable for inputs within ± 0.6. Beyond that, the DNL error is greater than 0.5 LSB. The DNL error occurs due to the restriction on the input signal amplitude for higher order incremental A/D converters in the same way that $\Delta\Sigma$ modulator states are only bounded for a given input signal amplitude.

For incremental A/D converters at high OSRs, the quantizer is guaranteed not to overload for an input range similar to $\Delta\Sigma$ modulators where [10]

$$\max|V_{\rm IN}| = \frac{N + 1 - \|h(n)\|_1}{N - 1} \tag{9}$$

for an N-level quantizer where $\|h(n)\|_1$ is the first norm of the NTF $H(z)$. For the second-order modulator of Fig. 5, $\|h(n)\|_1 = 4$ and it is clear that the input to a single-bit quantizer where $N = 2$ is never guaranteed to keep the quantizer input bounded unless the NTF is modified. When the converter input keeps the quantizer input bounded according to (9) (assuming an NTF of the form $(1 - z^{-1})^L$), the output will be identical to the ideal staircase output and the DNL will be zero. However, simulation can verify that the output may still have an acceptably low DNL in a larger range, as is the case for the single-stage architecture in Fig. 5.

For a single-stage architecture with an NTF of the form $(1 - z^{-1})^L$ (as well as a digital decimation filter with the same

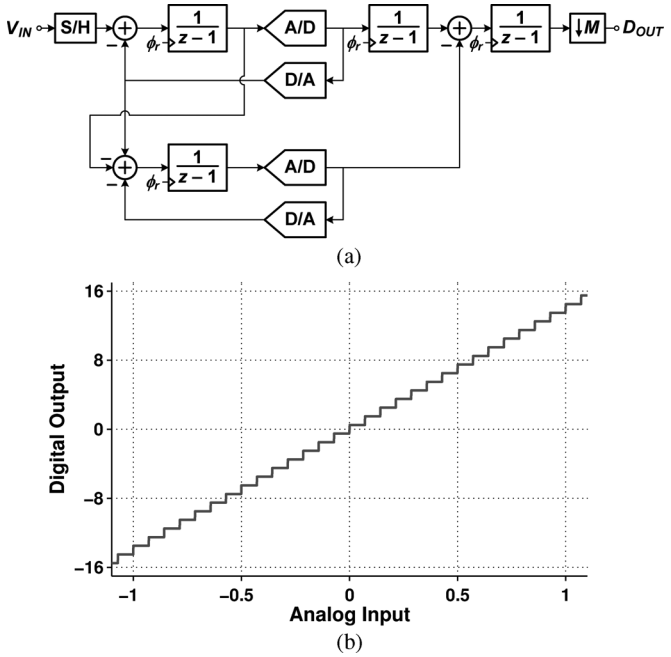


Fig. 6. Operation of a second-order cascaded incremental A/D converter with an OSR of 7 and binary quantizers, resulting in 32 output levels. (a) Architecture. (b) Output versus input plot.

transfer function), the resolution of the incremental A/D can be found using the following equation (see Appendix A)

$$6.02\log_2\left(\alpha(N-1)\frac{(M+L-1)!}{L!(M-1)!}+1\right)+1.76\text{ dB} \quad (10)$$

for an Lth-order converter with N quantizer levels and an OSR of M. The coefficient α is the maximum converter amplitude that keeps the quantizer input bounded and is usually less than unity.

2) Cascaded Incremental A/D Converters: Like $\Delta\Sigma$ modulators, the cascaded architecture is more stable for higher order converters. As opposed to feeding the output of the first integrator into the subsequent stage (as suggested in [1]), the first stage error can be fed into the following stage. This results in smaller signal amplitude being fed to the subsequent stage since it has less signal component, and facilitates the use of interstage gains and multi-bit quantizers to increase the SQNR.

Fig. 6 illustrates a second-order cascaded incremental A/D converter with an NTF of $(1-z^{-1})^2$. For the same NTF as in Fig. 5, the cascaded architecture has 30 output levels for an OSR of 7, and they form a perfect staircase output. Since an input amplitude as large as unity keeps the quantizer input bounded, no DNL error occurs for the entire input range.

It can also be seen that the input extends beyond unity and the perfect staircase is still intact. DNL errors result due to quantizer overload, but the quantizer in an incremental converter may not overload at lower OSRs since it is reset every OSR clock cycles, meaning that the accumulation responsible for quantizer overload is cut short, unlike in $\Delta\Sigma$ modulators. This allows slightly larger full-scale inputs than would be expected for an equivalent NTF of a $\Delta\Sigma$ modulator.

The MASH architecture that will be discussed in this paper is an Lth-order cascade of first-order stages with an NTF (and digital decimation filter) of $(1-z^{-1})^L$. The resolution of this particular MASH architecture can be computed as (see Appendix A)

$$6.02\log_2\left(\alpha(N-1)^L\frac{(M+L-1)!}{L!(M-1)!}+1\right)+1.76\text{ dB} \quad (11)$$

where M is the OSR, N is the number of quantizer levels and α is the product of the maximum converter input that keeps the quantizer bounded for each stage. Since the first-order incremental A/D converter does not overload with inputs as large as unity, α will be unity, or slightly larger. Eq. (11) assumes that an interstage gain of $N-1$ is used between cascaded stages.

E. Input-Referred Noise

Calculating the input-referred noise of an incremental A/D converter is quite different from a $\Delta\Sigma$ modulator. Every conversion has a weighting associated with each sample, and for higher order modulators earlier samples have a higher weighting than later samples because the digital filter has unequal weighting coefficients for higher order modulators [6]. The total input-referred noise power $\overline{v_n^2}$ is

$$\overline{v_n^2}=\sum_{i=1}^{M}w_i^2\overline{v_s^2}=\overline{v_s^2}\sum_{i=1}^{M}w_i^2 \quad (12)$$

where $\overline{v_s^2}$ is the input noise power of each sample, M is the OSR (and number of samples per conversion), and w_i is the weighting associated with each sample.

In a first-order modulator, assuming an accumulator as a decimation filter, the weighting factors are equal $(w_i=1/M)$ since the output is effectively an average of the M inputs added to the quantization noise error introduced. The resulting input-referred noise power is $\overline{v_n^2}/M$, as expected for an A/D converter oversampled by M. But as the modulator order increases this is no longer the case. For a second-order modulator with a 2-stage cascaded accumulating decimation filter, the weighting factors increase to

$$w_i=\left\{\frac{1}{M(M+1)/2},\frac{2}{M(M+1)/2},\ldots,\frac{M}{M(M+1)/2}\right\}. \quad (13)$$

The resulting total noise power is increased by a factor of up to 4/3 [6] since

$$\sum_{i=1}^{M}w_i<\frac{4/3}{M}. \quad (14)$$

At an OSR of 1, this reduces to the expected $1/M$, but for higher OSRs these higher order incremental A/D converters introduce more input-referred noise into the system when compared to $\Delta\Sigma$ modulators, to a maximum of 33% more.

The increased input-referred noise can be compared for modulators of various orders and OSRs, and the results are summarized in Table I. The results are normalized to the expected input-referred noise power of an oversampled A/D converter where the noise is $1/M$ for an OSR of M. It is clear that at high OSRs, lower order incremental A/D converters must be used to keep the input-referred noise power low. But when low OSRs

TABLE I
RELATIVE INPUT-REFERRED NOISE POWER FOR INCREMENTAL A/D CONVERTERS FOR INCREASING OSR AND ORDER

OSR	Order 1	2	4	8	12
1	1.00	1.00	1.00	1.00	1.00
2	1.00	1.11	1.36	1.60	1.72
4	1.00	1.20	1.69	2.32	2.68
8	1.00	1.26	1.93	2.99	3.74
16	1.00	1.29	2.09	3.51	4.67
32	1.00	1.31	2.18	3.85	5.35
64	1.00	1.32	2.23	4.05	5.77
128	1.00	1.33	2.26	4.15	6.00

TABLE II
COMPARISON OF SECOND-ORDER $\Delta\Sigma$ AND INCREMENTAL A/D AT LOW OSRS

OSR	Single-Stage, $N = 5$		MASH, $N = 3/3$	
	$\Delta\Sigma$	Inc.	$\Delta\Sigma$	Inc.
2	11 dB	24 dB	17 dB	26 dB
4	25 dB	33 dB	31 dB	35 dB
8	40 dB	44 dB	46 dB	46 dB
16	56 dB	54 dB	59 dB	57 dB

are used, there is a limit on the converter order to maintain a given noise power.

III. INCREMENTAL DATA CONVERTERS AT LOW OSRS

A. Single-Stage and Cascaded

Like $\Delta\Sigma$ modulators, cascaded incremental architectures have a much larger SQNR at low OSRs than single-stage architectures. But the reason is quite different, and this is why it is best to think of incremental A/D converters at low OSRs as operating distinctly from noise-shaping $\Delta\Sigma$ modulators.

When compared to $\Delta\Sigma$ modulators, incremental A/D converters will have one or more output levels for any non-zero values of L, M and N according to (10) and (11). Unlike $\Delta\Sigma$ modulators at low OSRs where noise shaping increases the total quantization noise power of the system [10], incremental A/D converters will always have a minimum resolution equal to the resolution of the quantizer, even at an OSR of 1 (which will be discussed in the next section).

Table II compares simulated SQNRs of a $\Delta\Sigma$ modulator and an incremental A/D converter at an OSR of 2, 4, 8 and 16 using an NTF of $(1 - z^{-1})^2$ with a second-order MASH architecture (with 3-level quantizers and an interstage gain of 2) as well as a second-order single-stage architecture (with a 5-level quantizer). At a low OSR of 2 and 4, the incremental A/D converter has a larger SQNR, while at an OSR of 8, the results are very similar. At higher OSRs of 16 and above, the $\Delta\Sigma$ modulator has a larger SQNR. These results motivate the use of incremental A/D converters instead of $\Delta\Sigma$ modulators at lower OSRs.

As another example, Fig. 7 shows a comparison of the SQNR at increasing OSRs for an eighth-order cascaded $\Delta\Sigma$, an eighth-order cascaded incremental A/D converter, and an 8-stage pipeline A/D converter. Each stage has a 3-level quantizer so the three converters are almost identical architecturally. As long as the OSR is less than 5.3, the incremental A/D converter has a higher SQNR than the other two architectures. Above an OSR of 5.3, noise-shaping in a $\Delta\Sigma$ modulator outperforms incremental A/D conversion. It is also interesting to note that a $\Delta\Sigma$ modulator only outperforms a pipeline A/D converter at OSRs greater than 2.5; at lower OSRs $\Delta\Sigma$ modulators increase the total quantization noise power to an extent that it is more beneficial to avoid noise-shaping altogether.

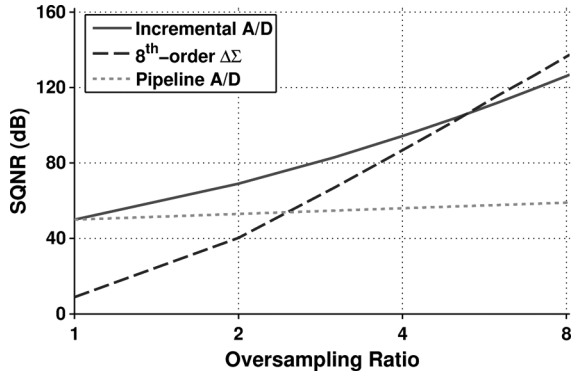


Fig. 7. Simulated SQNR versus OSR for three different architectures. All three A/D converters have the same internal 3-level quantizers. Simulations for the incremental A/D match equation (11).

Incremental A/D converters and $\Delta\Sigma$ modulators operate on different principles because the loop filter is reset and the input is held in an incremental converter. Since the incremental A/D converter has less noise than a $\Delta\Sigma$ modulator at an OSR of 1 due to the increased noise power from noise-shaping, it should not be surprising that the incremental A/D converter outperforms the $\Delta\Sigma$ modulator up until the OSR where noise-shaping begins to improve the $\Delta\Sigma$ modulator's resolution. Another reason for the increased resolution (as mentioned in Section II-D) is the larger allowable signal amplitudes. Since an incremental A/D converter resets after OSR clock cycles, the memory of previous conversions is lost, and thus a sustained large signal has only OSR clock cycles to accumulate in the integrator to overload the quantizer. Therefore, while a $\Delta\Sigma$ limits the signal amplitude at low OSRs as it would at high OSRs, an incremental A/D converter at low OSRs allows larger signal amplitudes than at high OSRs since there are fewer cycles for the signal to accumulate. This can contribute a few extra dB of resolution as the OSR is lowered.

At an OSR of 3, these three architectures can also be compared while varying the number of stages. The results are shown in Fig. 8. At this OSR the incremental A/D converter outperforms the $\Delta\Sigma$ modulator and pipeline A/D converter.

B. Pipeline Equivalency

As pointed out in the previous section, even with an OSR of 1, at very least the incremental A/D converter still resolves the input signal with the internal quantizer. If a cascaded incremental A/D converter is used, (11) predicts $\alpha(N-1)^L+1$ output levels for an Lth-order converter with N-level quantizers. This

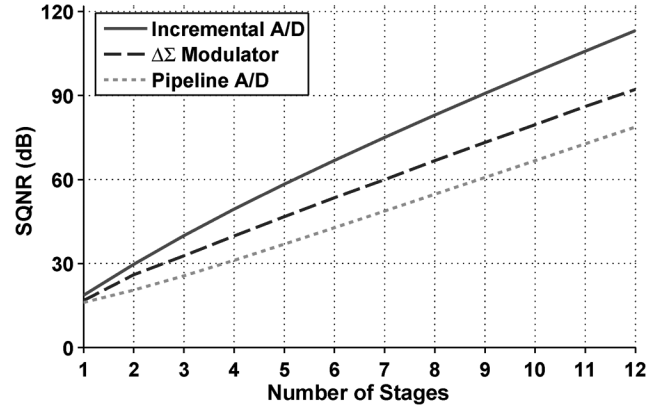


Fig. 8. Simulated SQNR versus number of stages for three different architectures at an OSR of 3 with 3-level internal quantizers. For the incremental converter and $\Delta\Sigma$ modulator, the number of stages is equivalent to its order since they use a cascade of first-order stages. Again, simulations for the incremental A/D match equation (11).

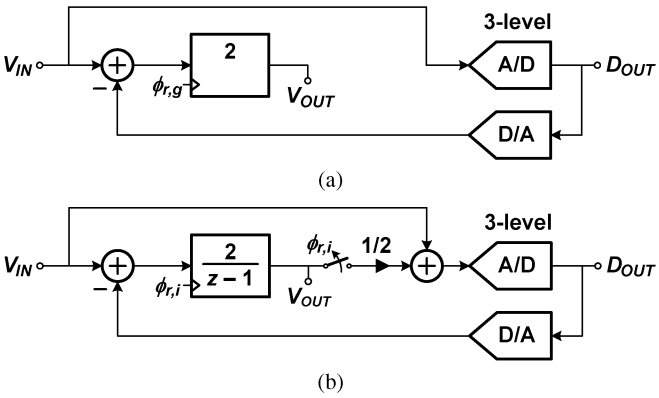


Fig. 9. The architectural similarity between the stages of a pipeline A/D converter and an input-feedforward cascaded incremental A/D converter. (a) Resetting gain stage. (b) Resetting integrating stage.

is identical to the resolution of an L-stage pipeline A/D converter with N-level internal quantizers. In fact, when the incremental A/D converter has an OSR of 1, it is effectively a pipeline A/D converter.

More specifically, an input feed-forward cascaded incremental A/D converter can be thought of as a higher order pipeline A/D converter where the OSR determines how frequently the resetting is done. Architecturally the two are almost identical; the main difference lies in designing a gain stage or an integrating stage. A single stage of both architectures is shown Fig. 9 and they are almost identical. The incremental A/D converter stage uses a resetting integrator while the pipeline A/D converter uses a gain stage which is effectively an integrator that resets on every clock cycle $\phi_{r,g}$. Also, the addition at the input of the quantizer in the incremental converter occurs on all clock cycles except for the resetting phase $\phi_{r,i}$. This is also true for the pipeline converter stage, but since it resets on every clock cycle, this addition is never performed.

At the circuit level, a resetting gain stage and a resetting integrating stage are shown in Fig. 10. The gain stage clock $\phi_{r,g}$ resets on ϕ_1, while the integrator clock $\phi_{r,i}$ resets on ϕ_1, but only every Mth clock cycle (for an OSR of M). Aside from a couple switches, the only difference lies in the resetting sequence. With the same C_1 and C_2 (a reasonable assumption since C_1 determines the thermal noise, and C_2 controls the gain), both *operational transconductance amplifiers* (OTAs) would be designed almost identically.

C. Removing the Input S/H

An incremental A/D converter ideally requires a very accurate S/H circuit on the input. The design of this block can be very difficult especially when trying to achieve better than 10-bit performance. The S/H can be removed from an incremental A/D converter, resulting in a modified STF. This can be understood by analyzing a first-order converter.

In a single-bit first-order incremental A/D converter it will be shown that the output of one conversion will always be the same as long as the average of the input for that conversion is constant (assuming no quantizer overload). For an input $V_{\rm IN}$, assuming an input feed-forward architecture, the input to the quantizer after the first M clock cycles will be

$$\begin{aligned} V_Q[1] &= V_{\rm IN}[1] \\ V_Q[2] &= V_{\rm IN}[1] + V_{\rm IN}[2] - V_{\rm REF} \cdot D_A[1] \\ V_Q[3] &= V_{\rm IN}[1] + V_{\rm IN}[2] + V_{\rm IN}[3] - V_{\rm REF} \\ &\quad \cdot (D_A[1] + D_A[2]) \\ &\vdots \\ V_Q[M] &= \sum_{i=1}^{M} V_{\rm IN}[i] - \sum_{i=1}^{M-1} V_{\rm REF} \cdot D_A[i]. \end{aligned} \tag{15}$$

If it is assumed that the converter is operating within the converter input range where the quantizer is not overloaded, then $-2V_{\rm REF} < V_Q[M] < 2V_{\rm REF}$. This also means that if the last sample $D_A[M]$ is included in the inequality,

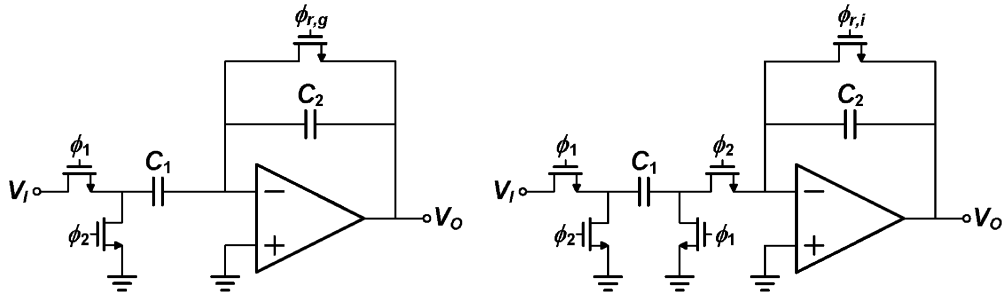
$$-V_{\rm REF} < V_Q[M] - V_{\rm REF} \cdot D_A[M] < V_{\rm REF} \tag{16}$$

which is equivalent to

$$-V_{\rm REF} < \sum_{i=1}^{M} V_{\rm IN}[i] - \sum_{i=1}^{M} V_{\rm REF} \cdot D_A[i] < V_{\rm REF}. \tag{17}$$

For a given sum of the inputs throughout the M cycles $\sum_{i=1}^{M} V_{\rm IN}[i]$, there is a unique sum of digital outputs $D_{\rm OUT} = \sum_{i=1}^{M} D_A[i]$ that will keep (17) bounded within $\pm V_{\rm REF}$. As long as $\sum_{i=1}^{M} V_{\rm IN}[i]$ is constant, $D_{\rm OUT}$ will be constant. Since $D_{\rm OUT}$ is simply the final digital output of the incremental A/D converter after going through the accumulating decimation filter, this will be a unique digital output as long as the sum of the inputs $V_{\rm IN}[i]$ is constant (which is equivalent to keeping the average of the input samples constant).

If the input of the first-order incremental A/D converter is averaged and then passed through a S/H, this system will be identical to one where a moving input enters the system with no S/H since the output is only a function of the sum. For example, if three samples of a moving input 0.1, 0.2, and 0.3 enter the first integrator of the system (for an OSR of 3), it is identical to a held input of 0.2 entering the first integrator for three cycles. So the incremental A/D converter with a moving input can be



(a) (b)

Fig. 10. The circuit-level difference between a pipeline A/D converter and an incremental A/D converter lies in the resetting sequence of the gain or integrating stage. (a) Resetting gain stage. (b) Resetting integrating stage.

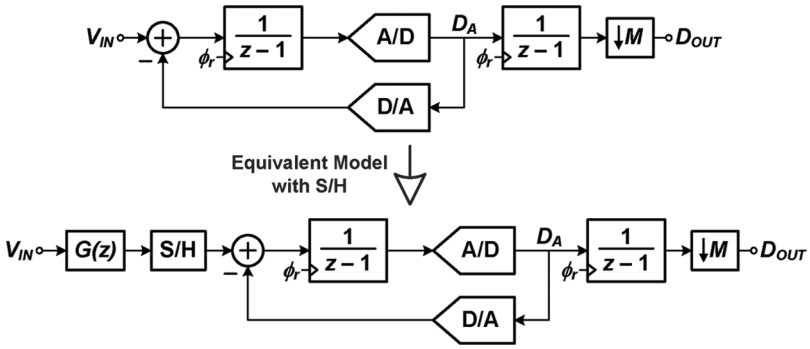
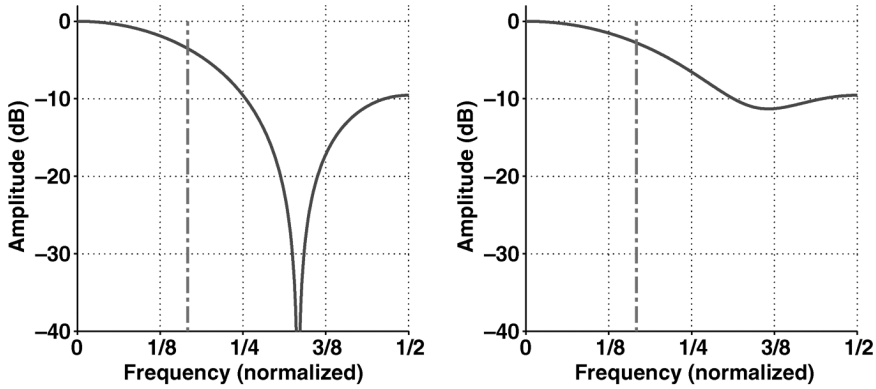


Fig. 11. Model of an incremental A/D converter with no S/H, and its equivalent model with an input S/H. $G(z)$ is not explicitly used, but it is the effective modification of the STF when the S/H is removed.



(a) (b)

Fig. 12. Signal transfer function $G(z)$ for incremental A/D converters with an OSR of 3. The vertical dotted line is at the signal band edge $f_s/(2 \cdot OSR)$. (a) First order. (b) Second order.

modeled as a typical incremental A/D converter where the S/H is preceded by an averaging filter $G(z)$, as shown in Fig. 11. This provides a direct way to analyze the effect of the moving input on an incremental A/D converter using the filter $G(z)$.

The filter $G(z)$, while not explicitly present in the incremental A/D converter, effectively modifies the STF when the input S/H is removed. Depending on the order of the modulator, $G(z)$ will have a different shape. The filter is of the form

$$G(z) = \frac{1 + z^{-1} + z^{-2} + \ldots + z^{-(M-1)}}{M} \tag{18}$$

for a first-order incremental with an OSR of M and Fig. 12 shows $G(z)$ with an OSR of 3. Since the input signal is limited to $f_s/(2 \cdot OSR)$, the attenuation will be no larger than 3.52 dB at the edge of the signal band, represented by the vertical dotted line in Fig. 12. The filter is a digital sinc filter similar to what was seen in the dual-slope A/D converter (which had no S/H). While input signals between $f_s/(2 \cdot OSR)$ and $f_s/2$ will still alias back into the signal band, they will be attenuated according to the STF.

The discussion can be extended to find STFs of higher order converters with removed S/H blocks. For these architectures the STF is a weighted sum of inputs $V_{\mathrm{IN}}[i]$ that are held constant, resulting in a more complicated filter $G(z)$ that is a weighted average of the inputs. The resulting equivalent filter $G(z)$ for a second-order incremental A/D converter with a moving input is

$$G(z) = \frac{1 + 2z^{-1} + 3z^{-2} + \ldots + Mz^{-(M-1)}}{M \cdot (M+1)/2}. \tag{19}$$

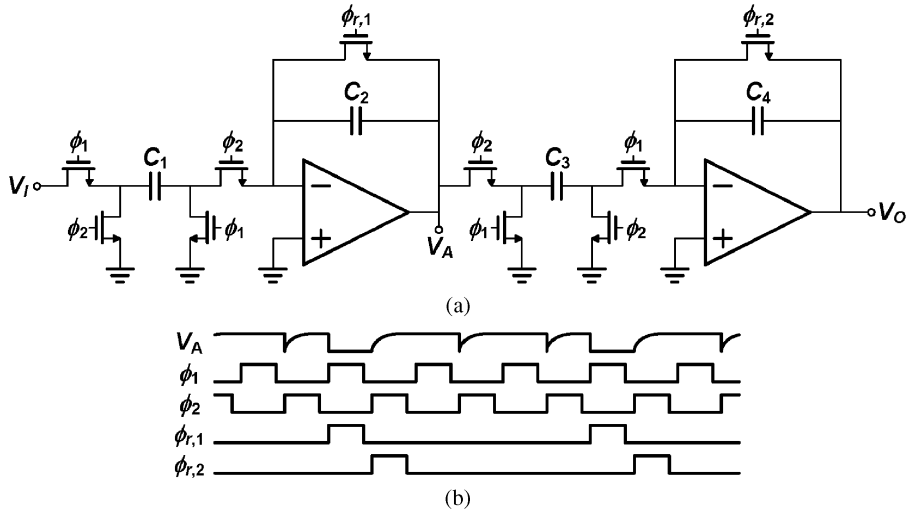


Fig. 13. Half-delaying resetting scheme for two cascaded integrators in an incremental A/D converter. (a) Resetting integrator; (b) clocking (OSR of 3).

The STF of this incremental A/D converter for an OSR of 3 is also shown in Fig. 12. The attenuation is 2.78 dB at the signal band edge. The attenuation at the edge of the signal band is less and will continue to reduce for higher order incremental A/D converters with the input S/H removed. Generalizing to an Lth-order converter (assuming an Lth-order accumulating decimation filter equal to the NTF), the STF is

$$G(z) = \frac{1 + \ldots + \frac{(M-2+L-1)!}{(M-2)!(L-1)!} z^{-(M-2)} + \frac{(M-1+L-1)!}{(M-1)!(L-1)!} z^{-(M-1)}}{\frac{(M+L-1)!}{M!(L-1)!}}. \tag{20}$$

D. Resetting Efficiency

One difficulty in designing power efficient incremental A/D converters at low OSRs is the reset phase. The simple way to reset the converter is to do the same as is done in a pipeline A/D converter. If each stage is delayed by half a clock cycle (i.e., odd stages are sampled on ϕ_1 and even stages are sampled on ϕ_2), then half a clock cycle is available to reset the integrator. As shown in Fig. 13, for the first stage the input is sampled on ϕ_1 and integrated on ϕ_2 and the opposite clock phases are used for the second stage. For an OSR of M, on every Mth clock phase of ϕ_1 the integrator is reset by $\phi_{r,1}$, and the entire ϕ_1 clock phase is available to reset. Because the output of the first integrator will only be valid at the end of ϕ_2 (due to the occasional reset during ϕ_1), the second integrator must sample on ϕ_2. The corresponding reset switch $\phi_{r,2}$ will then reset on every Mth clock phase of ϕ_2.

The resetting scheme of Fig. 13 is power inefficient because when the subsequent stage has a similarly sized capacitor as the current stage, additional loading occurs during the amplifying/integrating phase which is the phase that typically limits the OTA bandwidth. To charge the subsequent stage's sampling capacitance extra current must be drawn from the amplifier. This results in a larger amplifier and a reduced feedback factor β, further increasing the amplifier size for a given bandwidth.

At low OSRs, C_3 will likely be a significant fraction of C_2 and this increased load on the first integrator stage will increase the size of the OTA. An overdesign is required in the amplifying/integrating phase while in the sampling phase the OTA simply holds the current value and any power dissipated is wasted (although it cannot be turned off since it needs to hold the value on the capacitor). This is wasteful since both stages have significantly different requirements on the current consumption; it is far more efficient when the requirements on both stages are almost identical. The specific efficiencies are dependent on the architecture and the number of quantizer levels, but using half-delaying stages as opposed to full-delaying stages has the potential to increase the power by more than a factor of 2.

As an example, if the second stage is designed to contribute half the input-referred noise power of the first stage at an OSR of 3, then the second stage would be designed about 3 times smaller and $C_3 = C_1/3$. Also, if the integrator coefficient of the first stage is 2, then $C_1 = 2C_2$. When the first stage is not loaded by the second stage, the OTA sees a feedback capacitance of $2C_2/3$. But when it is loaded by the second stage, the sampling capacitance of the second stage $C_3 = 2C_2/3$ is added to the feedback capacitance, resulting in a doubling of the total capacitance seen by the first stage OTA, and hence a doubling of the OTA power as well.

E. Calibration

The circuit performance requirements of a cascaded incremental A/D converter are quite stringent when high resolution is desired, and calibration may be needed to achieve the full resolution. Similar to a MASH $\Delta\Sigma$ modulator, the analog filters must match the digital filters to avoid any noise leakage from earlier stages to the output. Some of the techniques presented in [11] and [12] for calibrating MASH $\Delta\Sigma$ modulators can be applied to incremental A/D converters to match the back-end digital filter to the non-ideal analog filters.

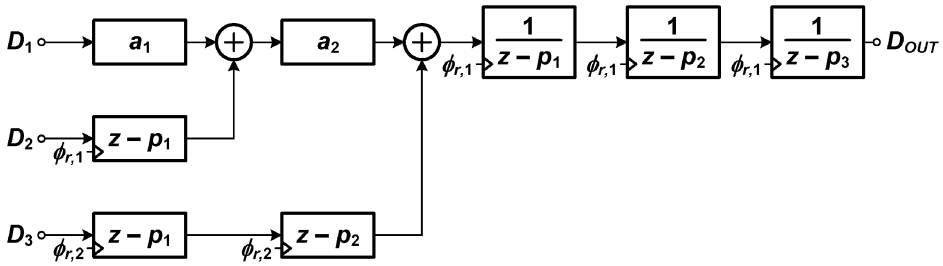


Fig. 14. Digital calibrating filter for a cascaded incremental A/D converter. A third-order structure is shown for simplicity, but it can be easily extended to an Lth-order modulator where L digital paths combine to a final $D_{\rm OUT}$.

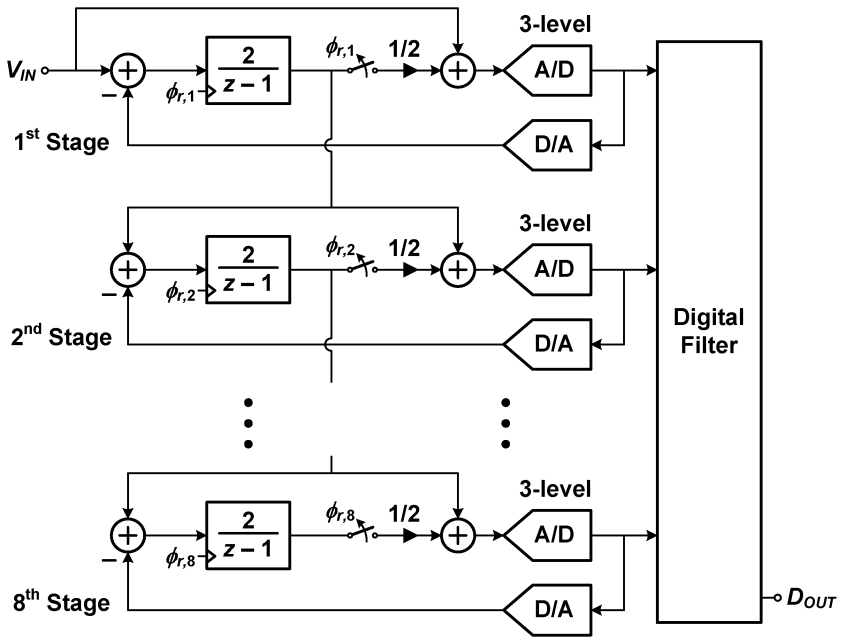


Fig. 15. Architecture for an eighth-order cascaded incremental A/D converter. The reset clocks are offset by one sample for each stage.

The coefficients that need calibration in an incremental A/D converter are similar to those of a cascaded $\Delta\Sigma$ modulator. A non-ideal integrator can be modeled as [10]

$$I(z) = \frac{a}{z - p} \tag{21}$$

where a and p are functions of the capacitor ratio and finite DC gain. If the cascaded incremental A/D converter is an ideal cascade of first-order modulators, then the back-end digital filter is as shown in Fig. 14 where the differentiators and accumulators are reset on the appropriate phases, and all of the coefficients $\{a_i, p_i\}$ are unity. If the integrators are non-ideal so that the coefficients $\{a_i, p_i\}$ characterize the ith first-order modulator according to (21), then the back-end digital filter shown in Fig. 14 will perfectly calibrate the incremental A/D converter. No noise leakage will occur when the modulator is perfectly calibrated so that the only remaining error term will exist due to the error of the last stage. For an Lth-order cascade of first-order modulators oversampled by 3 with an input $V_{\rm IN}$ and an Lth-stage quantization error ε_L, the output $D_{\rm OUT}$ is equal to (assuming a slowly varying input signal for simplicity)

$$D_{\rm OUT} = AV_{\rm IN} + B\varepsilon_L \tag{22}$$

where

$$A = \prod_{i=1}^{L} a_i \left(1 + \sum_{i=1}^{L} p_i + \sum_{i=1}^{L}\sum_{j=i}^{L} p_i p_j\right) \tag{23}$$

and

$$B = 1 + (a_L - p_L) + (a_L - p_L)^2. \tag{24}$$

The coefficient B does not deviate much from unity since both a_L and p_L are close to unity. However, the product of the coefficients that determine A can reduce the signal amplitude slightly. For example, in an eighth-order modulator with integrator DC gains of 40 B and perfect capacitor matching, the signal will be attenuated by 2.10 dB.

IV. Low OSR Incremental A/D Converter Example

This section will present a brief design example of a 12-bit (74 dB) incremental A/D converter, while also demonstrating its reconfigurability.

A. Architecture

As has been discussed, high-order cascaded architectures are better suited to low OSR incremental A/D design. The chosen architecture, shown in Fig. 15, is an eighth-order cascade of

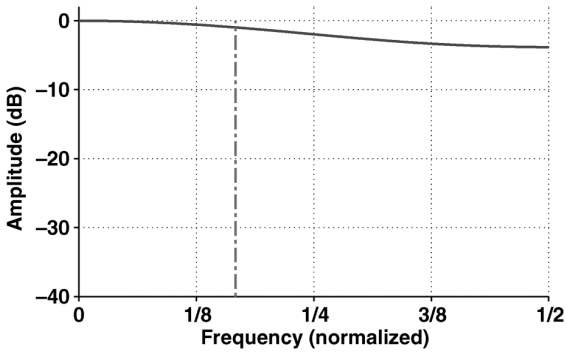


Fig. 16. STF for an eighth-order incremental A/D converter with an OSR of 3.

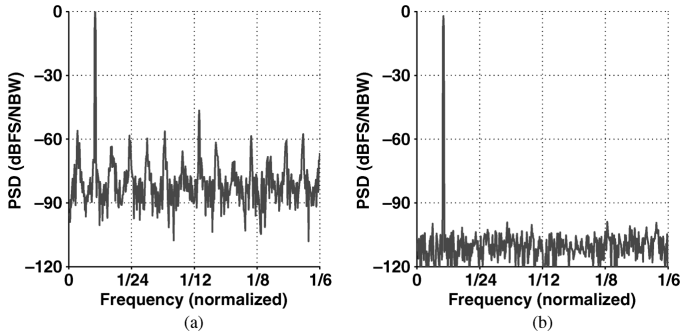


Fig. 17. Calibration of the proposed incremental A/D converter ($\mathrm{NBW} = 4.9 \times 10^{-4}$). (a) Uncalibrated. (b) Calibrated.

first-order stages with 3-level quantizers and an OSR of 3. It has a peak SQNR of 83.5 dB, 9.5 dB above the intended 74 dB resolution. Referring to Fig. 7, this architecture outperforms an equivalent $\Delta\Sigma$ architecture by 17 dB. The increased input noise due to the uneven weighting of the input samples is 3.05 dB. The corresponding weighting parameters for this architecture are $w(i) = \{1/45, 8/45, 36/45\}$.

If it is designed with controllable resetting clocks $\phi_{r,1}, \phi_{r,2}, \ldots, \phi_{r,8}$, then for any OSR of M, the clocks can be adjusted to reset every M clock cycles. If the OSR is set to 1, the architecture becomes an 8-stage pipeline A/D converter with 1.5 bits/stage. If desired, an extra 2-bit flash A/D could be added at the output of the last stage for a 10-bit pipeline architecture. If the OSR is set to infinity (i.e., the incremental converter never resets), the converter becomes an eighth-order cascaded $\Delta\Sigma$ modulator [13]. The analog circuitry remains the same but the decimation filter would need to be modified depending on the intended OSR of the $\Delta\Sigma$ modulator. The SQNR for both of these configurations were shown in Fig. 7. The chosen architecture can be reconfigured to realize any of the SQNR values on the plot by simply adjusting the resetting scheme.

B. STF

Assuming the S/H is removed, the STF of the eighth-order cascaded incremental A/D converter with an OSR of 3 and 3-level quantizers is shown in Fig. 16. The attenuation is 0.97 dB at the edge of the signal band. This is relatively small and would likely be considered a worthwhile trade-off since the high power S/H is no longer needed.

C. Calibration

The OTA gains of each stage must be high to keep the analog and digital filters matched, avoiding noise leakage. Otherwise calibration must be used where the digital filter coefficients can be calibrated to match the imperfect analog coefficients using a test signal injected in the quantizer [12]. The digital filter shown in Fig. 14 (extended to eighth-order) would be sufficient if the a_i and p_i coefficients could be calibrated to 11 bit resolution for the first-stage, and progressively less for later stages. Fig. 17 shows the spectrum of an incremental A/D converter before and after calibration, assuming OTA gains of 40 dB. The slight attenuation of the input signal due to calibration is visible.

V. Conclusion

In this paper, theory for designing incremental A/D converters at low OSRs was presented. It was shown that an incremental A/D converter has improved performance over a $\Delta\Sigma$ modulator at very low OSRs, and is equivalent to a pipeline A/D converter when oversampled by unity. The impact of removing the input S/H was analyzed, as well as the resetting phase power efficiency. A sample modulator was shown to demonstrate the feasibility of low OSR incremental A/D converters.

Appendix A

The following will derive the number of output levels for an Lth-order incremental A/D converter with an NTF of $(1-z^{-1})^L$ at an OSR of M with an N-level quantizer, and a digital decimation filter equal of $(1 - z^{-1})^L$. The A/D output $D_A[i]$ is assumed to be between ± 1 (i.e., $D_A[i] = \{-1, 1\}$ for $N = 2$, $D_A[i] = \{-1, 0, 1\}$ for $N = 3$, etc.), while the D/A output is the same value $D_A[i]$ multiplied by V_{REF}.

As a reference for the following derivations, an N-level quantizer with upper and lower quantizer levels ± 1 can have an input as large as $N/(N-1)$ without overloading the quantizer, meaning that the magnitude of the quantizer error is less than $1/(N-1)$. Input feed-forward architectures are analyzed, but feedback architectures will yield the same number of output levels.

A. First Order

In Section III-C it was shown that after M clock cycles, assuming a converter input where the quantizer input is not overloaded according to (9), the input to the quantizer is bounded by $-2V_{\mathrm{REF}} < V_Q[M] < 2V_{\mathrm{REF}}$ where

$$V_Q[M] = \sum_{i=1}^{M} V_{\mathrm{IN}}[i] - \sum_{i=1}^{M-1} V_{\mathrm{REF}} \cdot D_A[i]. \tag{25}$$

Generalized to an N-level quantizer, the quantizer input will be bounded by

$$-\frac{N}{N-1} V_{\mathrm{REF}} < V_Q[M] < \frac{N}{N-1} V_{\mathrm{REF}}. \tag{26}$$

The last digital output $V_{\mathrm{REF}} \cdot D_A[M]$ is the N-level quantized value of the input $V_Q[M]$. As long as the inequality of (26)

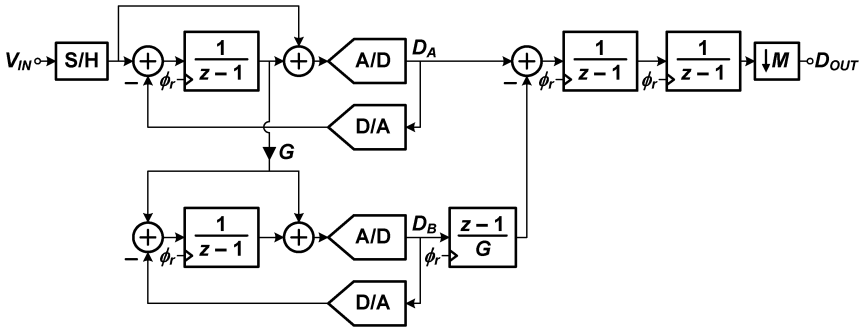


Fig. 18. A second-order input feed-forward cascaded incremental A/D converter.

holds, the difference between the input $V_Q[M]$ and the output $V_{\mathrm{REF}} \cdot D_A[M]$ must be constrained by the inequality

$$-\frac{1}{N-1}V_{\mathrm{REF}} < V_Q[M] - V_{\mathrm{REF}} \cdot D_A[M] < \frac{1}{N-1}V_{\mathrm{REF}} \tag{27}$$

or equivalently,

$$\begin{aligned}\frac{1}{N-1}V_{\mathrm{REF}} &> |V_Q[M] - V_{\mathrm{REF}} \cdot D_A[M]| \\ &= \left|\sum_{i=1}^{M} V_{\mathrm{IN}}[i] - \sum_{i=1}^{M-1} V_{\mathrm{REF}} \cdot D_A[i] \right. \\ &\quad \left. - V_{\mathrm{REF}} \cdot D_A[M]\right| \\ &= \left|MV_{\mathrm{IN}} - \sum_{i=1}^{M} V_{\mathrm{REF}} \cdot D_A[i]\right|. \end{aligned} \tag{28}$$

Dividing both sides by M and V_{REF}, the resulting inequality is

$$\frac{1}{M(N-1)} > \left|\frac{V_{\mathrm{IN}}}{V_{\mathrm{REF}}} - \frac{1}{M}\sum_{i=1}^{M} D_A[i]\right|. \tag{29}$$

The digital output of the incremental A/D converter, scaled for digital values between ± 1, is $(1/M)\sum_{i=1}^{M} D_A[i]$. Therefore, the inequality of (29) defines the error between the digital output of the incremental A/D converter and the normalized input $V_{\mathrm{IN}}/V_{\mathrm{REF}}$. Since the error magnitude is less than $1/M(N-1)$, and the error is uniformly distributed (as expected in a staircase output similar to those shown in Fig. 4 and Fig. 6 and verified in simulation), the A/D converter has $M(N-1)+1$ output levels.

B. Second-Order Single-Stage

Analyzing the second-order input feed-forward modulator of Fig. 5, the output of the first integrator is

$$\begin{aligned} V_{I,1}[1] &= 0 \\ V_{I,1}[2] &= V_{\mathrm{IN}}[1] - V_{\mathrm{REF}} \cdot D_A[1] \\ V_{I,1}[3] &= V_{\mathrm{IN}}[1] + V_{\mathrm{IN}}[2] - V_{\mathrm{REF}} \cdot (D_A[1] + D_A[2]) \\ &\vdots \\ V_{I,1}[M] &= \sum_{i=1}^{M-1} (V_{\mathrm{IN}}[i] - V_{\mathrm{REF}} \cdot D_A[i]). \end{aligned} \tag{30}$$

The output of the second integrator is

$$\begin{aligned} V_{I,2}[1] &= 0 \\ V_{I,2}[2] &= V_{I,1}[1] = 0 \\ V_{I,2}[3] &= V_{I,1}[2] + V_{I,1}[1] = V_{\mathrm{IN}}[1] - V_{\mathrm{REF}} \cdot D_A[1] \\ V_{I,2}[4] &= V_{I,1}[3] + V_{I,1}[2] + V_{I,1}[1] \\ &= 2V_{\mathrm{IN}}[1] + V_{\mathrm{IN}}[2] - V_{\mathrm{REF}} \cdot (2D_A[1] + D_A[2]) \\ &\vdots \\ V_{I,2}[M] &= \sum_{i=2}^{M-1} V_{I,1}[i] \\ &= \sum_{i=2}^{M-1}\sum_{j=1}^{i-1} (V_{\mathrm{IN}}[j] - V_{\mathrm{REF}} \cdot D_A[j]). \end{aligned} \tag{31}$$

The input to the quantizer is

$$\begin{aligned} V_Q[M] &= V_{I,2}[M] + 2V_{I,1}[M] + V_{\mathrm{IN}}[M] \\ &= \sum_{i=2}^{M-1}\sum_{j=1}^{i-1} (V_{\mathrm{IN}}[j] - V_{\mathrm{REF}} \cdot D_A[j]) \\ &\quad + 2\sum_{i=1}^{M-1} (V_{\mathrm{IN}}[i] - V_{\mathrm{REF}} \cdot D_A[i]) + V_{\mathrm{IN}}[M]. \end{aligned} \tag{32}$$

Assuming V_{IN} keeps the quantizer input from overloading, the input to the quantizer is again bounded according to

$$\frac{N}{N-1}V_{\mathrm{REF}} > |V_Q[M]|. \tag{33}$$

Adding the last digital output $V_{\mathrm{REF}} \cdot D_A[M]$, the resulting inequality (with some rearranging of (32)) is

$$\begin{aligned} &\frac{1}{N-1}V_{\mathrm{REF}} \\ &\quad > |V_Q[M] - V_{\mathrm{REF}} \cdot D_A[M]| \\ &\quad = \left|\sum_{i=1}^{M}\sum_{j=1}^{i} (V_{\mathrm{IN}}[j] - V_{\mathrm{REF}} \cdot D_A[j])\right| \\ &\quad = \left|\frac{M(M+1)}{2}V_{\mathrm{IN}} - \sum_{i=1}^{M}\sum_{j=1}^{i} V_{\mathrm{REF}} \cdot D_A[j])\right| \end{aligned} \tag{34}$$

Dividing both sides by $M(M+1)/2$ and V_{REF}, the inequality becomes

$$\frac{2}{M(M+1)(N-1)} > \left| \frac{V_{\mathrm{IN}}}{V_{\mathrm{REF}}} - \frac{2}{M(M+1)} \sum_{i=1}^{M} \sum_{j=1}^{i} D_A[i] \right|. \tag{35}$$

The scaled digital output D_{OUT} of the second-order incremental A/D converter is $(2/M(M+1)) \sum_{i=1}^{M} \sum_{j=1}^{i} D_A[i]$. Therefore, the inequality again defines the error between the digital output of the incremental converter and the normalized input. The error is less than $2/M(M+1)(N-1)$, so the A/D converter has $M(M+1)(N-1)/2+1$ output levels.

C. Second-Order Cascaded

To analyze a second-order cascaded architecture, the input feed-forward modulator of Fig. 18 will be used. The first quantizer has N_1 levels while the second quantizer has N_2 levels. The output of the first integrator is

$$\begin{aligned} V_{I,1}[1] &= 0 \\ V_{I,1}[2] &= V_{\mathrm{IN}}[1] - V_{\mathrm{REF}} \cdot D_A[1] \\ V_{I,1}[3] &= V_{\mathrm{IN}}[1] + V_{\mathrm{IN}}[2] - V_{\mathrm{REF}} \cdot (D_A[1] + D_A[2]) \\ &\vdots \\ V_{I,1}[M+1] &= \sum_{i=1}^{M} (V_{\mathrm{IN}}[i] - V_{\mathrm{REF}} \cdot D_A[i]). \end{aligned} \tag{36}$$

$M+1$ samples are taken since there is a delay from the input to the second stage. The integrator output gets multiplied by the gain G and becomes the input to the second integrator. The input to the second quantizer becomes

$$\begin{aligned} V_{Q,2}[1] &= 0 \\ V_{Q,2}[2] &= GV_{I,1}[2] = GV_{\mathrm{IN}}[1] - GV_{\mathrm{REF}} \cdot D_A[1] \\ V_{Q,2}[3] &= GV_{I,1}[3] + GV_{I,1}[2] - V_{\mathrm{REF}} \cdot D_B[2] \\ &= 2GV_{\mathrm{IN}}[1] + GV_{\mathrm{IN}}[2] - GV_{\mathrm{REF}} \\ &\quad \cdot (2D_A[1] + D_A[2]) - V_{\mathrm{REF}} \cdot D_B[1] \\ &\quad - V_{\mathrm{REF}} \cdot D_B[2] \\ &\vdots \\ V_{Q,2}[M+1] &= G \sum_{i=2}^{M+1} \sum_{j=1}^{i-1} (V_{\mathrm{IN}}[j] - V_{\mathrm{REF}} \cdot D_A[j]) \\ &\quad - \sum_{i=2}^{M} V_{\mathrm{REF}} \cdot D_B[i]. \end{aligned} \tag{37}$$

Assuming that V_{IN} keeps the quantizer input from overloading, and that the gain factor G increases the error term from the previous stage such that the input to the second stage also keeps the second quantizer input from overloading, then the input to the second quantizer is bounded according to

$$\frac{N_2}{N_2-1} V_{\mathrm{REF}} > |V_{Q,2}[M+1]|. \tag{38}$$

Adding the last digital output $V_{\mathrm{REF}} \cdot D_B[M+1]$, the resulting inequality is

$$\begin{aligned} &\frac{1}{N_2-1} V_{\mathrm{REF}} \\ &\quad > |V_Q[M+1] - V_{\mathrm{REF}} \cdot D_B[M+1]| \\ &\quad = \left| G \sum_{i=2}^{M+1} \sum_{j=1}^{i-1} (V_{\mathrm{IN}}[j] - V_{\mathrm{REF}} \cdot D_A[j]) \right. \\ &\qquad \left. - \sum_{i=2}^{M} V_{\mathrm{REF}} \cdot D_B[i] - V_{\mathrm{REF}} \cdot D_B[M+1] \right| \\ &\quad = \left| G \frac{M(M+1)}{2} V_{\mathrm{IN}} - G \sum_{i=2}^{M+1} \sum_{j=1}^{i-1} V_{\mathrm{REF}} \cdot D_A[j] \right. \\ &\qquad \left. - \sum_{i=2}^{M+1} V_{\mathrm{REF}} \cdot D_B[i] \right|. \end{aligned} \tag{39}$$

Dividing both sides by $GM(M+1)/2$ and V_{REF}, the inequality becomes

$$\begin{aligned} \frac{2}{GM(M+1)(N_2-1)} > \left| \frac{V_{\mathrm{IN}}}{V_{\mathrm{REF}}} - \frac{2}{M(M+1)} \sum_{i=1}^{M} \sum_{j=1}^{i} D_A[j] \right. \\ \left. - \frac{2}{M(M+1)} \sum_{i=2}^{M+1} \frac{D_B[i]}{G} \right|. \end{aligned} \tag{40}$$

Referring to Fig. 18, the digital output D_{OUT} of the second-order cascaded incremental A/D converter is

$$\sum_{i=1}^{M} \sum_{j=1}^{i} D_A[j] + \frac{1}{G} \sum_{i=2}^{M+1} \sum_{j=2}^{i} (D_B[j] - D_B[j-1]). \tag{41}$$

Since $D_B[1] = 0$ (no input has affected the second stage after one sample), the resulting digital output is

$$\sum_{i=1}^{M} \sum_{j=1}^{i} D_A[j] + \sum_{i=2}^{M+1} \frac{D_B[i]}{G}. \tag{42}$$

This digital output is identical to the digital signal subtracted from the normalized input signal in the inequality of (40) (aside from the scaling factor of $2/M(M+1)$ which keeps the digital signal between ± 1).

The inequality of (40) defines the error between the digital output of the cascaded incremental converter and the normalized input, and the error is less than $2/GM(M+1)(N_2-1)$ so the A/D converter has $GM(M+1)(N_2-1)/2+1$ output levels. Since the first quantizer has N_1-levels, if a converter input of unity keeps the second stage quantizer bounded (as is the case for this particular example), G can be as large as $N_1 - 1$, and the resulting number of output levels is

$$\frac{(N_1-1)(N_2-1)M(M+1)}{2} + 1. \tag{43}$$

D. Extension to Higher Order

For single-stage architectures the results can be generalized to higher order converters and the number of output levels is

$$(N-1)\frac{(M+L-1)!}{L!(M-1)!}+1. \tag{44}$$

It can be seen that this equation works for previous cases, and it should be clear how the previous analysis can be extended to third-order, fourth-order, and higher order converters (although it becomes quite tedious).

For cascaded architectures the results can also be generalized to higher order converters. The equation is very similar to that for the single-stage architecture, except that the number of output levels is increased (roughly) by the gain factor G_i associated with each stage. The resulting number of output levels for n stages is

$$(N_n-1)\prod_{i=1}^{n-1} G_i\frac{(M+L-1)!}{L!(M-1)!}+1. \tag{45}$$

If the stages are all identical first-order stages where a full-scale input keeps the quantizers bounded, then assuming each stage quantizer has N-levels, and $G_i=N-1$, the resulting number of output levels is

$$(N-1)^L\frac{(M+L-1)!}{L!(M-1)!}+1. \tag{46}$$

For an eighth-order cascaded incremental A/D converter with first-order 3-level quantizer stages, the number of output levels is

$$2^8\frac{(M+7)!}{8!(M-1)!}+1 \tag{47}$$

as the OSR M is varied. This is how the SQNR for the incremental A/D converter in Fig. 7 is found. It was also verified with simulations and matched the predicted resolution.

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