Analysis of Thermal Noise and the Effect of Parasitics in the Charge-Pump Integrator

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***Abstract*—The concept of using capacitive charge-pumps to reduce the power consumption in switched-capacitor (SC) integrators is further extended. It is shown that the charge-pump (CP) integrator can be implemented using both opamp-based and comparator-based SC circuits and achieve significant power savings. When the input sampling capacitor is split into two capacitors, the opamp-based CP integrator ideally consumes 1/4 of the power of a conventional SC integrator, while maintaining almost the same thermal noise performance. An analytical expression for the input-referred thermal noise of the CP integrator is derived and compared with the conventional integrator. The effect of parasitic capacitances on the CP integrator circuit is discussed. Input-referred thermal noise simulation results are provided.**

I. Introduction

In a SC delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) with a large oversampling ratio (OSR), the first integrator of the loop filter is typically the largest consumer of power in the ADC. Without the noise shaping effect for the first integrator, maintaining thermal noise floor below the overall accuracy requirement of the modulator puts severe demands on the opamp power consumption. More specifically, sampling capacitors are sized to achieve sufficiently low thermal noise, and for a given sampling rate and settling accuracy this translates to certain bandwidth and power dissipation for the first integrator opamp. On the other hand, circuit noise generated beyond the first integrator in the loop is attenuated by at least the first integrator gain, which is quite high over the signal band if $OSR >> 1$. Hence, the power consumption of such circuits is typically much smaller than the first stage opamp.

In [1] a charge-pump based SC integrator was proposed, which consumes significantly less power compared to the conventional SC integrator. In this paper it is shown that the proposed technique can also be applied to a comparator-based design. Section II of this paper presents the SC CP integrator circuits. Comparative analysis of the power consumption of the CP integrator versus the conventional SC integrator is presented in Section III. In Section IV input-referred thermal noise of the opamp-based CP integrator is derived and the results are confirmed with simulation. Section V discusses the effects of parasitic capacitances on the CP integrator. Section VI concludes the paper.

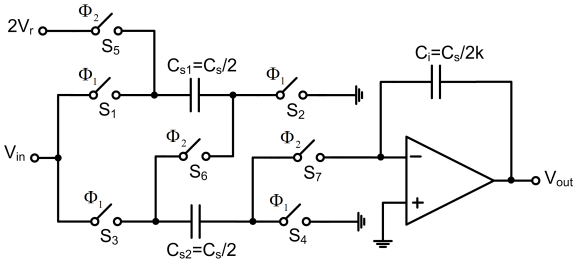

Fig. 1. Opamp-based CP integrator.

II. Charge-Pump (CP) integrator

The circuit diagram of the CP integrator circuit first proposed in [1] is shown in Fig. 1. In this circuit, during Φ_1 the sampling capacitor is divided into two halves: $C_{s1} = C_{s2} = C_s/2$. During Φ_2, C_{s1} and C_{s2} are connected in series and discharged into the feedback capacitor, C_i, through the virtual ground of the opamp. In this phase, $2V_r$ is applied in order to integrate the signal $V_{in} - V_r$. Ignoring parasitic capacitances, series connection of the sampling capacitors implements a passive gain of two for the input voltage, which is stored across an equivalent series capacitance of $C_{eq} = C_s/4$. The integrator coefficient in this case is:

$$k = \frac{2C_{eq}}{C_i} = \frac{C_s}{2C_i}. \tag{1}$$

The CP integrator circuit with separate DAC capacitor is shown in Fig. 2. Separate feedback SC branch reduces the signal-dependent distortion from the DAC reference voltage, and allows easy scaling of the feedback signal relative to the input signal. Fig. 2 shows the single-ended circuit, however in practice it is implemented fully-differentially. In this circuit, the additional CP based SC branch uses a cross-coupled differential reference voltage V_{r-} to integrate the difference voltage $V_{in} - V_r$. By sampling the reference voltage during Φ_1, it does not require $2V_r$ during Φ_2 [2]. As shown, it is also possible to sample the common-mode voltage V_{cm} during Φ_1 and apply $2V_{r+}$ during Φ_2.

The idea of using capacitive charge-pumps at the input of the integrator circuit can also be generalized by splitting the sampling capacitor into $n > 2$ capacitors during Φ_1. During Φ_2 the n sampling capacitors are connected in series and dis-

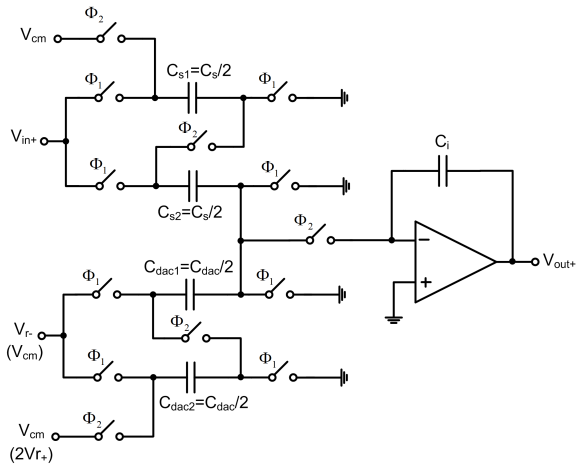

Fig. 2. Opamp-based CP integrator with separate DAC capacitor.

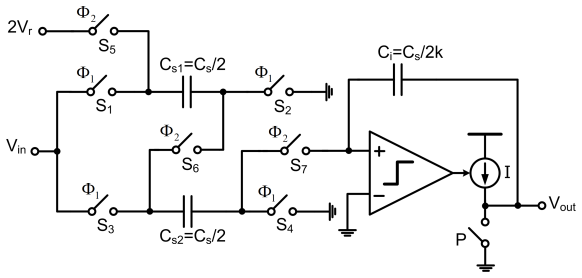

Fig. 3. Comparator-based CP integrator.

charged onto the feedback capacitor C_i=C_s/nk. This approach ideally reduces the power consumption of the integrator opamp by $1/n^2$. For simplicity in this paper we mainly focus on the case of splitting C_s into two capacitors.

The CP integrator can also be implemented using comparator-based switched-capacitor (CBSC) [3] circuits as shown in Fig. 3. In this case the comparator-based CP integrator also achieves significant power savings compared to the conventional CBSC integrator. Power consumption analysis of the CP integrator is discussed next.

III. Power consumption analysis

For a single-stage opamp the input differential pair transconductance (g_m) is proportional to the power consumption of the amplifier. Since the input differential pair transistors are typically biased in weak inversion their transconductance is linearly proportional to their bias current, which is a fixed percentage of the opamp total bias current. The required opamp transconductance can be calculated from the feedback loop parameters as [4]:

$$g_m = \frac{\omega_{-3dB} C_L}{\beta}, \tag{2}$$

where ω_{-3dB} is the closed-loop -3dB frequency, C_L is the effective load capacitance and β is the feedback factor.

For the conventional integrator, ignoring parasitics, the load capacitance seen by the opamp and the feedback factor are given by:

$$C_{L,Conv} = \frac{C_s}{k+1}, \qquad \beta_{Conv} = \frac{1}{k+1}. \tag{3}$$

For the CP integrator, C_L and β are as follows:

$$C_{L,CP} = \frac{C_s/2}{k+2}, \qquad \beta_{CP} = \frac{2}{k+2}. \tag{4}$$

Based on (3) and (4) and for the same sampling capacitance C_s, the effective close-loop load capacitance C_L/β of the CP integrator is 1/4 of that of the conventional integrator. As it is shown in Section IV, the CP integrator also achieves approximately the same input-referred thermal noise as the conventional integrator. Therefore, for the same sampling rate, thermal noise performance and settling accuracy, the required opamp transconductance (hence power dissipation) in the CP integrator is 1/4 of the conventional integrator.

In a comparator-based CP integrator reduction in the effective load capacitance C_L compared to the conventional circuit directly affects the required charging/discharging current. This is simply because for a fixed output voltage change (ΔV) caused by a constant current I charging a capacitive load within a fixed time period $(\Delta t \simeq 1/2f_s)$, the required current is proportional to the load capacitance. Therefore, the ratio of current in a comparator-based CP integrator over a comparator-based conventional integrator, both with coefficients of k, is given by:

$$\frac{I_{CP}}{I_{Conv}} = \frac{C_{L,CP}}{C_{L,Conv}} = \frac{k+1}{2(k+2)}, \tag{5}$$

which varies between 1/4 and 1/2 depending on k.

Moreover in this case, series connection of input sampling capacitors during Φ_2 appears to relax the thermal noise requirements of the comparator, so it can be designed to have a lower power (g_m) and higher input-referred thermal noise. This further reduces the power consumption of the comparator-based CP integrator compared to the conventional comparator-based integrator.

IV. Opamp-based CP Integrator Thermal noise

In this section input-referred thermal noise of the CP integrator caused by switches $S_1 - S_7$ in Fig. 1 and the opamp is derived. For noise analysis, the input voltage is set to zero and the conducting switches are replaced by their noise voltages and on-resistances, R_{on}. This is shown in Fig. 4(a) for phase Φ_1, where noise voltages and on-resistances of the series switches have been combined. During Φ_1, the mean-square (MS) value of the noise charge sampled from switches $S_1 - S_4$ onto C_{s1} and C_{s2} is: $kTC_{s1} = kTC_{s2} = kTC_s/2$. During Φ_2, the capacitors are reconfigured and the noise charge is redistributed as shown in Fig. 4(b). The noise charge entering C_i during Φ_2 is the same as the change in charge of the series

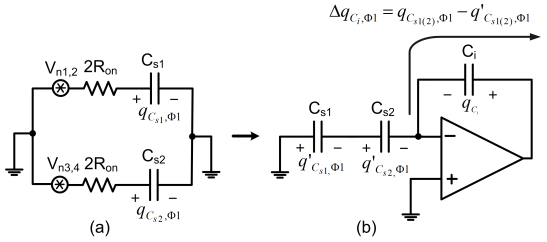

Fig. 4. (a) CP integrator circuit during Φ_1. (b) Noise charge redistribution during Φ_2.

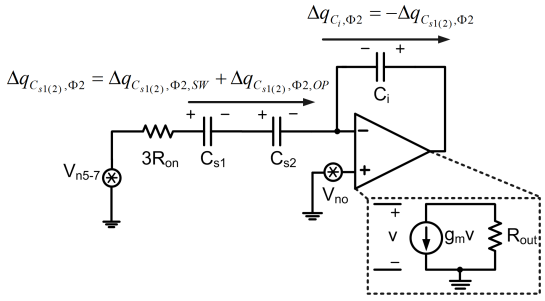

Fig. 5. CP integrator circuit during Φ_2 with the switches and opamp noise sources.

capacitors C_{s1} and C_{s2}. The MS value of this noise charge is found to be:

$$\overline{\Delta q^2_{C_i,\Phi_1}} = kTC_{eq} = \frac{kTC_s}{4}. \tag{6}$$

The noisy circuit during the integration phase Φ_2 is shown in Fig. 5, where V_{n5-7} and $3R_{on}$ represent the combined voltage noise of the switches $S_5 - S_7$ and their on-resistances, respectively. The opamp has an input-referred noise of V_{no} and is modeled by a transconductance g_m in parallel with an output resistance R_{out}. Analysis of this circuit for large R_{out} gives the MS noise charge added to C_i by the switch noise sources during each Φ_2 period as:

$$\overline{\Delta q^2_{C_i,\Phi_2,sw}} = \frac{kTC_s}{4}\left(\frac{1}{1+1/3R_{on}g_m}\right). \tag{7}$$

If the opamp is assumed to have an input-referred thermal noise power spectral density (PSD) of $V_{no} = 16kT/3g_m$ [5], its contribution to the added noise charge on C_i during Φ_2 can be calculated as:

$$\overline{\Delta q^2_{C_i,\Phi_2,op}} = \frac{kTC_s}{4}\left(\frac{4/3}{1+3R_{on}g_m}\right). \tag{8}$$

Since the three noise components above are uncorrelated, the MS value of the total noise is the sum of the individual MS values. Expressing the total noise in terms of the voltage change across C_i during Φ_2 gives:

$$\Delta V^2_{C_i} = \frac{kTC_s}{4C_i^2}\left(1+\frac{1}{1+1/3R_{on}g_m}+\frac{4/3}{1+3R_{on}g_m}\right). \tag{9}$$

Dividing (9) by the square of the CP integrator coefficient given in (1) yields the MS value of the input-referred noise voltage as:

$$V^2_{N,in,CP} = \frac{kT}{C_s}\left(1+\frac{1}{1+1/3R_{on}g_m}+\frac{4/3}{1+3R_{on}g_m}\right). \tag{10}$$

It has been shown in [5] that the MS value of the input-referred noise in the conventional SC integrator is given by:

$$V^2_{N,in,Conv} = \frac{kT}{C_s}\left(1+\frac{1}{1+1/2R_{on}g_m}+\frac{4/3}{1+2R_{on}g_m}\right). \tag{11}$$

SC circuits noise simulation feature in SpectreRF was used to verify the CP integrator noise analysis presented above. For simulations the opamp-based CP integrator of Fig. 1 was implemented in behavioral form. Specifically each switch was modeled as an ideal switch in series with an on-resistance R_{on}, which included thermal noise. The opamp was modeled as shown in Fig. 5 with a dc gain of $A = 1000$ and an input-referred noise PSD of $V_{no} = 16kT/3g_m$. Also, $C_s = 8pF$, $R_{on} = 200\Omega$, $T = 300°K$ and $OSR = 128$ were assumed. For the conventional integrator $g_m = 8mA/V$ and for the CP integrator $g_m = 2mA/V$ was used. Table I shows the input-referred thermal noise powers obtained from analysis and simulation for both integrators. Simulation results confirm the analysis presented above and show that the CP integrator achieves almost the same input-referred noise while having 1/4 of the opamp g_m compared to the conventional integrator.

TABLE I
CP/CONV INTEGRATOR INPUT-REFERRED THERMAL NOISE RESULTS.

	CP/Calc.	CP/Sim.	Conv/Calc.	Conv/Sim.
$V^2_{N,in}(dBV)$	-110.5	-110.6	-110.6	-110.7

V. SENSITIVITY TO PARASITIC CAPACITANCES

The CP integrator is parasitic-sensitive. Parasitic capacitors affect the thermal noise performance and the integrator gain coefficient as discussed below.

A. Effect on Thermal Noise

Fig. 6 shows the integrator circuit with the parasitic capacitors explicitly shown. Among these parasitics C_{p2} to C_{p4} reduce the low-frequency gain of the integrator and therefore increase the input-referred thermal noise in the signal band. Intuitively, series connection of C_{s1} and C_{s2} during phase Φ_2 implements a passive gain of two for the input signal. The integrator output signal-to-noise ratio (SNR) improvement in this case is 6 dB (or 4X power consumption) compared to

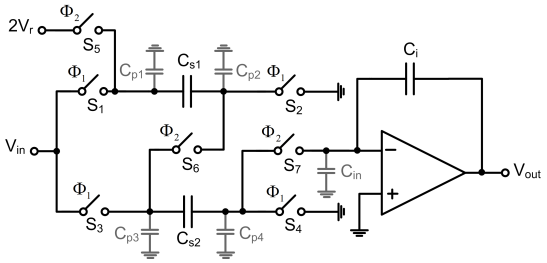

Fig. 6. CP integrator with the parasitic capacitances shown.

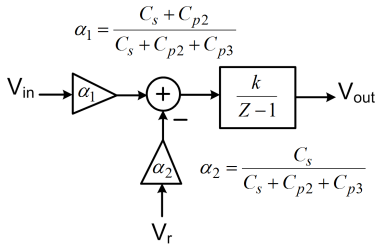

Fig. 7. CP integrator model showing the effect of parasitics on the integrator coefficient.

the conventional SC integrator. Parasitic capacitors reduce the passive gain and make the SNR improvement less than 6 dB.

Effect of parasitics on the input-referred thermal noise of the CP integrator was investigated using SpectreRF simulations. In this case $C_s = 8pF$, $T = 300^\circ K$ and $OSR = 128$ were assumed. The opamp was modeled as a transconductance $g_m = 0.5mA/V$ in parallel with an output impedance $R_{out} = 2M\Omega$. The opamp noise was assumed to be dominated by the input differential pair devices and given by $V_{no} = 16kT/3g_m$. Since the parasitic capacitors C_{p2} and C_{p3} also affect the integrator gain coefficient (as shown in Section V-B), in the simulations the top-plates of the sampling capacitors were connected to these nodes. With no parasitics included in the simulation the total input-referred thermal noise power integrated over the signal band was -110.3 dBV. To include the effect of parasitics, bottom-plate parasitic capacitance $C_{p1,4} = C_{p,bp}$ was varied from 0 to 20% while keeping the top-plate parasitics equal to 1/4 of it. Also, parasitic capacitance of the switches was assumed to be 20 fF on each side. Table II shows how the input-referred noise power changes with $C_{p,bp}$.

TABLE II
EFFECT OF PARASITICS ON THE INPUT-REFERRED THERMAL NOISE OF THE CP INTEGRATOR.

$C_{p,bp}$	1%	5%	10%	20%
$V^2_{N,in}(dBV)$	-110.1	-109.7	-109.1	-108.2

The worst case thermal noise increase, which occurs at $C_{p,bp} = 20\%$ is about 2.1 dB. This maintains 3.9 dB SNR improvement compared to the conventional SC integrator, which corresponds to a factor of 2.4 saving in power. In nanometer CMOS technologies however, parasitic capacitors are usually lower than 20%, and so their effect on the thermal noise performance is not as significant. For a typical case of $C_{p,bp} = 5\%$, the input-referred thermal noise power is -109.7 dB, which is 0.6 dB higher than the ideal (parasitic-free) CP integrator. In this case, CP integrator achieves a power reduction factor of approximately 3.5.

B. Effect on the Integrator Coefficient

Assuming an infinite gain for the opamp, C_{p2} and C_{p3} in Fig. 6 affect the gain coefficient of the integrator in the input and reference voltage paths. Neglecting the voltage dependence of parasitics, it can be shown that the effect of parasitics can be modeled as gain errors shown in Fig. 7. Assuming the worst case parasitic capacitance of C_{p2} and C_{p3} to be 5% of C_{s1} and C_{s2}, α_1 and α_2 in Fig. 7 are still very close to one:

$$\alpha_1 = 0.976, \qquad \alpha_2 = 0.952. \tag{12}$$

On the other hand, ΔΣ modulators especially single-stage architectures are generally tolerant of integrator gain coefficient errors. For second-order modulators gain variations as much as 20% have only a minor impact on the performance of the modulator [6]. In practice, there are also non-linear parasitic capacitances of the switches, which can add distortion. However, in applications with small input signals, such as wireless and sensory systems, performance is fundamentally limited by thermal noise as opposed to linearity. In this case, the CP integrator achieves a performance same as the conventional integrator, while consuming significantly less power.

VI. Conclusion

The concept of using capacitive charge-pumps in SC integrators was shown to be applicable to comparator-based circuits. For the same thermal noise performance, it was shown that the technique can significantly reduce the power consumption of SC integrators. Parasitic capacitances were shown to have small effects on the thermal noise performance as well as the integrator gain coefficients.

Acknowledgment

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