A Low-Power Delta-Sigma Modulator Using a Charge-Pump Integrator

Alireza Nilchi, *Student Member, IEEE*, and David A. Johns, *Fellow, IEEE*

***Abstract*—In this paper a low-power switched-capacitor integrator based on a capacitive charge-pump (CP) is presented, and its practical effects are discussed. The CP integrator is employed as the first stage of a $\Delta\Sigma$ ADC. The 0.13 μm CMOS prototype of the CP based ADC achieves the same performance as a conventional ADC while consuming 66% lower OTA power in the front-end integrator. The CP based modulator realizes 87.8 dB SNDR, 89.2 dB SNR and 90 dB DR over a 10 kHz bandwidth with 148 μW power consumption. The conventional ADC has similar performance but dissipates 241 μW. The energy required per conversion-step for the CP based ADC (0.369 pJ/step) is almost 40% lower than that of the conventional ADC (0.607 pJ/step).**

***Index Terms*—ADC, charge-pump integrator, chopper-stabilization, delta-sigma modulator, low-power, oversampling, switched-capacitor, thermal noise limited circuits.**

I. Introduction

POWER consumption is one of the main constraints of sensory systems. Small output signals produced by sensors put severe demands on the power consumption of the interface circuits processing such signals [1]–[3]. In high resolution switched-capacitor (SC) systems with small inputs, for a given sampling capacitor size, a large oversampling ratio (OSR) is typically required to lower the thermal noise level below the accuracy requirement of the system, and this leads to an increased operational transconductance amplifier (OTA) power consumption. Even though technology scaling has considerably reduced the digital power in sensory systems, analog front-end circuits including the analog-to-digital converters (ADCs) have not benefited from scaling in terms of power dissipation [4], [5].

A common technique for digitizing sensory signals with high resolution and low bandwidth is to use a $\Delta\Sigma$ converter with a high OSR [6], [7]. To reduce the power consumption within the scope of $\Delta\Sigma$ ADCs several techniques have been utilized. Double sampling effectively halves the required ADC sampling-rate, hence reduces its power consumption [8]–[10]. OTA sharing has allowed the implementation of $\Delta\Sigma$ ADCs with only one OTA [7], [11]. Turning off the OTA for half a clock cycle has also been used to save analog power [12]. Comparator-based switched-capacitor (CBSC) circuits replace the OTAs with more power efficient circuits such as comparators and current sources [13], [14].

In this paper, we present a technique using capacitive charge-pumps (CPs) to significantly reduce the OTA power consumption in thermal noise limited SC integrators. The approach is experimentally validated in a second order $\Delta\Sigma$ modulator with an OSR of 128. It is shown that the CP based modulator achieves the same performance as a conventional modulator, while consuming 1/3 of the OTA power in the front-end integrator.

The organization of the paper is as follows. Section II presents the CP integrator circuit. Section III discusses the power savings achievable using this technique. In Section IV practical effects in the CP integrator circuit are discussed. In Section V the CP integrator circuit with more than two sampling capacitors is described. Section VI discusses the architecture and circuit level implementation of the CP based $\Delta\Sigma$ ADC of this work. Section VII presents the experimental results obtained from a 0.13 μm CMOS prototype of the CP based ADC, and compares it with a conventional ADC. Section VIII demonstrates the system level benefits of the proposed approach over the conventional approach. Section IX concludes the paper.

II. Charge-Pump Integrator

Fig. 1(a) shows the circuit diagram of a conventional SC integrator. In this circuit, during Φ_2 the input signal $V_{\rm in}$ is sampled onto the sampling capacitor C_s. During Φ_1, C_s is connected between the OTA virtual ground and the digital-to-analog converter (DAC) reference voltage $V_{\rm ref}$ to integrate $(V_{\rm in} - V_{\rm ref})$. The integrator coefficient is given by

$$k = \frac{C_s}{C_i}. \tag{1}$$

The CP integrator circuit is shown in Fig. 1(b). In this circuit, during Φ_2 sampling capacitors $C_{s1}, C_{s2} = C_s/2$ sample the input signal. In Φ_1, the sampling capacitors are connected in series and discharged into the integrating capacitor $C_i = C_s/(2k)$ through the virtual ground of the OTA. Ignoring the parasitic capacitances, series connection of the sampling capacitors implements a voltage gain of two for the input signal $(2V_{\rm in})$, stored across an equivalent input capacitance of $C_s/4$. In order to integrate the voltage $(V_{\rm in} - V_{\rm ref})$ in this case, $2V_{\rm ref}$ is applied during Φ_1, and the difference of the sampled charge in the two phases $C_s(V_{\rm in} - V_{\rm ref})/2$ is transferred to the output [15]. The integrator coefficient in this case is given by

$$k = \frac{C_s}{2C_i}. \tag{2}$$

Manuscript received May 15, 2012; revised July 14, 2012; accepted July 31, 2012. Date of publication December 21, 2012; date of current version April 24, 2013. This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC) and the Robert Bosch Corporation. Chips were fabricated through the Canadian Microelectronics Corporation (CMC) foundry service. This paper was recommended by Associate Editor J. B. da Silva.

The authors are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4 Canada (e-mail: alireza@eecg.toronto.edu, johns@eecg.toronto.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2012.2220462

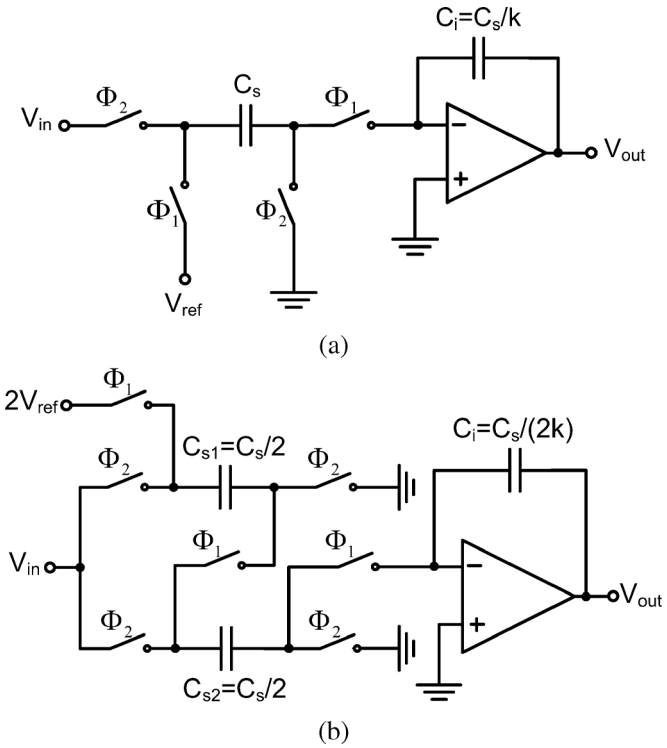

Fig. 1. (a) Conventional SC integrator and (b) proposed CP integrator.

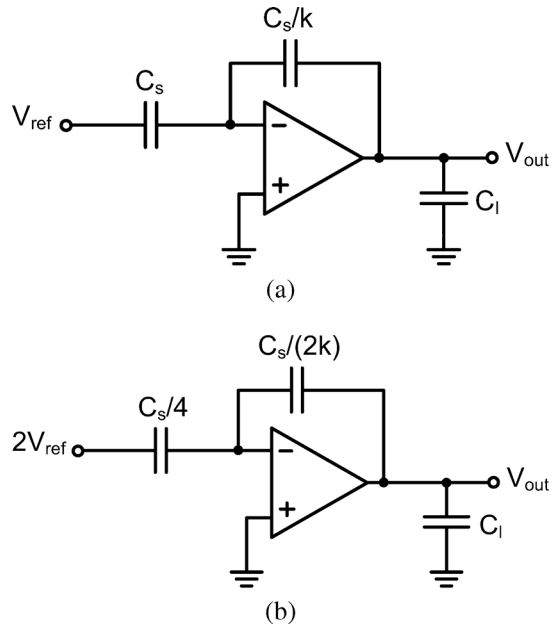

Fig. 2. Equivalent circuits of (a) the conventional and (b) CP integrators during the integration phase.

Alternatively, the required DAC reference voltage in the CP integrator can be halved by sampling it during Φ_2 [16].

III. CP Integrator Power Consumption

In SC $\Delta\Sigma$ modulators with a large OSR the first integrator of the loop filter dominates the ADC performance and power consumption. The first stage OTA power consumption depends on the sampling-rate, thermal noise performance and the required settling accuracy. More specifically, sampling capacitors are sized to achieve sufficiently low thermal noise, and for a given sampling-rate and settling accuracy this translates to certain bandwidth and power dissipation for the first stage OTA. In Section III.A the achievable power saving of the CP integrator is derived using a linear feedback model for the integrator. Next, the effects of signal forward transmission and the OTA partial slew-rate limited settling are also taken into account. Simulation results comparing the settling behavior of the CP and conventional integrators are presented in Section III.C.

A. Linear Feedback Model

For a single-stage class-A amplifier with linear settling, the input differential pair transconductance (g_m) is proportional to the power consumption of the amplifier. To achieve maximum power efficiency, the input differential pair are typically biased in weak inversion. Therefore, their transconductance is linearly proportional to their bias current. In weak inversion

$$g_m = \frac{I_D}{nV_T} \tag{3}$$

where I_D is the current flowing through one transistor of the input differential pair, n is the weak inversion slope factor and V_T is the thermal voltage [17]. The bias current I_D is a fixed percentage of the OTA total bias current, therefore

$$P_{\mathrm{OTA}} \propto g_m \tag{4}$$

where P_{OTA} is the OTA total power consumption.

The required OTA transconductance for a given sampling-rate, thermal noise performance and settling accuracy is given by [18]

$$g_m = \frac{\omega_{-3\,\mathrm{dB}} C_L}{\beta} \tag{5}$$

where $\omega_{-3\,\mathrm{dB}}$ is the closed-loop -3 dB frequency, C_L is the load capacitance seen by the OTA, and β is the feedback factor.

Ignoring the parasitics, C_L consists of the feedback network of the current stage, plus the load capacitance from the next stage C_l. Fig. 2 shows the equivalent circuits of the conventional and CP integrators during the integration phase. For the conventional integrator C_L and β are given by

$$C_{L,\mathrm{Conv}} = \frac{C_s}{k+1} + C_l \tag{6}$$

$$\beta_{\mathrm{Conv}} = \frac{1}{k+1}. \tag{7}$$

For the CP integrator, they are found to be

$$C_{L,\mathrm{CP}} = \frac{C_s/2}{k+2} + C_l \tag{8}$$

$$\beta_{\mathrm{CP}} = \frac{2}{k+2}. \tag{9}$$

Hence the effective closed-loop load capacitance C_L/β of the conventional and CP integrators are as follows:

$$\left(\frac{C_L}{\beta}\right)_{\mathrm{Conv}} = C_s + C_l(k+1) \tag{10}$$

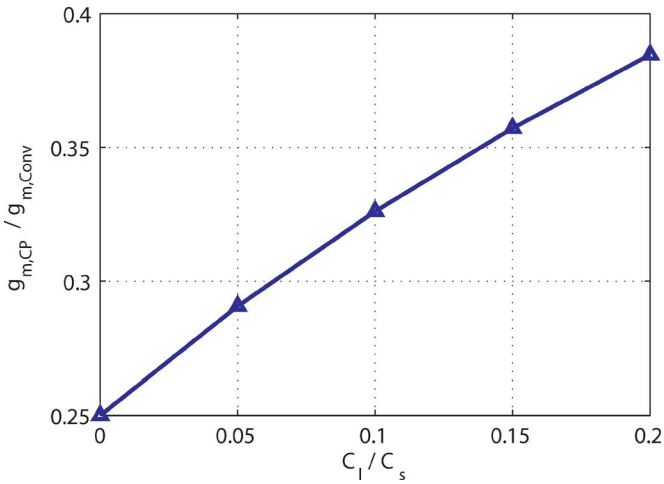

Fig. 3. Ratio of the required transconductance in the CP and conventional integrators for $k = 0.5$ as a function of C_l/C_s.

$$\left(\frac{C_L}{\beta}\right)_{\text{CP}} = \frac{C_s}{4} + C_l\left(\frac{k}{2}+1\right). \tag{11}$$

If C_l can be neglected, (10) and (11) indicate that C_L/β of the CP integrator is 1/4 of the conventional integrator.

Thermal noise analysis of the CP integrator shows that it achieves the same input-referred thermal noise as the conventional integrator [19]. During the sampling phase Φ_2, sampled thermal noise power of the CP and the conventional integrators are equal. During the integration phase Φ_1, sampled noise power of the CP integrator is four times larger than the conventional circuit, due to the series connection of C_{s1} and C_{s2}. However, this is offset by the gain of two for the input signal. Hence, both circuits require the same sampling capacitor size C_s to meet a given thermal noise performance. In this case, for the same speed, thermal noise performance and settling accuracy, the required OTA transconductance in the CP integrator is four times smaller than the conventional integrator:

$$g_{m,\text{CP}} = \frac{g_{m,\text{Conv}}}{4}. \tag{12}$$

This corresponds to four times reduction in the CP OTA power consumption:

$$P_{\text{OTA,CP}} = \frac{P_{\text{OTA,Conv}}}{4}. \tag{13}$$

Power savings in (13) can ideally be achieved when the integrator output is sampled during Φ_2 in which case $C_l = 0$. However, if the integrator output is sampled during Φ_1, the CP integrator OTA requires a transconductance higher than 1/4 of the conventional integrator OTA to drive its total capacitive load. Fig. 3 plots the ratio of the required OTA transconductance in the CP and conventional integrators $g_{m,\text{CP}}/g_{m,\text{Conv}}$ for $k = 0.5$ as a function of C_l/C_s. The required transconductance in the CP integrator is less than 40% of the conventional circuit when $C_l/C_s = 0.2$. In $\Delta\Sigma$ modulators with a high OSR, the ratio of C_l/C_s is small. This is because any error including sampled thermal noise voltage from the circuits following the first stage, when referred back to the input is attenuated by the gain of the first integrator, which is quite high in the signal band. As a result, sampling capacitors of such following stages are typically much smaller than the first stage.

It is worth noting that the CP integrator circuit shown in Fig. 1(b) also presents four times lower capacitive load to the reference voltage buffers during the integration phase. Therefore, it achieves considerable savings in the power consumption of the reference buffers as well.

B. Signal Feedforward and Partial SR-Limitation

In the integration phase of a SC integrator the feedback capacitor C_i provides not only signal feedback, but also signal feedforward. Also, depending on the magnitude of the output step, the OTA response typically includes a slewing period followed by a linear period. In this case, settling speed depends not only on the OTA transconductance, but also on its slew-rate (SR). In order to find the effect of SR-limited settling on the CP integrator power savings, a more accurate analysis of the SC integrator during the integration phase is required.

Assuming infinite DC gain for the OTA and $C_l = 0$, the closed-loop transfer function of the SC integrators in Fig. 1 during the integration phase is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = k\frac{1 - s/\omega_z}{1 + s/\omega_{-3\,\text{dB}}} \tag{14}$$

where for the conventional integrator

$$\omega_{-3\,\text{dB,Conv}} = \frac{g_{m,\text{Conv}}}{C_s} \quad \omega_{z,\text{Conv}} = \frac{g_{m,\text{Conv}}}{C_s/k} \tag{15}$$

and for the CP integrator

$$\omega_{-3\,\text{dB,CP}} = \frac{g_{m,\text{CP}}}{C_s/4} \quad \omega_{z,\text{CP}} = \frac{g_{m,\text{CP}}}{C_s/(2k)}. \tag{16}$$

The typical settling behavior of a SC integrator is illustrated in Fig. 4. Here $K_z > 1$ causes an initial step in the output response and increases the overall voltage change from $V_{o,\text{step}}$ to $K_z V_{o,\text{step}}$. The value of K_z is given by

$$K_z = 1 + \frac{\omega_{-3\,\text{dB}}}{\omega_z}. \tag{17}$$

The CP integrator has a larger K_z compared to the conventional integrator as follows:

$$\frac{K_{z,\text{CP}}}{K_{z,\text{Conv}}} = \frac{k+2}{k+1}. \tag{18}$$

Also the OTA's slewing period T_{SR} in a SC integrator is given by [20]

$$T_{\text{SR}} = \frac{K_z|V_{o,\text{step}}|}{\text{SR}} - \tau. \tag{19}$$

For a single-stage OTA for which bandwidth and SR are determined by the same amount of current I_{SS}, the ratio of the slewing periods in the CP and conventional integrators can be expressed as

$$\frac{T_{\text{SR,CP}}}{T_{\text{SR,Conv}}} = \frac{1}{2}\frac{I_{\text{SS,Conv}}}{I_{\text{SS,CP}}}\frac{|V_{o,\text{step}}/k| - V_{\text{ov}}/2}{|V_{o,\text{step}}/k| - V_{\text{ov}}} \tag{20}$$

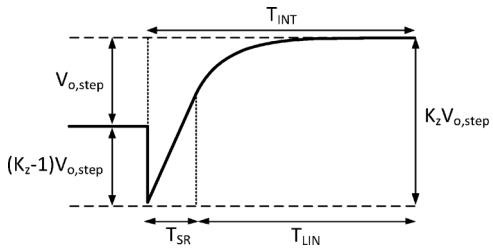

Fig. 4. OTA settling behavior during the integration phase.

where $V_{o,\mathrm{step}}/k$ is the input-referred voltage step of the integrator, and $V_{\mathrm{ov}} = 2nV_T$ is the overdrive voltage of the input differential pair biased in weak inversion. Equation (20) indicates that if $I_{\mathrm{SS,CP}} = I_{\mathrm{SS,Conv}}/4$ and $|V_{o,\mathrm{step}}/k| \gg V_{\mathrm{ov}}$, the slewing period in the CP integrator is almost two times larger than the conventional integrator. This reduces the available time for linear settling in the CP integrator, and requires a CP OTA transconductance higher than that given by (12). On the other hand, if $I_{\mathrm{SS,CP}} = I_{\mathrm{SS,Conv}}/2$, the slewing periods become almost equal. In this case, linear settling times are almost the same, while the final settling error of the CP integrator is smaller than the conventional integrator, as a result of a higher -3 dB bandwidth by a factor of two.

In a general case, to find an estimate of the achievable power savings in the CP integrator, a theoretical minimum current for the OTAs [21] in the CP and the conventional integrators can be derived. In this approach, the integration phase is partitioned into a slewing period (T_{SR}) and a linear settling period (T_{LIN}) as shown in Fig. 4. The required current for linear settling with N' time constants during the integration phase is given by

$$I_{\mathrm{SS,LIN}} = \frac{N'V_{\mathrm{ov}}}{\beta T_{\mathrm{LIN}}} C_L. \tag{21}$$

Using (19) the required slewing current during T_{SR} is found to be

$$I_{\mathrm{SS,SR}} = \frac{K_z|V_{o,\mathrm{step}}|}{\tau + T_{\mathrm{SR}}} C_L. \tag{22}$$

For the conventional and CP integrators, the required linear and slewing currents can be plotted versus the partition ratio $T_{\mathrm{SR}}/T_{\mathrm{INT}}$, as shown in Fig. 5. The optimum partition ratio and the minimum bias current occur at the intersection of the two curves. As can be seen from the graphs, the optimum slewing period increases for the CP integrator compared to the conventional integrator. The plots in Fig. 5 are based on $N' = 12$, $C_s = 10$ pF, $V_{\mathrm{ov}} = 2nV_T = 80$ mV, $k = 0.5$ and $T_{\mathrm{INT}} = 0.2$ μs. The maximum differential input-referred step size is assumed to be $V_{o,\mathrm{step}}/k = 150$ mV, which corresponds to the $\Delta\Sigma$ modulator architecture implemented in this work. The ratio of the minimum OTA currents in the CP and conventional integrators determines the achievable power saving. In this case, the CP integrator's minimum OTA current is 28.6% of that of the conventional integrator. Table I compares the results for three different input-referred steps of 350 mV, 250 mV and 150 mV. It can be seen that the power saving of the CP integrator increases for smaller step voltages. In $\Delta\Sigma$ modulators with a large OSR and a unity-gain signal transfer function (STF) in the signal band, multi-bit quantization reduces the step size of the SC integrator and makes the OTA response more linear [22]. Therefore, it helps to maximize the achievable power saving using the CP based technique.

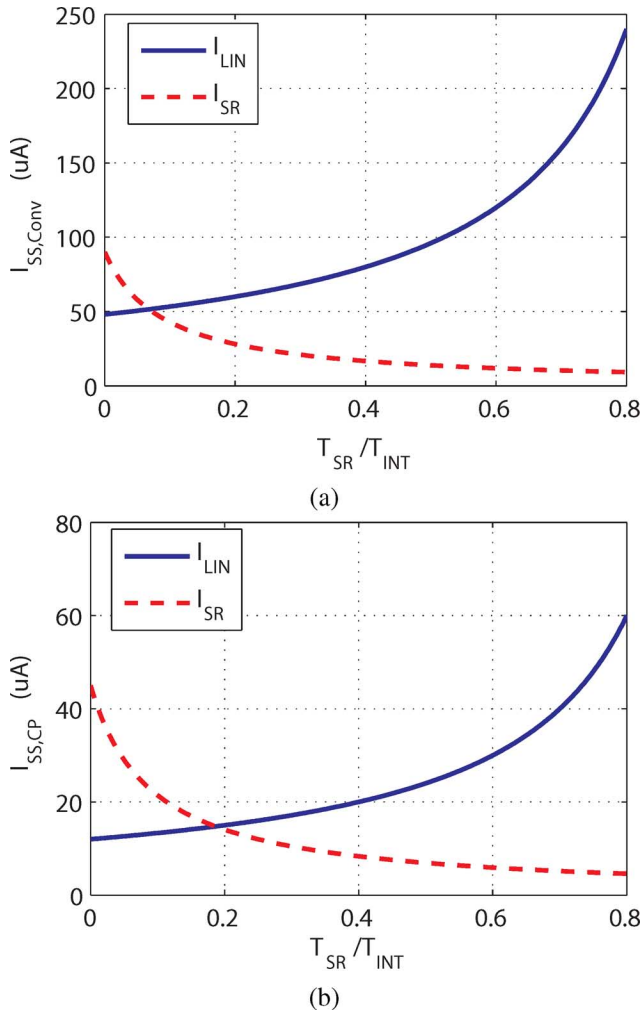

Fig. 5. Theoretical linear and SR OTA currents I_{SS} required in (a) the conventional and (b) CP integrators for a differential input-referred voltage step of 150 mV.

TABLE I
OPTIMUM SLEWING FRACTION OF THE INTEGRATION PHASE AND THE CP INTEGRATOR CURRENT CONSUMPTION RELATIVE TO THE CONVENTIONAL INTEGRATOR FOR THREE INPUT-REFERRED STEP VOLTAGES

$V_{o,step}/k$	350 mV	250 mV	150 mV
$T_{SR,Conv}/T_{INT}$	22%	15%	7%
$T_{SR,CP}/T_{INT}$	39.2%	30.5%	18.7%
I_{CP}/I_{Conv}	32.1%	30.5%	28.6%

C. Transient Simulation Results

Spectre simulations were used to verify the settling behavior of the CP and conventional integrators. The first stage CP and conventional integrators of the $\Delta\Sigma$ modulators implemented in this work (as will be described in Section VI) were simulated

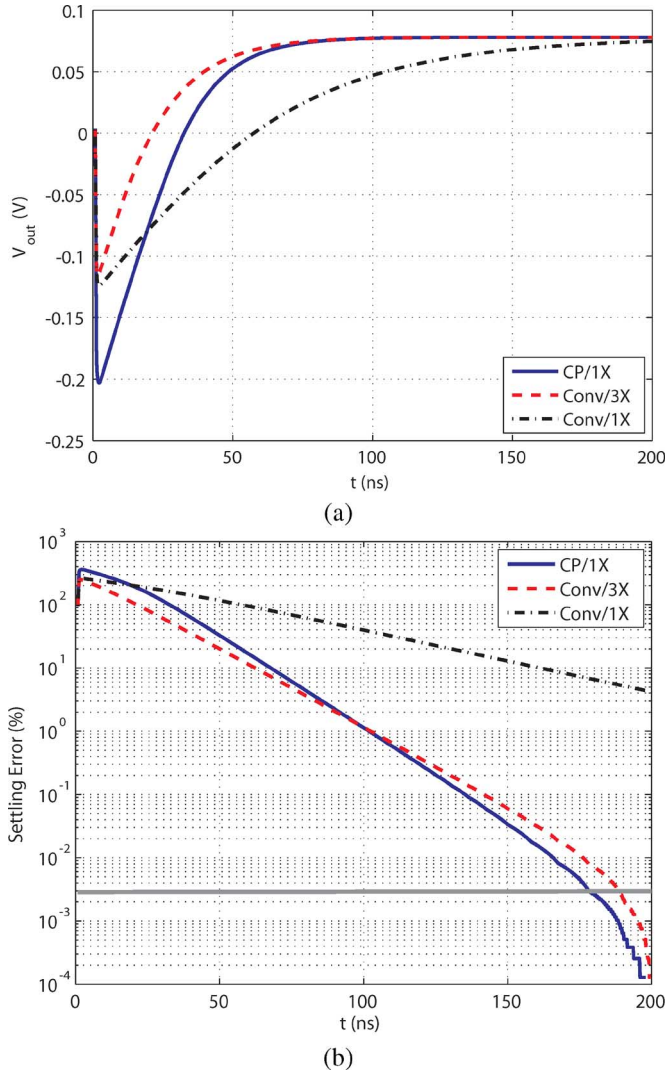

Fig. 6. (a) Simulated output response of the CP/1X, Conv/3X and Conv/1X integrators for a differential input voltage step of 150 mV (b) Percentage of settling error versus time in the waveforms shown in (a).

with a differential input voltage step of 150 mV. The CP integrator OTA (1X) in this work is designed to be three times smaller than the conventional integrator OTA (3X), therefore it consumes three times lower power. For comparison, the conventional integrator was also simulated with the 1X OTA.

Fig. 6(a) shows the simulated output response of the CP/1X, Conv/3X and Conv/1X integrators. Simulations also show that the CP/1X integrator has a larger step in its output response at the beginning of the integration phase. In order to compare the settling speed of the integrators, the percentage of settling error versus time for the transient responses of Fig. 6(a) is shown in Fig. 6(b). The horizontal line in this figure indicates the settling error required for 15-bit accuracy. To reach this accuracy, the CP/1X integrator requires 178 ns, while the Conv/3X integrator requires 189 ns. The Conv/1X integrator is much slower than the CP/1X and Conv/3X integrators. As a result, its settling error near the end of the integration phase is larger than that of the CP/1X and Conv/3X integrators by more than three orders of magnitude.

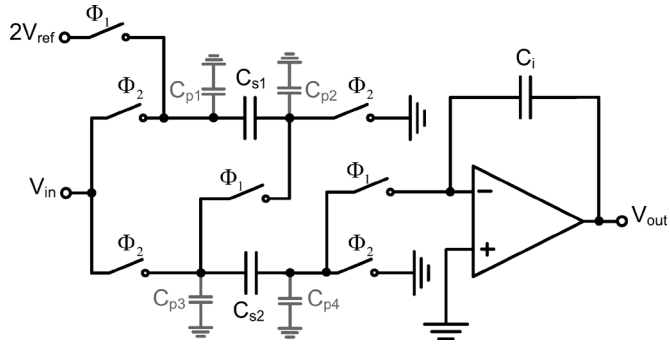

Fig. 7. CP integrator circuit with the CP parasitics shown.

IV. Other Practical Effects in the CP Integrator

A. CP Parasitic Capacitances

Fig. 7 shows the CP integrator circuit with the CP parasitics $C_{p1}-C_{p4}$ explicitly shown. Parasitic capacitors affect the input-referred thermal noise and the integrator coefficient as discussed below.

1) Effect on Thermal Noise: CP parasitics C_{p2} to C_{p4} reduce the low-frequency gain of the integrator, hence increase the input-referred thermal noise in the signal band. In this section, the effect of parasitics on the input-referred thermal noise of the CP integrator is simulated using the SC circuits noise simulation feature in SpectreRF [23]. The CP integrator shown in Fig. 7 is implemented in behavioral form. The single-stage OTA is modeled by a transconductance (g_m) in parallel with an output resistance $R_{\rm out}$, with a DC gain of $A = 60$ dB. Each switch is modeled as an ideal switch in series with an on-resistance $R_{\rm on}$, which includes thermal noise. The OTA thermal noise is assumed to be dominated by the input differential pair. In this case its input-referred noise power spectral density (PSD) is given by $S_{\rm OTA}(f) = 16kT/3g_m$ [24]. The sampling capacitor and the sampling-rate are $C_s = 10$ pF and $F_s = 2.5$ MHz, respectively. Other simulation parameters are as follows: $R_{\rm on} = 200\ \Omega$, $g_m = 0.2$ mA/V, $T = 300°$ K, and OSR $= 128$.

To include the effect of parasitics, bottom-plate parasitic capacitance $C_{p1,3} = C_{bp}$ was varied from 0 to 10% of the sampling capacitors, while keeping the top-plate parasitics equal to 1/4 of the bottom-plate parasitics. Also, parasitic capacitance of the switches was assumed to be 20 fF on each side. Fig. 8 shows how the input-referred noise power changes with C_{bp}.

From Table I, the CP integrator power consumption is about 30% of the conventional integrator. The maximum thermal noise increase, which occurs at $C_{bp} = 0.1C_{s1,2}$ is about 0.7 dB. To compensate for this increase in the input-referred thermal noise, capacitor sizes in the CP integrator must be increased by 17.5%. This increases the power consumption of the CP integrator from 30% to 35% of the conventional circuit, which still involves a substantial saving of 65% in power consumption. In nanometer CMOS technologies with metal-insulator-metal (MIM) capacitors, top and bottom-plate parasitic capacitances are typically small, hence their effect on the CP integrator thermal noise performance is also small.

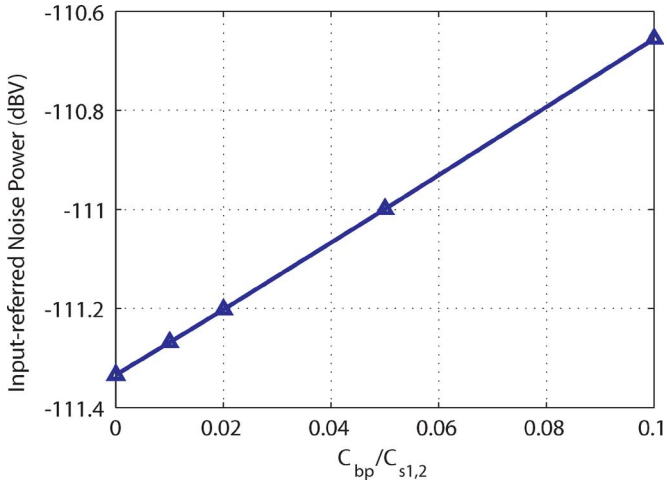

Fig. 8. In-band thermal noise power as a function of bottom-plate parasitics C_{bp}.

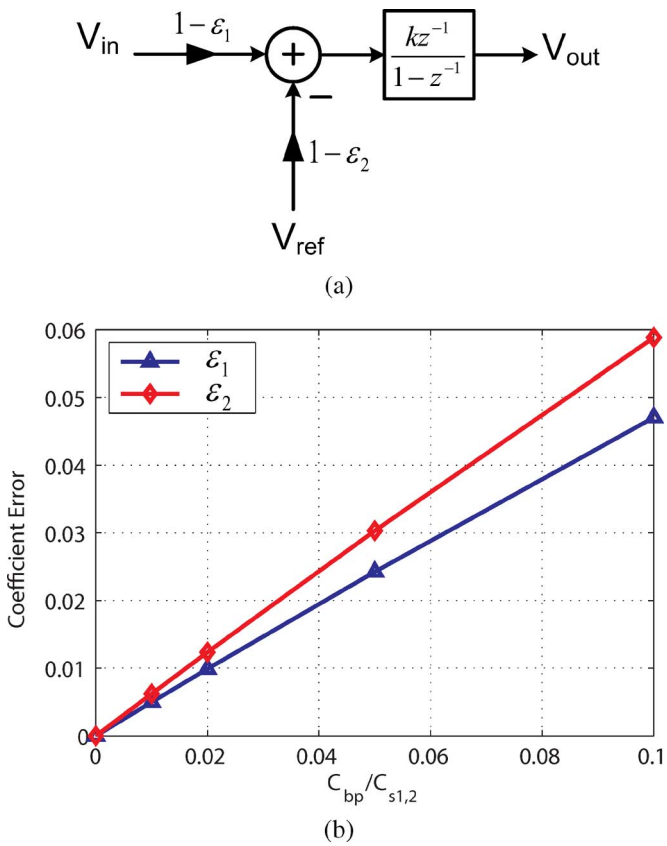

Fig. 9. (a) Modeling the CP integrator parasitics as coefficient errors ϵ_1 and ϵ_2 (b) coefficient errors as a function of C_{bp}.

2) Effect on the Integrator Coefficient: Assuming an infinite gain for the OTA, C_{p2} and C_{p3} in Fig. 7 affect the gain coefficient of the integrator in the input and reference voltage paths. Ignoring the variations in the parasitics, their effect can be modeled as coefficient errors ϵ_1 and ϵ_2 shown in Fig. 9(a), where ϵ_1 and ϵ_2 are given by

$$\epsilon_1 = \frac{C_{p3}}{C_s + C_{p2} + C_{p3}} \tag{23}$$

$$\epsilon_2 = \frac{C_{p2} + C_{p3}}{C_s + C_{p2} + C_{p3}}. \tag{24}$$

TABLE II
α_A, β_A AND γ_{OS} IN THE CP AND CONVENTIONAL INTEGRATORS

	α_A	β_A	γ_{OS}
Conventional	$\frac{1}{1+(1+k)\mu}$	$\frac{1+\mu}{1+(1+k)\mu}$	$\frac{k}{1+(1+k)\mu}$
CP	$\frac{1}{1+(1+k/2)\mu}$	$\frac{1+\mu}{1+(1+k/2)\mu}$	$\frac{k/2}{1+(1+k/2)\mu}$

Fig. 9(b) plots the errors as a function of bottom-plate parasitics C_{bp}. In this plot, C_{p2} and C_{p3} are assumed to be dominated by the top and bottom-plate parasitics of the sampling capacitors respectively, where $C_{tp} = C_{bp}/4$. The maximum percentage of coefficient error in the case of 10% parasitics is about 6%.

Variation in the modulator coefficients alters the noise transfer function (NTF), and therefore the amount of quantization noise suppression in the signal band. However, performance change in the case of single-stage modulators is negligible [25]. For instance, when ϵ_1 and ϵ_2 vary within the range shown in Fig. 9(b), change in the baseband quantization noise power of the $\Delta\Sigma$ modulator of this work, with the block diagram shown in Fig. 12, is less than 0.7 dB.

It is noted that parasitic capacitors can also cause distortion if they are nonlinear. However in applications with small input signals, such as sensory and wireless systems, performance is fundamentally limited by thermal noise as opposed to linearity.

B. Capacitor Mismatch

In practice sampling capacitors C_{s1} and C_{s2} deviate from their nominal value $C_s/2$. Such variations affect their equivalent series capacitance during the integration phase, and modify the CP integrator coefficient. However, as noted in Section IV.A, single-stage $\Delta\Sigma$ modulators are generally tolerant of large coefficient errors. Therefore variation in their performance caused by capacitor matching errors is insignificant.

C. OTA Finite Gain and Offset

The time-domain output of a delaying SC integrator with finite OTA gain (A) and offset $(V_{\rm OS})$ can be expressed as

$$V_{\rm out}(nT) = k\alpha_A V_{\rm in}(nT - T) + \beta_A V_{\rm out}(nT - T) + \gamma_{\rm OS} V_{\rm OS} \tag{25}$$

Here α_A modifies the integrator gain, β_A is the shifted pole location, and $\gamma_{\rm OS}$ is the gain seen by the OTA offset voltage. Table II shows the values of the above coefficients for the conventional and CP integrators. In this Table μ represents the inverse of the OTA gain $(\mu = 1/A)$, and for the CP integrator parasitics in the CP are ignored. It is seen that α_A and β_A for the CP integrator are closer to the ideal value of one than the conventional integrator. For instance, the pole location in the CP integrator can be approximated as $\beta_{A,\rm CP} \approx 1 - k\mu/2$, while for the conventional integrator $\beta_{A,\rm Conv} \approx 1 - k\mu$.

The effect of finite OTA gain on the CP and conventional integrators was simulated in Spectre. For the simulations, the second order $\Delta\Sigma$ modulator of this work was modeled as behavioral schematics. The first integrator was implemented as both CP and conventional circuits. The second integrator was assumed to be a conventional integrator with a DC gain of $A =$

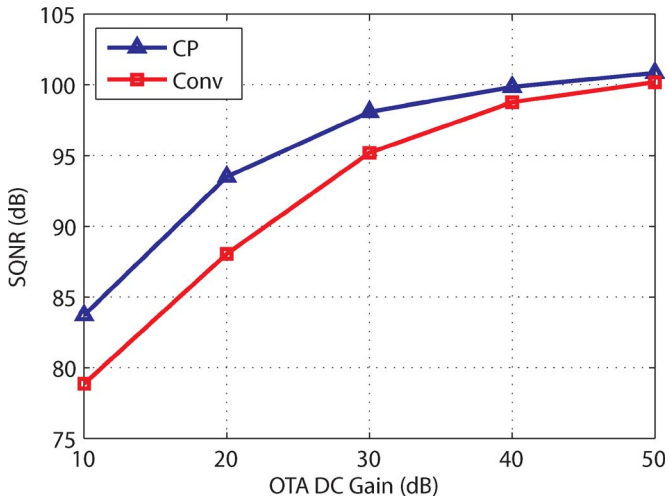

Fig. 10. SQNR performance of the CP and conventional $\Delta\Sigma$ modulators of this work versus the first stage OTA DC gain.

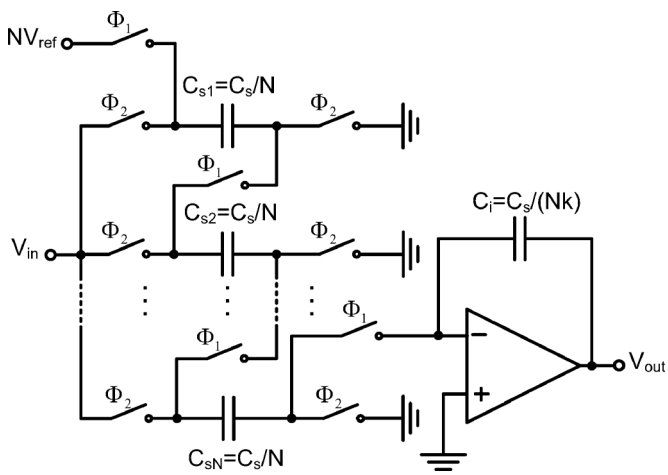

Fig. 11. CP integrator circuit using $N > 2$ sampling capacitors.

60 dB. Fig. 10 shows the SQNR of the modulators versus the first stage OTA DC gain. It is seen that the performance of the modulator with a CP based front-end integrator is less sensitive to finite OTA gain.

In terms of the OTA offset voltage, $\gamma_{\rm OS}$ in the CP integrator is almost two times smaller than the conventional circuit. Therefore to achieve the same input-referred offset, the OTA offset voltage in the CP integrator can be two times larger than the conventional integrator. Since the OTA offset standard deviation is proportional to $1/\sqrt{WL}$, where W and L are transistor dimensions, OTA scaling by four according to (13) results in the same input-referred offset voltage for the CP integrator as the conventional integrator.

V. CP Integrator Using N Sampling Capacitors

The CP integrator circuit can also be implemented using $N > 2$ sampling capacitors, as shown in Fig. 11. In this case the power consumption can ideally be reduced by a factor of N^2 compared to the conventional integrator. However, with the effect of non-linear settling taken into account the power savings decrease. For example, performing the analysis of Section III.B

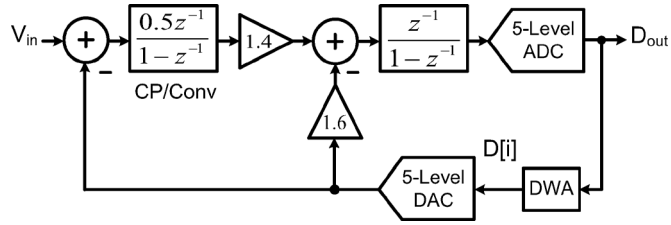

Fig. 12. $\Delta\Sigma$ modulators block diagram.

for the CP integrator with three sampling capacitors and an input-referred step size of 150 mV differential, the ratio of the minimum OTA currents in the CP and conventional integrators is $I_{\rm CP3}/I_{\rm Conv} = 14.3\%$.

Also in this case, parasitic capacitances at the various nodes of the CP increase the input-referred thermal noise. For instance, assuming $C_{bp} = 0.05C_{s1-3}$, $C_{tp} = C_{bp}/4$ and 20 fF parasitics on each side of the switches, the input-referred thermal noise increase is about 0.9 dB. Including this thermal noise increase into account, the power consumption of the CP integrator becomes 17.6% of the conventional integrator. This corresponds to an OTA scaling by a factor >5.

VI. Prototype Implementation

Two $\Delta\Sigma$ modulators are implemented. The first ADC employs a CP integrator while the second ADC uses a conventional integrator in their first stages, respectively. Circuits beyond the first stage are identical between the two ADCs. This allows for a direct comparison of the proposed CP based technique with the conventional approach.

A. Architecture

To achieve a thermal noise limited signal-to-noise ratio (SNR) of 86 dB (14 bits), a SQNR of approximately 100 dB is required, so that in-band quantization noise is sufficiently lower than thermal noise. A second order modulator with an OSR of 128 and a 5-level quantizer is selected to achieve the desired SQNR. The block diagram of the $\Delta\Sigma$ modulators is shown in Fig. 12. The delta-sigma toolbox [26] is used to synthesize the modulator NTF with a maximum out-of-band gain of 8 dB. Next, dynamic range scaling is performed to optimize the output signal range of integrators. Modulator coefficients are then approximated to allow implementation with a practical unit capacitor size.

B. Circuit Implementation

Fig. 13 shows the CP and conventional first stage integrators of the $\Delta\Sigma$ modulators. Although the figures show single-ended circuits for simplicity, the actual implementation is fully differential.

The ADC full-scale input is 400 mVpp differential required for a MEMS accelerometer application. With a 5-level DAC, the conventional integrator OTA (Conv/3X) uses three slices of the CP integrator OTA (CP/1X) and therefore consumes three times the power. The 5-level DACs are implemented using four SC unit elements. To reduce the OTA power consumption, DAC capacitors are shared with input sampling capacitors. Switches in Fig. 13 are NMOS transistors with the exception of the switches

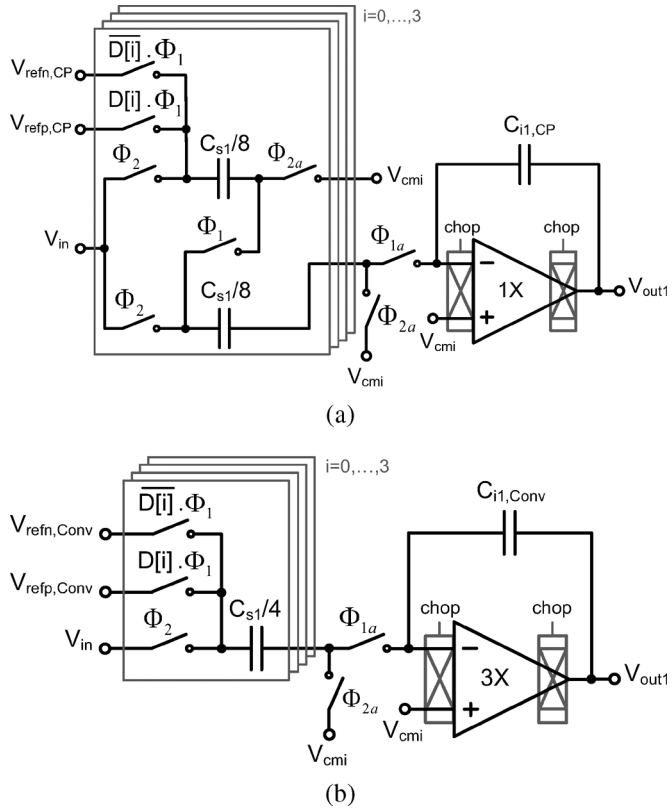

Fig. 13. (a) CP and (b) conventional first stage integrators. (Single-ended circuits are shown for simplicity.).

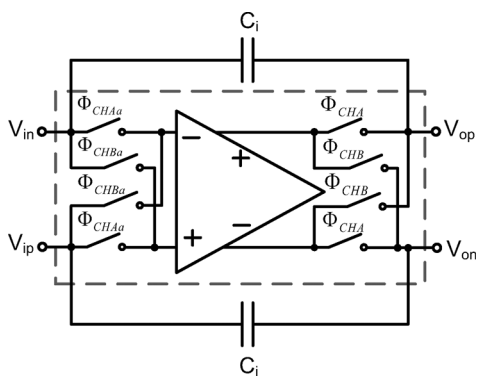

Fig. 14. Implementation of chopper-stabilization for the first stage OTAs.

sampling $V_{refp,\mathrm{CP}}$ in the CP integrator, which are implemented as CMOS transmission gates. Bottom-plate sampling with advanced clocks Φ_{1a} and Φ_{2a} is used to minimize the signal-dependent charge-injection. The sampling capacitor size in the first stage integrators is $C_{s1} = 10$ pF.

Chopper-stabilization is used to suppress OTA offset and 1/f noise in the first stage as shown in Fig. 14. Chopping is performed at half the sampling-rate, with the input chopping clocks being advanced compared to the output chopping clocks. Input chopping switches are implemented as NMOS switches due to a low OTA input common-mode voltage of $V_{cmi} = 0.2$ V. However, CMOS transmission gates are used for the output chopping switches to accommodate the OTA output voltage swings.

The 1X OTA slice in the first integrators is shown in Fig. 15. The PMOS input folded-cascode architecture allows for a low

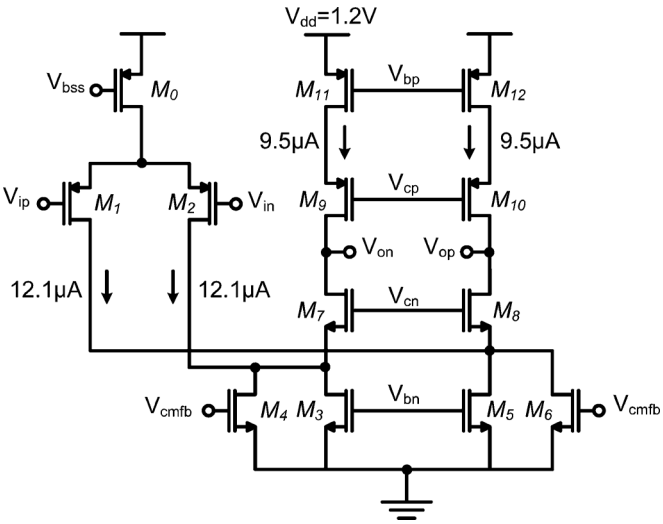

Fig. 15. 1X OTA slice used in the first stage of the CP and conventional $\Delta\Sigma$ ADCs.

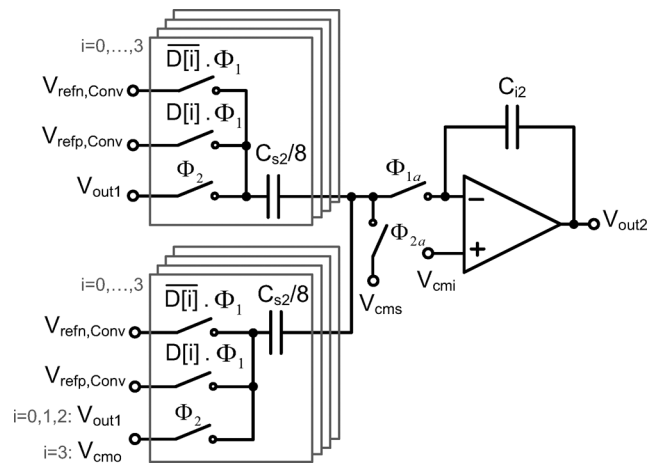

Fig. 16. Second stage integrators of the CP and conventional ADCs.

input common-mode voltage, and therefore relaxes the design of switches by affording NMOS transistors a large overdrive voltage. In the implemented prototype, the simulated DC gain of the 1X and 3X OTAs is 50.8 dB. The loop unity-gain bandwidth of the 1X OTA in the CP integrator is 12.7 MHz, while that of the 3X OTA in the conventional integrator is 9.8 MHz. The current in the OTA output devices is smaller than the input differential pair by about 20%. The simulated power consumption of the 1X OTA is 52 μW.

A single-ended version of the second stage integrators is shown in Fig. 16. The size of the sampling capacitor in the second stage is $C_{s2} = 0.48$ pF. Data-weighted averaging (DWA) is used to linearize the DACs feeding both the first and second stage integrators [27].

The 5-level quantizer is implemented as a flash ADC consisting of four dynamic comparators. Fig. 17 shows the circuit schematic of the comparator. It consists of a dynamic regenerative latch preceded by switched capacitors that are precharged to the input and quantizer reference voltages during the reset phase Φ_1. A SR-latch follows the comparator to hold its outputs during Φ_1. The threshold of comparison is set by the capacitor

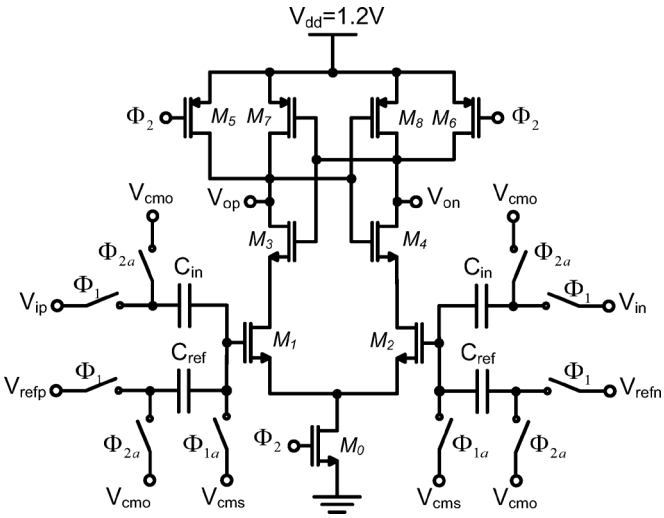

Fig. 17. Dynamic comparator used in the 5-level quantizer.

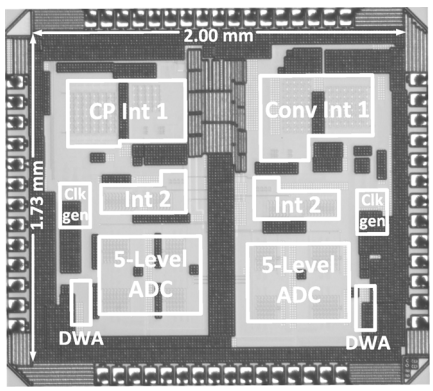

Fig. 18. Die micrograph of the fabricated prototype in 0.13 μm CMOS.

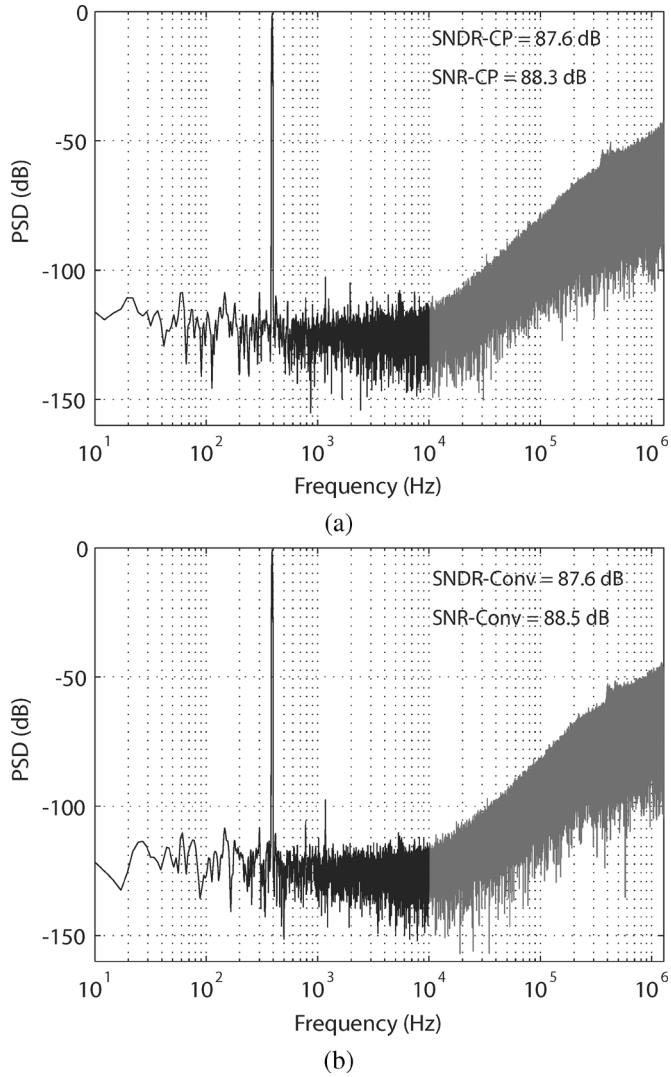

Fig. 19. Measured 2^{20}-point PSDs of (a) the CP and (b) conventional ADC outputs for a -1 dBFS, 390 Hz input sinusoid and 2.56 MHz clock (Window = Blackman–Harris).

ratio $C_{\rm ref}/C_{\rm in}$. In the implemented prototype, the comparators worst-case offset standard deviation is approximately 6.2 mV, obtained from 200 Monte-Carlo simulations.

VII. Measurement Results

The chip is fabricated in a 1.2 V 0.13 μm CMOS process. The die micrograph is shown in Fig. 18, where the core area is 3.46 mm^2. Fig. 19 shows the measured 2^{20}-point FFT output spectra of the CP and conventional ADCs for a -1 dBFS 390 Hz sinusoidal input and a 2.56 MHz clock. The ADC outputs are windowed using a Blackman-Harris window before applying the FFT.

The signal-to-noise-and-distortion ratio (SNDR) variation of the ADCs with sampling-rate for a fixed input bandwidth of 10 kHz is shown in Fig. 20. At sampling-rates up to about 1 MHz the SNDR of both modulators is quantization noise limited. From about 2.5 MHz to 3 MHz thermal noise dominates the performance. Beyond 3.5 MHz, the SNDR of both ADCs drops almost at the same rate due to insufficient settling of the OTAs. For comparison, the SNDR of the conventional ADC when its OTAs' bias current is reduced by 66% is also shown on the same plot (Conv/1X). The conventional ADC performance drops significantly at 2.5 MHz, when its first stage consumes the same

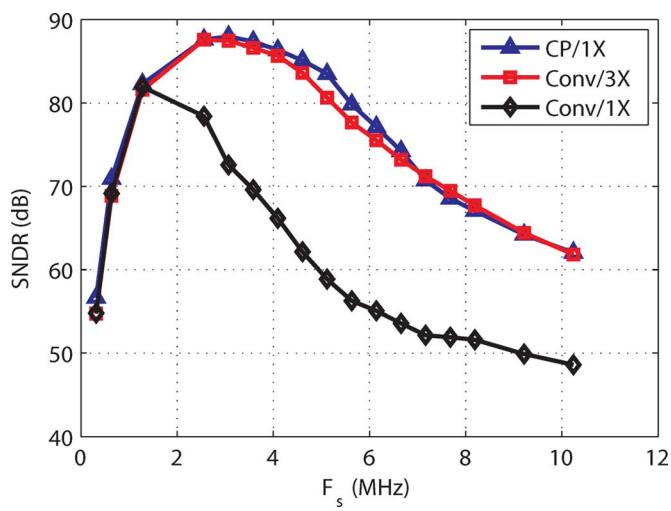

Fig. 20. Measured SNDR variation of the CP and conventional modulators versus sampling-rate (F_s) for a fixed input bandwidth of 10 kHz.

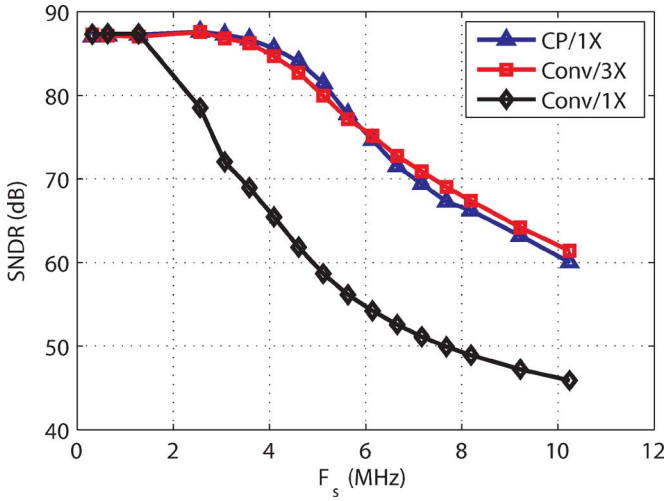

Fig. 21. Measured SNDR variation of the CP and conventional modulators versus sampling-rate (F_s) for a fixed OSR of 128.

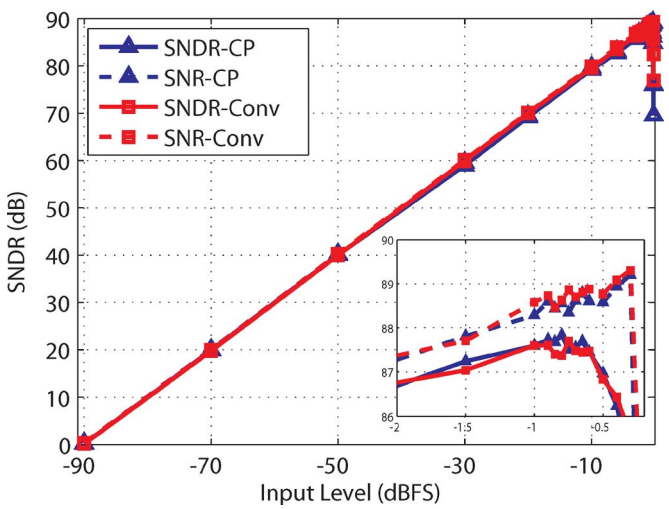

Fig. 22. Measured SNR and SNDR versus input signal level for the CP and conventional $\Delta\Sigma$ modulators.

power as the CP ADC first stage. It is noted that in this case the second stage OTA current is also scaled down with the ADC bias current scaling, however the SNDR drop can mostly be attributed to settling errors in the first stage, which are not noise shaped. Fig. 21 shows the SNDR variation versus sampling-rate for a fixed OSR of 128. In this case, the SNDR is limited by thermal noise at lower frequencies. At higher clock rates the SNDR drop follows a nearly similar trend as the fixed input bandwidth case.

Fig. 22 shows the measured SNDR/SNR of the two modulators versus input signal level for a 2.56 MHz clock. The CP ADC achieves 87.8 dB SNDR, 89.2 dB SNR and 90 dB dynamic range (DR) over a 10 kHz signal bandwidth while dissipating 148 μW. The conventional ADC has similar SNDR, SNR and DR performance but dissipates 241 μW.

The key measurement results of the two ADCs are compared in Table III. Table IV shows the power consumption breakdown of the two modulators. The CP ADC consumes extra digital

TABLE III
PERFORMANCE SUMMARY OF THE CP VERSUS CONVENTIONAL ADCS

ADC	Conventional	CP
Technology	0.13 μm	0.13 μm
Supply Voltage	1.2 V	1.2 V
Input Range (diff.)	0.4 Vpp	0.4 Vpp
Signal Bandwidth	10 kHz	10 kHz
Oversampling Ratio	128	128
Peak SNDR	87.7 dB	87.8 dB
Peak SNR	89.3 dB	89.2 dB
Dynamic Range	90 dB	90 dB
Total Power	241 μW	148 μW
FOM	607 fJ/conv-step	369 fJ/conv-step

TABLE IV
MEASURED POWER CONSUMPTION BREAKDOWN OF THE CP AND CONVENTIONAL ADCS

ADC Power	Conventional (μW)	CP (μW)
Integrator 1	156.6	52.1
Integrator 2	22	21.7
5-level ADC	4	4
Biasing	10.6	10.6
Digital	47.8	59.6

power in the clock buffers used to drive the PMOS switches in the CP integrator. However, this is not fundamental to the approach and could be avoided by selecting a lower common-mode for the CP DAC reference voltages. Based on a figure-of-merit (FOM) of

$$\text{FOM} = \frac{\text{Power}}{2 \cdot \text{BW} \cdot 2^{(\text{SNDR(dB)}-1.76)/6.02}} \tag{26}$$

the CP ADC achieves 369 fJ/conversion-step, which is almost 40% lower than the conventional ADC FOM. This overall improvement in the FOM is accomplished through the use of the front-end CP integrator that consumes 66% lower OTA power compared to the conventional integrator.

Table V compares the performance of the CP ADC with the state-of-the-art SC $\Delta\Sigma$ ADCs having an input signal range $\leq$1.1 Vpp differential and OSR $\geq$ 100. Here, FOM-dB is defined as

$$\text{FOM} - \text{dB} = \text{SNDR(dB)} + 10\log_{10}\left(\frac{\text{BW}}{\text{Power}}\right). \tag{27}$$

From the Table, [28] achieves a low power consumption of 36 μW for an input signal range of 1 Vpp differential. However, it makes use of pseudo-differential inverters instead of fully-differential OTAs, and has a lower SNDR. Even though the CP ADC of this work digitizes a relatively small input signal, it achieves higher power efficiency compared to other OTA-based ADCs.

TABLE V
COMPARISON WITH OTHER SC $\Delta\Sigma$ MODULATORS WITH AN INPUT RANGE $\leq$ 1.1 VPP DIFFERENTIAL AND OSR $\geq$ 100

	Tech. [μm]	Supply [V]	Input Range [$V_{pp-diff}$]	OSR	BW [kHz]	SNDR [dB]	Power [μW]	FOM [pJ/conv.]	FOM-dB [dB]
[7]	0.18	0.9	1.0	256	10	80.1	200	1.21	157.1
[9]	0.18	1.0	0.5	100	20	84	660	1.27	158.8
[10]	0.13	0.9	1.1	128	24	89	1500	1.36	161
[28]	0.18	0.7	1.0	100	20	81	36	0.098	168.4
[This work]	0.13	1.2	0.4	128	10	87.8	148	0.369	166.1

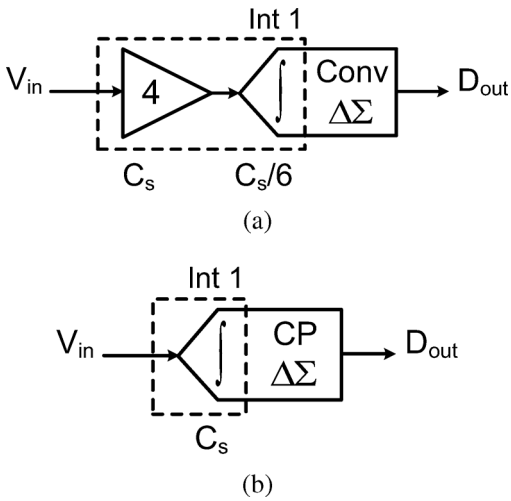

Fig. 23. Two implementations of a SC system (a) conventional approach (b) CP based approach.

VIII. SYSTEM LEVEL POWER ANALYSIS

In this section, a first order power analysis for two implementations of a SC system with a high OSR is presented. In the first implementation, as shown in Fig. 23(a), a SC gain stage is placed in front of a conventional $\Delta\Sigma$ modulator ADC. In the second approach, shown in Fig. 23(b), a CP based $\Delta\Sigma$ modulator is used to digitize the input signal without amplification. It is assumed that the input signal to the circuits is 400 mVpp differential, and the closed-loop gain of the SC amplifier is $G = 4V/V$.

In the analysis only the analog power consumption of thermal noise limited front-end circuits is taken into account. As indicated by dashed outlines these circuits include the SC gain stage and the first integrator of the conventional ADC in Fig. 23(a), and the first integrator of the CP based ADC in Fig. 23(b). It is assumed that OTA settling is linear, and the analog power consumption is proportional to the sampling capacitance of SC circuits. The latter is the case when the load capacitance seen by the OTA is dominated by the feedback network of the current stage rather than the load capacitance from the next stage. In this case, the power consumption of the front-end circuits in the conventional approach is given by

$$P_{\mathrm{Conv}} = K_p C_s \left(1 + \frac{1}{6}\right) \tag{28}$$

while the total input-referred thermal noise is

$$N_{\mathrm{Conv}} = \frac{K_n}{C_s}\left(1 + \frac{3}{8}\right). \tag{29}$$

K_p and K_n in (28) and (29) are constants of proportionality for power and noise respectively, C_s is the front-end gain stage sampling capacitor size and 1/6 is the scaling factor of the sampling capacitor for the first integrator of the conventional ADC.

For the CP based implementation

$$P_{\mathrm{CP}} = \frac{K_p C_s}{3} \tag{30}$$

where C_s is the sampling capacitor of the first integrator of the CP ADC, and the factor of three saving in power is based on the experimental results of this work. The total input-referred thermal noise is given by

$$N_{\mathrm{CP}} = \frac{K_n}{C_s}. \tag{31}$$

The product of power and noise *PN* quantifies the system analog power efficiency, where a lower figure indicates higher power efficiency. In this case, for the two implementations above

$$P_{\mathrm{Conv}} N_{\mathrm{Conv}} = 1.604 K_p K_n \tag{32}$$

hbox and

$$P_{\mathrm{CP}} N_{\mathrm{CP}} = \frac{K_p K_n}{3}. \tag{33}$$

Equations (32) and (33) indicate that the CP based approach achieves $4.8\times$ (6.8 dB) higher analog power efficiency compared to the conventional approach.

IX. CONCLUSION

A low-power $\Delta\Sigma$ modulator employing a capacitive CP integrator was presented. With a full-scale input of 400 mVpp differential, the CP ADC achieves 87.8 dB SNDR in a 10 kHz BW, while consuming 148 μW. Compared to a conventional ADC, the CP based modulator achieves the same performance while saving 66% of the front-end OTA power. From a system level perspective, the proposed approach is best suited for sensory or wireless systems with small inputs, where it can significantly reduce the power consumption of dominant front-end circuits.

REFERENCES

[1] B. E. Boser, "Electronics for micromachined inertial sensors," *Proc. IEEE Transducers '97*, pp. 1169–1172.

[2] M. Bennati, F. Thei, M. Rossi, M. Crescentini, G. D'Avino, A. Baschirotto, and M. Tartagni, "A sub-pA $\Delta\Sigma$ current amplifier for single-molecule nanosensors," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 348–349.
[3] R. Wu, J. H. Huijsing, and K. A. A. Makinwa, "A 21b$\pm$40 mV range read-out IC for bridge transducers," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 110–112.
[4] A.-J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Analog circuits in ultra-deep-submicron CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 132–143, Jan. 2005.
[5] Y. Chiu, B. Nikolic, and P. Gray, "Scaling of analog-to-digital converters into ultra-deep-submicron CMOS," in *Proc. IEEE CICC*, Sep. 2005, pp. 375–382.
[6] H.-B. Le, S.-G. Lee, and S.-T. Ryu, "A regulator-free 84 dB DR audio-band ADC for compact digital microphones," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2010, pp. 1–4.
[7] J. Goes, B. Vaz, R. Monteiro, and N. Paulino, "A 0.9 V $\Delta\Sigma$ modulator with 80 dB SNDR and 83 dB DR using a single-phase technique," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 191–200.
[8] P. Hurst and W. McIntyre, "Double sampling in switched-capacitor delta-sigma A/D converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1990, pp. 902–905.
[9] C.-H. Kuo, D.-Y. Shi, and K.-S. Chang, "A low-voltage fourth-order cascade delta-sigma modulator in 0.18-μm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2450–2461, Sep. 2010.
[10] M. G. Kim, G.-C. Ahn, P. Hanumolu, S.-H. Lee, S.-H. Kim, S.-B. You, J.-W. Kim, G. C. Temes, and U.-K. Moon, "A 0.9 V 92 dB double-sampled switched-RC delta-sigma audio ADC," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1195–1206, May 2008.
[11] K.-T. Tiew and M. Je, "A 0.06-mm^2 double-sampling single-OTA 2nd-order $\Delta\Sigma$ modulator in 0.18-μm CMOS technology," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2011, pp. 253–256.
[12] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel, and R. Thewes, "A 0.7 V MOSFET-only switched-opamp $\Sigma\Delta$ modulator," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2002, pp. 310–311.
[13] M.-C. Huang and S. L. Liu, "A fully differential comparator-based switched-capacitor $\Delta\Sigma$ modulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 5, pp. 369–373, May 2009.
[14] T. Musah, S. Kwon, H. Lakdawala, K. Soumyanath, and U.-K. Moon, "A 630 μw zero-crossing-based $\Delta\Sigma$ ADC using switched-resistor current sources in 45 nm CMOS," in *Proc. IEEE CICC*, Sep. 2009, pp. 1–4.
[15] A. Nilchi and D. A. Johns, "Charge-pump based switched-capacitor integrator for $\Delta\Sigma$ modulators," *Electron. Lett.*, vol. 46, no. 6, pp. 400–401, Mar. 2010.
[16] T. Wang and G. C. Temes, "Low-power parasitic-insensitive switched-capacitor integrator for delta-sigma ADCs," *Electron. Lett.*, vol. 46, no. 16, pp. 1114–1116, May 2010.
[17] P. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 2001.
[18] T. C. Carusone, D. A. Johns, and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 2011.
[19] A. Nilchi and D. A. Johns, "Analysis of thermal noise and the effect of parasitics in the charge-pump integrator," in *Proc. Ph.D. Research in Microelectronics and Electronics Conference (PRIME)*, Jul. 2010, pp. 1–4.
[20] A. Hamoui, T. Alhajj, and M. Taherzadeh-Sani, "Behavioral modeling of opamp gain and dynamic effects for power optimization of delta-sigma modulators and pipelined ADCs," in *Proc. Int. Symp. Low Power Electron. and Design (ISLPED)*, Oct. 2006, pp. 330–333.
[21] F. Wang and R. Harjani, "Power analysis and optimal design of op amps for oversampled converters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 4, pp. 359–369, Apr. 1999.
[22] H. Park, K. Nam, D. Su, K. Vleugels, and B. Wooley, "A 0.7-V 870 μw digital-audio CMOS sigma-delta modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1078–1088, Apr. 2009.
[23] K. Kundert, "Simulating switched-capacitor filters with SpectreRF," [Online]. Available: http://www.designers-guide.com/Analysis//sc-filters.pdf
[24] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 11, pp. 2358–2368, Nov. 2005.
[25] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1298–1308, Dec. 1988.
[26] R. Schreier, "The delta-sigma toolbox for matlab," [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange/19
[27] M. Miller and C. Petrie, "A multibit sigma-delta ADC for multimode receivers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 475–482, Mar. 2003.
[28] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, Feb. 2009.

Alireza Nilchi (S'01) received the B.Sc. degree (hons.) in electrical and electronics engineering from the University of Tehran, Tehran, Iran, in 2005 and the M.A.Sc. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2008, where he is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering.

He held a summer position with the Universität der Bundeswehr München, Munich, Germany, in 2004. He also worked as an intern at Kapik Integration, Toronto, Canada from November 2010 to March 2011. His current research interests are on scaled CMOS analog/mixed-signal integrated circuits and very low power data converters for sensor applications.

Mr. Nilchi was the recipient of the Best Student Paper Award of the IEEE Circuits and Systems Conference (ISCAS), as well as a co-recipient of the Best Paper Award of the Sensory Systems Technical Committee of the IEEE Circuits and Systems Society in 2009.

David A. Johns (S'81–M'89–SM'94–F'01) received the B.A.Sc., M.A.Sc., and Ph.D. degrees from the University of Toronto, ON, Canada, in 1980, 1983, and 1989, respectively.

In 1988, he was hired at the University of Toronto where he is currently a Full Professor. He has ongoing research programs in the general area of analog integrated circuits. His research work has resulted in more than 80 publications as well as the 1999 IEEE Darlington Award. Together with academic experience, he also has spent a number of years in the semiconductor industry and was a co-founder of a successful IP company called Snowbush Microelectronics.

Dr. Johns served as a guest editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS as well as being a member of the SSCS Adcom from 2002 to 2008.