A 5TH ORDER GM-C FILTER IN 0.25㎜M CMOS WITH DIGITALLY PROGRAMMABLE POLES & ZEROES

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ABSTRACT

This paper describes a 5th order Gm-C filter in a 0.25 µm CMOS technology. The signal path, including transconductors and Miller integrators, consists entirely of NMOS transistors for high speed operation. All poles and zeros are digitally programmable. A prototype configured for a lowpass response demonstrates a signal bandwidth of 45 MHz.

1. INTRODUCTION

As digital CMOS processes continue to advance, the size and power consumption of digital circuitry decreases dramatically. At the same time, lower supply voltages make the design of high resolution analog-to-digital converters increasingly difficult. Therefore, there is great motivation to implement some signal processing in the analog domain in order to reduce A/D converter resolution. Analog adaptive filters can be very useful in this regard. A major problem limiting the use of analog adaptive filters today is that analog adaptation circuitry is difficult to design and suffers from dc offset effects [1]. In order to obviate the need for analog adaptation circuitry, it is desirable to have a digitally programmable analog filter, which is the focus of this paper.

This paper describes a 5th order digitally programmable orthonormal ladder filter in a 0.25 µm CMOS process intended for analog adaptive filtering applications. All poles and zeros are digitally programmable so that the adaptation algorithm can be implemented digitally. The orthonormal ladder structure has the advantage of maintaining optimal dynamic range scaling for any stable pole and zero locations [2], thus making it particularly well suited to highly programmable analog filters. A digital process technology was used (no double-poly or thick oxide options) to facilitate integration in mixed-signal systems. Digital control was provided via programmable transconductances in a Gm-C circuit topology.

2. CIRCUIT DESCRIPTION

2.1 A Digitally-Programmable CMOS Transconductor

CMOS transconductors based upon the transconductance of a differential pair must have small input signal swings to ensure their voltage-current relationship remains linear. In order to allow for larger input signals (and hence improved dynamic range) a transistor biased in triode can be used to source-degenerate the differential pair. Linearity can be further improved by using feedback to fix the gate-source voltage of the input transistors.

In the transconductor of Fig. 1A [3], M3 provides the source-degeneration and the source-followers at M6 and M7 provide a feedback path to increase linearity. However, this circuit is not well suited to low supply voltages because the gate-source voltages of two active devices are cascaded (Vgs4 and Vgs6). The

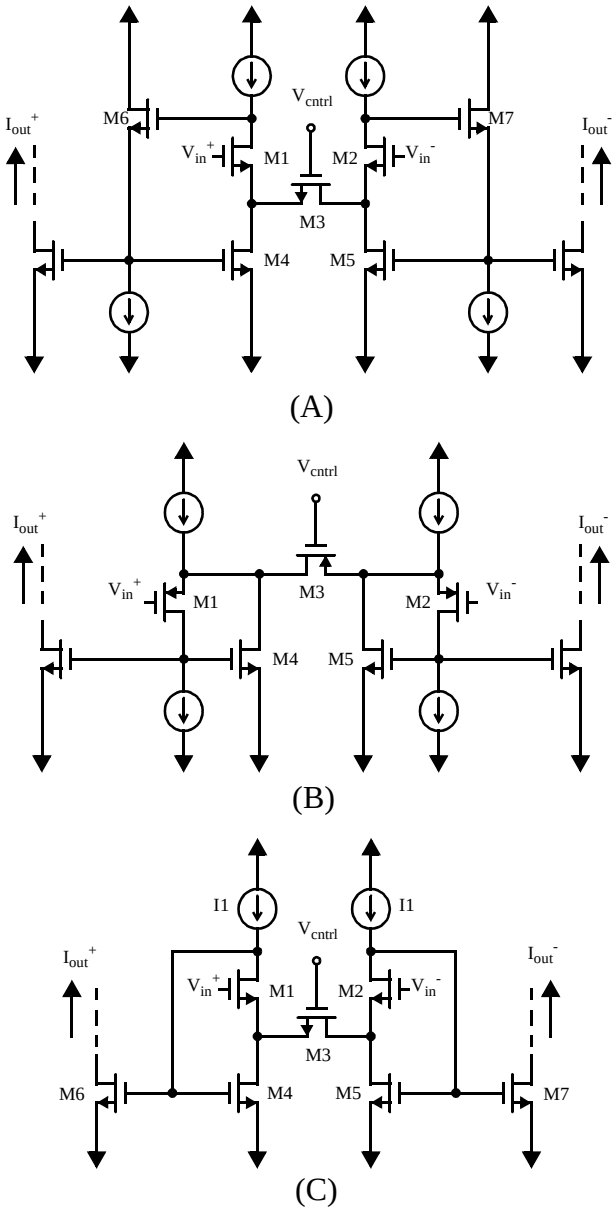

Figure 1. Three transconductors based upon triode-region MOS devices (M3) with feedback to improve linearity: (A) [3] (B) [4] (C) this work.

circuit in Fig. 1B [4] is suitable for lower supply voltages. However, M1, M2, and M3 are p-channel and, hence, must be larger than the corresponding n-channel devices in Fig. 1A in order to

have the same transconductance. This results is larger parasitic capacitances which limit the circuit's speed.

The transconductor shown in Fig. 1C was used in this design. Negative feedback is provided by directly connecting the gate of M4 (M5) to the drain of M1 (M2). By eliminating the source follower from Fig. 1A, lower supply voltages can be used and a parasitic pole is eliminated from the transconductor's frequency response. Unlike Fig. 1B, the signal path consists entirely of n-channel transistors; p-channel devices are used only for biasing.

The dc small-signal transconductance of the circuit in Fig. 1C is approximately given by,

$$\frac{I_{out}^{+} - I_{out}^{-}}{V_{in}^{+} - V_{in}^{-}} = G_m = M(2G_{ds3} + G_{ds4} + G_{s1}) \qquad (1)$$

In Eqn. (1), M is the gain of the output current mirror formed by M4/M5 and M6/M7. G_{ds3} is the drain-source conductance of M3. in triode, G_{ds4} is the drain-source conductance of transistor M3 in saturation, and G_{s1} is due to the body effect of M1. In this design, the values of M and G_{ds3} are controlled digitally, but the values of G_{ds4} and G_{s1} are parasitic conductances which are not easily controlled.

Transistor M3 in Fig. 1C is actually a binary-weighted array of unit transistors. The gate voltage of each can be set to either V_{SS} which turns it off, or V_{cntrl} which puts it in triode. The array provides 5 bits of control [g_2 g_1 g_0 g_{-1} g_{-2}] over the value of G_{ds3}.

An additional 2 bits of programmability is provided at the output current mirrors formed by M4/M5 and M6/M7. This allows small values of G_m to be realized even in the presence of finite parasitic conductances G_{ds4} and G_{s1}. Two control bits, d_1 - d_0, allow the output current mirror gain to be set at M = 1, 0.75, 0.25, or 0. When M < 1, parallel dc current sources are activated to maintain the same bias currents through $I_{out}^{\pm}$. In some transconductors, the positive and negative signal paths were also cross-coupled using switches to provide digital control of the output polarity via a sign bit. Overall, the transconductor is programmable up to a maximum gain of approximately 0.35 mA/V.

2.2 Miller Integrator

In order to reduce the effects of non-linear junction capacitances and finite output impedance at the transconductor outputs, the integrating capacitors were placed in feedback around an opamp (called a Miller Integrator). For high-speed operation it is desirable to use a simple opamp with as few internal nodes as possible. In [5] a PMOS common-source stage provides high gain with common-gate current-mode inputs (Fig. 2A). The bandwidth of this circuit is limited by the high-impedance nodes at the gates of the common-source transistors M3 and M4. In order to provide sufficient gain, these devices must be relatively large. An NMOS cascode gain stage can be used instead as shown in Fig. 2B to provide the same gain with smaller transistor sizes and, hence, less capacitance at the speed-critical nodes. Again, the entire signal path consists of NMOS transistors; PMOS transistors are used only for biasing. Transistor M_C is biased in triode to provide lead compensation.

2.3 Common-Mode Feedback

Although a continuous-time CMFB obviates the need for clock generation circuitry and avoids clock feed through glitches

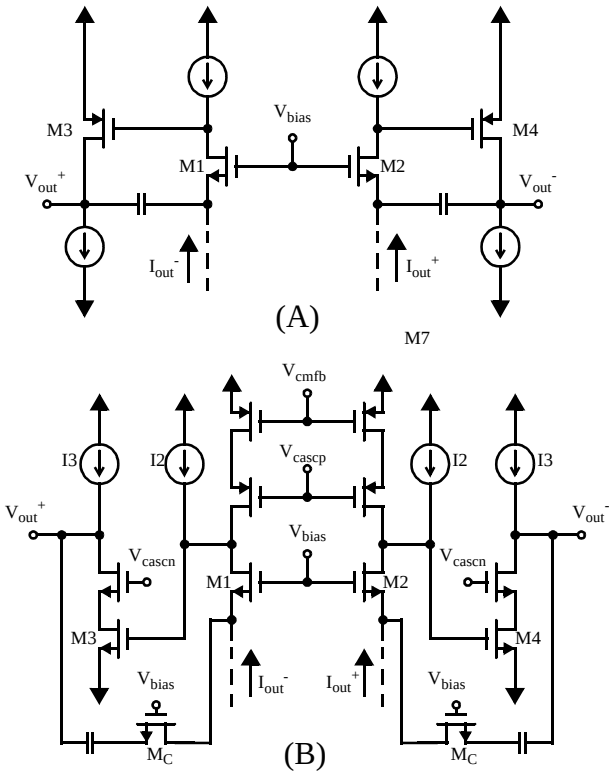

Figure 2. Current-input CMOS active integrators: (A) reference [5] (B) this work.

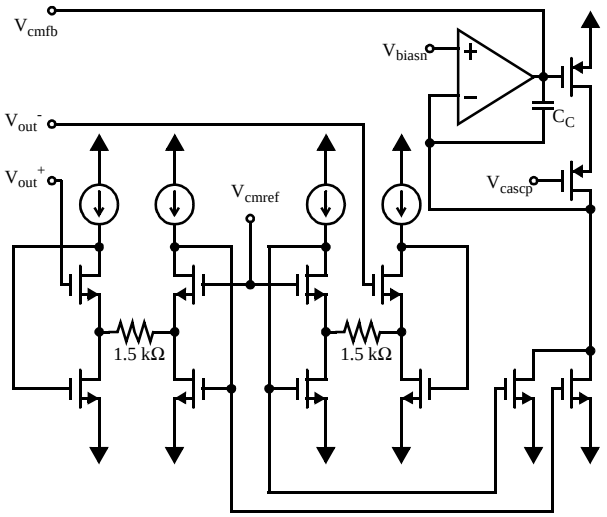

Figure 3. Schematic diagram of continuous-time CMFB.

at the filter output, a continuous-time design is complicated by the low supply voltage (2.5 V). The CMFB circuit must be stable and relatively fast to eliminate as much high-frequency common-mode noise as possible. Furthermore, in this application it is also important that the common-mode potential of the output accurately matches the common mode reference, V_{cmref}. Since the control voltage V_{cntrl} is referenced to V_{cmref}, a change in the out-

put common model level will affect the gain of a subsequent transconductor stage.

A schematic of the CMFB design appears in Fig. 3. The current outputs of two differential transconductors were taken single-endedly, summed, and mirrored to the 1st stage of the Miller integrator via V_{cmfb}. The opamp fixes the drain of M7 at the same dc potential as the drain of M1 & M2 in Fig. 2B to avoid systematic offsets in the CMFB loop. Compensation of the loop is complicated by the presence of high-impedance nodes at the integrator outputs, V_{out}^{+} and V_{out}^{-}. In a simple Gm-C topology, it would be possible to compensate the loop by adding capacitance to the output nodes. However, because the integrating capacitors in this design are not grounded, they cannot be used to stabilize the CMFB loop. Instead, Miller compensation was applied at the output of the CMFB circuit via C_C.

Another difficulty in designing the common-mode feedback circuit is that it must fix the common-mode level of both the first and second stages of the Miller integrator. Therefore, the feedback control voltage V_{cmfb} is applied to the first stage current source. As a result, there is a large dc gain from V_{cmfb} to the filter outputs, V_{out}^{+} and V_{out}^{-}. To maintain stability of the feedback loop, V_{cmfb} is connected to only 2 of 18 fingers in the first stage current source. The other 16 fingers provide a fixed dc bias current, I2, as shown in Fig. 2B.

2.4 Prototype

A prototype was fabricated in a standard digital 0.25 µm CMOS process. Two filters were included:

- A first-order lowpass filter section (Fig. 4).
- A 5th order orthonormal ladder filter (Fig. 5).

All of the summations in Fig. 5 were performed by combining the output currents of transconductors. Where a summation node has fewer than three inputs, fixed dc current sources were added to properly bias the input stage of the subsequent Miller integrator. Since all of the filter parameters a_i and b_i were implemented as digitally programmable transconductors, the location of all poles and zeros can be set digitally. This level of digital programmability in an analog continuous time filter has previously only been reported up to 8 MHz, and in that case in a BiCMOS process [6]

A die photo of the prototype is shown in Fig. 6. The total area of test chip is 2.5 mm × 1.7 mm. Of that, only 1.25 mm × 0.38 mm ≈ 0.5 mm^2 is occupied by the actual filter. The rest includes test circuitry, probe pads, and digital logic to store the filter coefficients. Most of the filter area is occupied by metal-metal capacitors. The capacitance per unit area could have been increased by using interleaved capacitors thereby reducing the analog filter layout by approximately 40% to 0.3 mm^2.

3. EXPERIMENTAL MEASUREMENTS

Fig. 7 shows the normalized gain of G_{m1} in the first-order filter as a function of the 5-bit control word g_2-g_{-2} while holding the feedback gain G_{m2} constant. The curves in Fig. 7 do not pass through the origin because even when all of the triode transistors are turned off, the transconductor in Fig. 1C has a nonzero gain due to parasitic conductances between the drain/source of M3 and ground. Reprogramming the transconductor's output current mirror gain to $M = 0.25$ allows one to realize smaller gains, however many transfer functions require feedin gains of exactly zero. In these cases, the output current mirror gain can be set to zero.

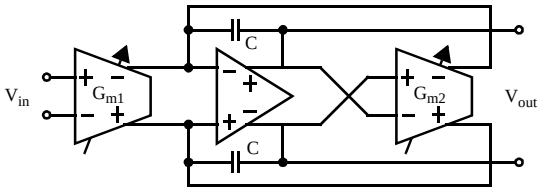

Figure 4. First-order G_m-C filter with programmable pole and dc gain.

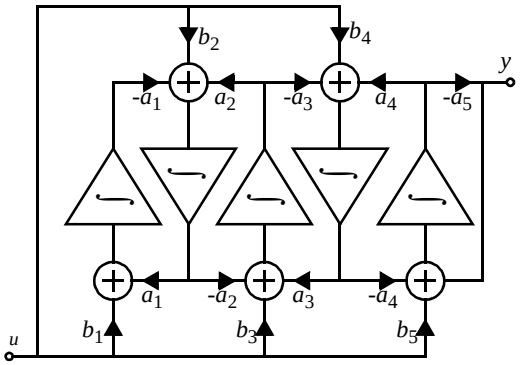

Figure 5. 5th order orthonormal ladder filter structure with multiple feedins.

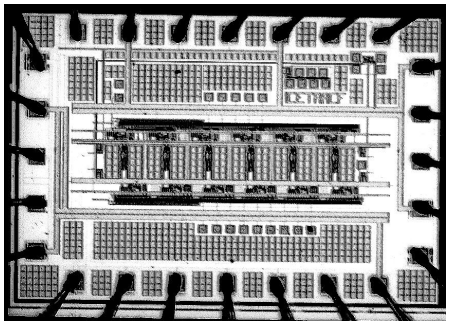

Figure 6. Die photo of prototype.

To demonstrate the programmability of the filter and measure linearity, noise, SFDR, etc., the orthonormal ladder was configured as a 5th order lowpass filter. The magnitude responses with the filter reprogrammed with different cutoff frequencies and dc gains are plotted in Fig. 8. Three-dB frequencies up to 45 MHz are observed. The cutoff is not as sharp as one would expect from a 5th order filter because the nominal values of the feedin and feedback transconductors, a_i and b_i, are unpredictable and not necessarily well matched. In an adaptive application, the filter parameters would be automatically optimized by the adaptive algorithm.

4. CONCLUSIONS

Techniques for implementing a 5th order digitally programmable filter in a 0.25 µm CMOS process were described for analog adaptive filtering applications. The measured results from a prototype implementation of the filter are summarized in Table 1.

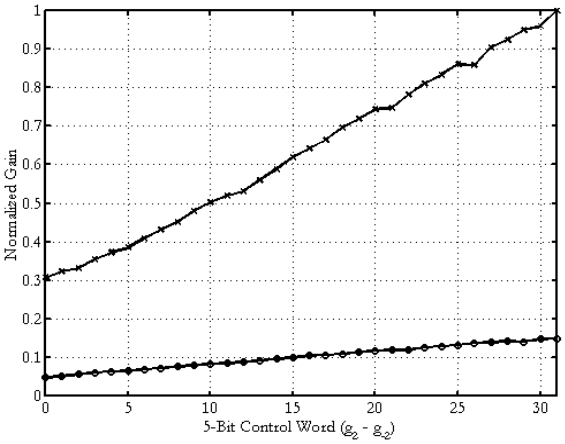

Figure 7. Normalized gain Gm1 in Fig. 4 vs. digital control word. The output current mirror gain is $M = 1$ for the top curve (×) and $M = 1/4$ for the lower curve (O).

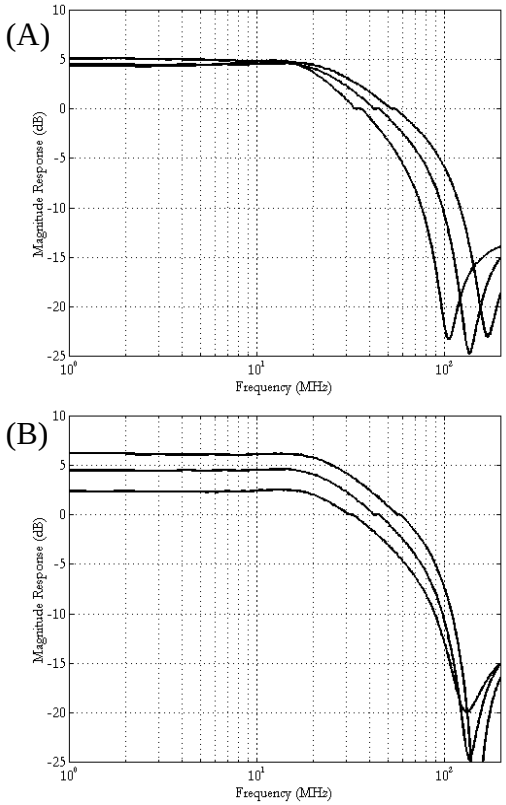

Figure 8. Measured frequency responses of the orthonormal ladder as a lowpass filter with (A) varying cutoff frequency and (B) varying dc gain.

Traditional transconductor and Miller integrator circuits were redesigned with only NMOS devices in the signal path to take advantage of their superior speed. A major limitation of transconductor circuits which rely on differential pairs which are source-degenerated by a triode MOS device is that their transconductance and linearity depend upon the input common mode level. Therefore, strongly inverted triode devices should be used to reduce this dependence, or the MOS devices should be replaced by passive resistors.

Poor linearity was measured in the 5th order filter due to imbalances in the fully-differential circuits. However, the circuit techniques demonstrated their potential for moderate linearity in the first-order case. The 5th-order filter was still useful as a vehicle for testing digital adaptation algorithms on analog filters [7].

Entire Prototype Gm-C Filter IC	
Technology	0.25 µm CMOS
Supply Voltage	2.5 V
Integrated Area	2.5 mm × 1.7 mm = 4.25 mm^2
Power	233 mW (Simulated) 250 mW (Measured)
First Order Filter Test Structure	
THD at 8 MHz, 200 mV_{pp} input, 125 mV_{pp} output	-41 dB
5th Order Lowpass Orthonormal Ladder Filter	
Integrated Area	1.25 mm × 0.38 mm = 0.469 mm^2
Power Consumption	87.5 mW (Simulated)[a]
Noise Power	1.656 mVrms
THD at $f_{3\,dB}/2 = 18$ MHz, 125 mVpp input, 170 mVpp output	-27.7 dB[b]
SFDR with input tone at $f_{3\,dB}/2$	30 dB

Table 1. Summary of prototype filter IC measurements.

a. Includes shared bias circuitry.

b. Measurements for different transfer functions varied between -20 dB and -30 dB.

5. REFERENCES

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