A 20-Gb/s Coaxial Cable Receiver Analog Front-End in 90-nm CMOS Technology

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Receiver AFE Specifications

- 20-Gb/s operation
- 75-ohm input (cable impedance)
- 50-ohm output (testing)
- External gain and equalization control (non-adaptive)
- < 0.5 mV_{rms} input-referred noise
- 90-nm CMOS, 1.3-V supply

Basic transceiver link.
AFE Block Diagram

- **Broadband Preamplifier**
  - CM: 0.55 V
  - Input: 60 mVpp

- **S2D**
  - 0.75 V

- **Analog Equalizer**
  - Gain (DIFF): 7.5 dB (SE)
  - Bandwidth: 11.6 GHz
  - Swing/side: 140 mVpp
  - Power: 26 mW
  - 0.95 V

- **Post-Amplifier**
  - 0.95 V
  - Variable
  - 70–185 mVpp
  - 31 mW

- **Output Driver**
  - 0.90 V
  - 0–6.5 dB
  - > 19.6 GHz
  - 145–190 mVpp
  - 23 mW

- 0.95 V

- **eq_ctl**

- **r_ctl**

Gain (DIFF): 8.3 dB
Bandwidth: 19 GHz
Swing/side: 185 mVpp
Power: 42 mW
Design - Broadband Preamplifier

- Shunt-feedback TIA stages have recently been used as low-noise broadband preamplifiers.
- TIA topologies were narrowed down to 1) nMOS TIA with common source (CS) and 2) nMOS TIA with active bias, and compared in simulation.

Shunt-feedback TIA topology. 
\[ Rin = \frac{R_f}{1+|A|} \]

Topology: nMOS TIA with CS. The CS stage provides gain and level-shifting.

Topology: nMOS TIA with active bias. The CS stage is removed, \( M_3 \) added to raise the output CM.
Design - Broadband Preamplifier

- Simulation comparison results:

nMOS TIA with active bias (solid) and nMOS TIA with CS (dashed). Both topologies were designed to have the same $A_{DC}$ and BW. At 10 GHz, active-bias topology has 0.5-dB lower NF and 50% higher input $P_{1dB}$. 

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• By increasing $R_l$, the nMOS TIA with CS can have significantly larger gain, and so is preferable where large voltage gain is desired.
• In this work, the output is linearly processed by the rest of the AFE. Based on the previous simulation comparison, the nMOS TIA with active bias was used.

Design - Broadband Preamplifier

nMOS TIA with CS.

nMOS TIA with active bias.
Design - Broadband Preamplifier

- Implemented nMOS TIA with active bias.
- Dummy stage used for power supply rejection.
• Simulation results:

\[ |S_{11}|, \text{ NF and NF}_{\text{MIN}}. \]
\[ |S_{11}| < -15 \text{ dB up to 16.6 GHz,} \]
\[ \text{NF @ 10 GHz} = 5.8 \text{ dB.} \]

AC gain (single-ended input).
\[ A_{\text{DC}} = 7.5 \text{ dB, BW} = 11.6 \text{ GHz.} \]
Design – Equalizer

- Implemented split-path equalizer.

\[
A_{EQ}(s) = \frac{A_{DC}(1 + s/\omega_{z1})}{(1 + s/\omega_{p1})},
\]

\[
A_{DC} = g_{m1,2}g_{m5,6}R_{1,2}R_{5,6}
\]

\[
\omega_{z1} = \frac{R_{3,4}}{L_{3,4}(1 + g_{m7,8}g_{m3,4}R_{3,4}/g_{m5,6}g_{m1,2}R_{1,2})}
\]

\[
\omega_{p1} = \frac{R_{3,4}}{L_{3,4}}
\]

\[
\begin{align*}
R1 & \quad R2 & \quad R3 & \quad R4 \\
M1 & \quad M2 & \quad M3 & \quad M4 \\
\text{Lp} & \quad \text{lp} & \quad \text{h} & \quad \text{hp} \\
\text{eq_ctl} & \quad \text{eq_ctl} & \quad \text{eq_ctl} & \quad \text{eq_ctl}
\end{align*}
\]

LP Path  HP Path  Weighted Sum
Design – Equalizer

- Low-pass and high-pass paths are combined:

AC gains for various equalizer settings on linear and log scales. $A_{DC} = -8.6 - 0.3$ dB, maximum peaking = 8.6 dB.
• Post-amplifier uses three cascaded source-degenerated stages, providing some gain-control.

\[ A_{DC} = 0 - 6.5 \text{ dB}, \text{ BW} \geq 19.6 \text{ GHz} \]
**Design – AFE**

- Simulation results - $|S_{21}|$:

AFE: Simulated single-ended $|S_{21}|$ for maximum (top) and minimum (bottom) post-amplifier gains across equalizer setting.
### Design – AFE

#### Simulation results - summary:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>S_{11}</td>
</tr>
<tr>
<td>Peaking @ 10 GHz</td>
<td>4.6 dB</td>
</tr>
<tr>
<td>Gain control range</td>
<td>6.8 dB</td>
</tr>
<tr>
<td>$P_{1dB}$ @ 10 GHz (Excluding output driver)</td>
<td>105 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
</tr>
<tr>
<td>min EQ, min post-amp. gain</td>
<td>98 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
</tr>
<tr>
<td>max EQ, max post-amp. gain</td>
<td></td>
</tr>
<tr>
<td>NF @ 10 GHz</td>
<td>12.9 dB</td>
</tr>
<tr>
<td>Differential output noise (max EQ, max post-amp. gain)</td>
<td>2.0 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
<tr>
<td>Input-referred noise (max EQ, max post-amp. gain)</td>
<td>0.36 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
<tr>
<td>Input sensitivity @ BER = 10&lt;sup&gt;-15&lt;/sup&gt;</td>
<td>5.7 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
</tr>
</tbody>
</table>
Measurements

- Power/Area: 138 mW/0.89 mm$^2$
S Parameter Measurements

- $|S_{11}|, |S_{22}| < -10 \text{ dB}$ up to 16, 20 GHz, respectively (converted from 50-ohm to 75/50-ohm input/output environment)
Transient Measurements

- 16.25 Gb/s, 9-ft SMA cable
- Launch amplitude ~ 47 mV

Potential TX power savings

- -5.7 dB @ 8.125 GHz

Graph showing frequency response with markers for 10 mV/div and 50 mV/div.
Transient Measurements

- 20.4 Gb/s, 9-ft SMA cable
- Launch amplitude ~ 47 mV

Potential TX power savings

![Graph showing signal attenuation with frequency]

| Frequency [GHz] | $|S_{21}|$ [dB] |
|-----------------|-------------|
| 5               | -10         |
| 10              | -15         |
| 15              | -20         |
| 20              | -25         |
| 25              | -30         |
| 30              | -35         |

-7.5 dB @ 10.2 GHz
# Measurement Summary

<table>
<thead>
<tr>
<th>Technology/Supply</th>
<th>Power/Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology/Supply</td>
<td>90-nm CMOS/1.3 V</td>
</tr>
<tr>
<td>Power/Area</td>
<td>138 mW/0.89 mm²</td>
</tr>
</tbody>
</table>

| $|S_{11}|$, $|S_{22}|$ | Maximum Peaking |
|-----------------|------------------|
| -10 dB up to 16, 20 GHz | 6.5 dB @ 8 GHz |
| 6.0 dB | ≥ 294 GHz |

<table>
<thead>
<tr>
<th>GBW Product (differential)</th>
<th>1 GHz</th>
<th>7 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{1dB}$</td>
<td>$-30.75$ dBm</td>
<td>$-31.6$ dBm</td>
</tr>
<tr>
<td>(no EQ, min gain)</td>
<td>$-39.75$ dBm</td>
<td>$-38.6$ dBm</td>
</tr>
<tr>
<td>(no EQ, max gain)</td>
<td>$-36.75$ dBm</td>
<td>$-35.6$ dBm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Rate</th>
<th>16.25 Gb/s</th>
<th>20.4 Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>9-ft SMA Cable Loss</td>
<td>5.7 dB @ 8.125 GHz</td>
<td>7.5 dB @ 10.2 GHz</td>
</tr>
<tr>
<td>Input Swing (single-ended)</td>
<td>40 mV$_{pp}$</td>
<td>40 mV$_{pp}$</td>
</tr>
<tr>
<td>Output Swing (single-ended)</td>
<td>225 mV$_{pp}$</td>
<td>225 mV$_{pp}$</td>
</tr>
<tr>
<td>RMS Jitter</td>
<td>2.5 ps</td>
<td>2.7 ps</td>
</tr>
<tr>
<td>Timing Margin (BER = 10$^{-12}$)</td>
<td>0.58 UI</td>
<td>0.32 UI</td>
</tr>
</tbody>
</table>
### Comparison - Equalizers

<table>
<thead>
<tr>
<th>Reference</th>
<th>[ZG05]</th>
<th>[HMC+05]</th>
<th>[GLTR05]</th>
<th>[Lee06]</th>
<th>[TKO+05]</th>
<th>[SC06]</th>
<th>[LL08b]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit Rate (Gb/s)</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>20</td>
<td>10</td>
<td>30</td>
<td>40</td>
<td>20.4</td>
</tr>
<tr>
<td>Loss¹ (dB)</td>
<td>13</td>
<td>18</td>
<td>19</td>
<td>9.5</td>
<td>20</td>
<td>14.5</td>
<td>10</td>
<td>7.5</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>3.3</td>
<td>1.8</td>
<td>1.2</td>
<td>1.5</td>
<td>1.2</td>
<td>1</td>
<td>–</td>
<td>1.3</td>
</tr>
<tr>
<td>EQ Power (mW)</td>
<td>155</td>
<td>7.3</td>
<td>25</td>
<td>60</td>
<td>13.2</td>
<td>25</td>
<td>58</td>
<td>31 (sim.)</td>
</tr>
<tr>
<td>Adaptive</td>
<td>YES</td>
<td>NO</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Type²</td>
<td>SP</td>
<td>4-FIR</td>
<td>CD</td>
<td>CD</td>
<td>CH</td>
<td>3-FIR</td>
<td>SP+CD</td>
<td>SP</td>
</tr>
<tr>
<td>Process</td>
<td>0.18-um BiCMOS</td>
<td>0.18-um CMOS</td>
<td>0.13-um CMOS</td>
<td>0.13-um CMOS</td>
<td>0.11-um CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.705</td>
<td>–</td>
<td>0.162 (CORE)</td>
<td>0.2 (CORE)</td>
<td>0.004 (EQ)</td>
<td>0.3</td>
<td>0.539</td>
<td>0.891</td>
</tr>
</tbody>
</table>

¹ Loss compensated at one-half the symbol rate.
² SP: split-path; CD: capacitive-degeneration; CH: Cherry-Hooper.
## Comparison – CMOS Amplifiers

<table>
<thead>
<tr>
<th>Reference</th>
<th>[GR04]</th>
<th>[SSH+04]</th>
<th>[CL07]</th>
<th>[WSJ06]</th>
<th>[LL08a]</th>
<th>[LWL+05]</th>
<th>[TWKC05]</th>
<th>This Work</th>
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</thead>
<tbody>
<tr>
<td>Bit Rate (Gb/s)</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>N/A</td>
<td>N/A</td>
<td>20.4</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>2.2</td>
<td>1.8</td>
<td>2.8</td>
<td>1</td>
<td>1.2</td>
<td>2.4</td>
<td>–</td>
<td>1.3</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>190</td>
<td>140</td>
<td>250</td>
<td>80</td>
<td>75</td>
<td>120</td>
<td>122</td>
<td>138</td>
</tr>
<tr>
<td>Diff. Gain (dB)</td>
<td>15</td>
<td>4</td>
<td>20</td>
<td>20</td>
<td>26</td>
<td>7.4</td>
<td>7</td>
<td>31.2</td>
</tr>
<tr>
<td>BW (GHz)</td>
<td>22</td>
<td>39</td>
<td>39.4</td>
<td>23</td>
<td>22</td>
<td>80</td>
<td>70</td>
<td>8.1</td>
</tr>
<tr>
<td>GBP (GHz)</td>
<td>124</td>
<td>62</td>
<td>394</td>
<td>230</td>
<td>440</td>
<td>188</td>
<td>157</td>
<td>294</td>
</tr>
<tr>
<td>VGA</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>Type¹</td>
<td>CGS</td>
<td>DA</td>
<td>DA</td>
<td>CGS</td>
<td>CGS</td>
<td>DA</td>
<td>DA</td>
<td>CGS</td>
</tr>
<tr>
<td>Process</td>
<td>0.18-um CMOS</td>
<td>0.18-um CMOS</td>
<td>0.18-um CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.5</td>
<td>3.3</td>
<td>2.24</td>
<td>0.033 (CORE)</td>
<td>0.56</td>
<td>0.72</td>
<td>0.72</td>
<td>0.891</td>
</tr>
</tbody>
</table>

¹ CGS: cascaded gain stage; DA: distributed amplifier.
Conclusion

• A binary receiver AFE targeting 20 Gb/s for coaxial cable was designed in 90-nm CMOS.
• The nMOS TIA with active bias used as the preamplifier had not previously been implemented in CMOS.
• Main AFE blocks were the broadband preamplifier, analog (split-path) peaking equalizer and post-amplifier, and functionality was verified by measurement up to 20.4 Gb/s.
Backup Slides
Equalizer Comparison

- Capacitive-degeneration (CD) and split-path (SP) equalizers have similar transfer functions, but the SP equalizer was chosen due to 1) the absence of varactor models and 2) potentially greater single-stage peaking.

\[
A_{CD}(s) = A_{DC}(1 + s/\omega_z)/(1 + s/\omega_p)
\]

\[
A_{DC} = g_{m1}R_1/(1 + g_{m1}R_s)
\]

\[
\omega_z = 1/C_sR_s
\]

\[
\omega_p = (1 + g_{m1}R_s)/C_sR_s
\]

\[
A_{SP}(s) = A_{DC}(1 + s/\omega_z)/(1 + s/\omega_p)
\]

\[
A_{DC} = g_{m1}g_{m3}R_1R_3
\]

\[
\omega_z = R_2/L(1+g_{m4}g_{m2}R_2/g_{m3}g_{m1}R_1)
\]

\[
\omega_p = R_2/L
\]
Equalizer Comparison

- The split-path (SP) equalizer actually has a 2\textsuperscript{nd} order transfer function due to the “tank” capacitance $C_p$:

\[ A_3 = g_{m3} g_{m_1} R_1 R_3, \]
\[ A_4 = g_{m4} g_{m_2} R_3 R_2, \]
\[ \omega_0 = \sqrt{\frac{1}{LC_p}} \]
\[ Q = \omega_0 C_p R_2 \]
\[ \text{Boost Ratio} = \frac{A(\omega_0)}{A(\omega_0)} = 1 + \frac{A_4}{A_3} = 1 + \frac{g_{m4} g_{m_2} R_2}{g_{m3} g_{m_1} R_1} \]

Equalizer transfer function (2\textsuperscript{nd} order).

\[ A_{SP}(s) = A_{DC}(1 + s/\omega_{z1})/(1 + s/\omega_{p1}) \]
\[ A_{DC} = g_{m1} g_{m_3} R_1 R_3 \]
\[ \omega_{z1} = R_2/L(1+g_{m4} g_{m_2} R_2/g_{m3} g_{m_1} R_1) \]
\[ \omega_{p1} = R_2/L \]

Equalizer transfer function (1\textsuperscript{st} order).

Note that the boost ratio from the 2\textsuperscript{nd} order transfer function is equal to $\omega_{p1}/\omega_{z1}$ derived using the 1\textsuperscript{st} order expressions. This implies that both expressions predict the same amount of gain boost relative to DC.
Alternative 1: Post-amplifier before the equalizer. This may be better for noise, since the post-amplifier gain is closer to the input side (and the equalizer has loss). However, this would require a larger equalizer input-swing limit.

Alternative 2: VGA integrated with (or before) the broadband preamplifier. This is probably best in terms of noise, as the required gain is at the front. However, only gain reduction is easily implemented here. Subsequent gain stages would still likely be required. Input matching might be affected.
Design – Broadband Preamplifier

- Noise contribution of the active bias device (M3):

\[
v_{n,M_3}^2 = (I_{n,M_3})^2
\]

\[
|A_v|^2 = \left( \frac{1}{R_S} \right)^2 + \left( \frac{1}{R_f} \right)^2 + \left( \frac{1}{r_{o1}r_{o2}} \right)^2 \left( \frac{1}{sC_3} \right)^2
\]

\[
|A_v|^2 = \left( \frac{1}{R_S} \right)^2 + \left( \frac{1}{R_f} \right)^2 + \left( \frac{1}{r_{o1}r_{o2}} \right)^2 \left( \frac{1}{sC_3} \right)^2
\]

\[
|A_v|^2 = \left( \frac{1}{R_S} \right)^2 + \left( \frac{1}{R_f} \right)^2 + \left( \frac{1}{r_{o1}r_{o2}} \right)^2 \left( \frac{1}{sC_3} \right)^2
\]

Noise of M3 referred to vs:

\[
v_{n,M_3,\text{in}}^2(f) = 4kTg_{m3} + \frac{K_N}{C_{ox}W_3L_3f} g_{m3}^2 R_S^2
\]

\[
\left( R_S \right) Z_F \|| r_{o3} \|| \frac{1}{sC_1} \|| \frac{1}{sC_2} \|
\]

\[
\left( R_S \right) Z_F \|| r_{o3} \|| \frac{1}{sC_1} \|| \frac{1}{sC_2} \|
\]

\[
\left( R_S \right) Z_F \|| r_{o3} \|| \frac{1}{sC_1} \|| \frac{1}{sC_2} \|
\]
Design – S2D

- Single-ended to differential (S2D) block is used as the preamplifier has no common-mode (CM) rejection.

\[ A_{DC} = 8.3 \text{ dB}, \quad BW = 19.0 \text{ GHz}. \]

\[ A_{CM} @ 10 \text{ GHz} = -21.5 \text{ dB}. \]
Design – S2D

- Simulation results:

  - AC gain (single-ended input).
    \[ A_{DC} = 8.3 \text{ dB}, \text{ BW} = 19.0 \text{ GHz}. \]

  - CM gain.
    \[ A_{CM@10 \text{ GHz}} = -21.5 \text{ dB}. \]
Simulation results:

\[ \Delta R_{\text{triode}} (\text{at } V_{\text{DS}} = 50 \text{ mV}) = 3.8\% \]

**A\textsubscript{DC} = 0 - 6.5 dB, BW \geq 19.6 GHz**

Resistance of triode-region nMOS vs. \( V_{\text{DS}} \) for various values of \( r_{\text{ctl}} \).

\( \Delta R_{\text{triode}} (\text{at } V_{\text{DS}} = 50 \text{ mV}) \) is 3.8\%.
The output driver provides \( \sim 0 \)-dB gain to the 50-ohm testing environment.

\[ A_{DC} = 0.4 \text{ dB}, \quad \text{BW} = 25.6 \text{ GHz} \]
• Simulation results - linearity:

Gain compression at 10 GHz.

<table>
<thead>
<tr>
<th>VGA</th>
<th>EQ</th>
<th>$P_{1dB} @ 10,\text{GHz}$</th>
<th>$P_{1dB} @ 10,\text{GHz}$ (no output driver)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>Min</td>
<td>82 mV$_{pp}$</td>
<td>105 mV$_{pp}$</td>
</tr>
<tr>
<td>Min</td>
<td>Max</td>
<td>93 mV$_{pp}$</td>
<td>108 mV$_{pp}$</td>
</tr>
<tr>
<td>Max</td>
<td>Min</td>
<td>54 mV$_{pp}$</td>
<td>87 mV$_{pp}$</td>
</tr>
<tr>
<td>Max</td>
<td>Max</td>
<td>68 mV$_{pp}$</td>
<td>98 mV$_{pp}$</td>
</tr>
</tbody>
</table>

Single-ended input $P_{1dB} @ 10\,\text{GHz}$.
Design – AFE

- Simulation results - noise:

AFE: Simulated single-ended NF for maximum (left) and minimum (right) VGA gains across equalizer setting.

<table>
<thead>
<tr>
<th>VGA</th>
<th>EQ</th>
<th>Input-referred noise</th>
<th>Differential output noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>Min</td>
<td>0.22 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>1.6 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
<tr>
<td>Min</td>
<td>Max</td>
<td>0.49 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>1.3 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
<tr>
<td>Max</td>
<td>Min</td>
<td>0.18 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>3.0 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
<tr>
<td>Max</td>
<td>Max</td>
<td>0.36 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>2.0 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
</tbody>
</table>

AFE: Simulated noise voltages at the limits of VGA and equalizer controls.
Design – AFE

- Simulation results - noise:

AFE: Simulated single-ended NF for maximum (left) and minimum (right) VGA gains across equalizer setting.

AFE: Simulated noise voltages at the limits of VGA and equalizer controls: differential output noise (left) and single-ended available input-referred noise (right).
Design – AFE

• Simulation results - transients:

AFE: Simulated single-ended input and differential output eye diagrams: 15-m cable at 16.6 Gb/s (top), and 20 Gb/s (bottom).
Measurement Setup

PC
NI PCI-6733
NI BNC-2110 Connector Block
DC bias/control

AFE

50 ohm

S parameter Setup
HP 8510C VNA
(45 MHz – 26.5 GHz)
Port 1 Port 2

Transient Setup
HP 83650B
Signal Generator
(10 MHz – 50 GHz)

Pattern Generator Setup
Centellax Boards:
2x OTB3P1A 10–Gbps PRBS
UXC40M Divider
MS4S1M 4-to-1 Mux

Channel

Agilent 86100C Infinium DCA–J Wideband Oscilloscope

Precision Timebase

CH3 CH4
**Linearity Measurements**

Measured (markers) and simulated (no markers) $P_{1\text{dB}}$ at 1- and 7-GHz.

<table>
<thead>
<tr>
<th>AFE Setting</th>
<th>$P_{1\text{dB}}$ at 1-GHz [dBm]</th>
<th>$P_{1\text{dB}}$ at 7-GHz [dBm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>no EQ, min gain</td>
<td>-30.8</td>
<td>-31.6</td>
</tr>
<tr>
<td>no EQ, max gain</td>
<td>-39.8</td>
<td>-38.6</td>
</tr>
<tr>
<td>max EQ, max gain</td>
<td>-36.8</td>
<td>-35.6</td>
</tr>
</tbody>
</table>