

Design Considerations for Continuous-Time Bandpass ADCs

Richard Schreier
Oct 24 2005



Outline

- 1 An ADC Figure-of-Merit
- 2 Overview of Bandpass ADCs
- 3 A High-Q Active-RC Resonator
- 4 IDAC Design Considerations
 - Thermal noise
 - Switching dynamics

1

2

An ADC Figure-of-Merit?

- Is an ADC which has SNR = 100 dB over BW = 1 MHz fundamentally better or worse than an ADC which has SNR = 90 dB over the same bandwidth, if ADC1 consumes 1 W while ADC2 consumes 100 mW?

3

An ADC Figure-of-Merit?

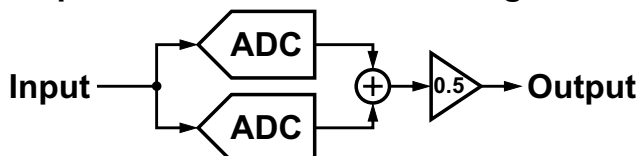
- More generally, what is the fundamental trade-off between

Bandwidth (BW),
Dynamic Range (DR)
and
Power consumption (P)
?

4

DR-P Trade-Off: Part 1

- To increase DR at the expense of P, parallel two ADCs and average:



- Averaging reduces noise by a factor of $\sqrt{2}$: DR += 3 dB
Assuming the ADCs' noises are uncorrelated
- But uses twice the power: P += 3 dB

5

DR-P Trade-Off: Part 2

- To reduce P at the expense of DR, "cut the ADC in half"

May not be practical if the ADC is already small, but if it can be done,
P -= 3 dB & DR -= 3 dB

- \therefore For an ADC of some BW,
x dB in DR costs x dB in P,
or
DR (in dB) - 10log₁₀(P) = const

6

Q: Is This Trade-Off Optimal?

- **A: Yes, because it is bi-directional**
The fact that you can (in principle) go both ways for any ADC means that no other trade-off can exist for ADCs that are optimal.
- **Consider a (supposedly) optimal ADC that can get more than 3 dB increase in DR for a doubling of P**
Double P, then cut that ADC in half.
The resulting ADC has the same P as the original, but more DR.

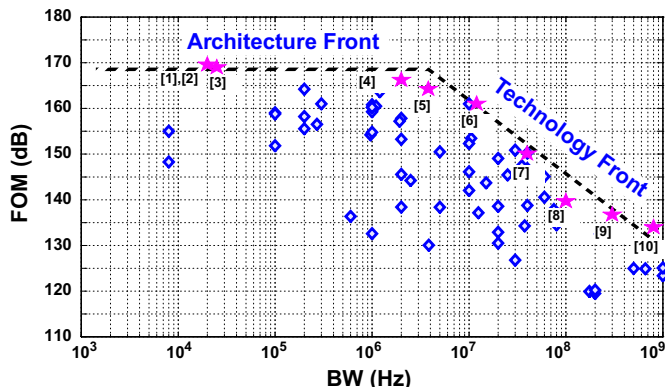
7

What About BW?

- **Reducing BW by a factor of 2 increases DR by 3 dB but leaves P alone**
Assuming the noise is white (distortion is not dominant) and that digital filtering takes no power.
- **Time-interleaving two ADCs doubles BW and doubles P, but leaves DR unchanged**
I/Q processing does the same.
Assumes that interleaving is perfect (can be calibrated).

9

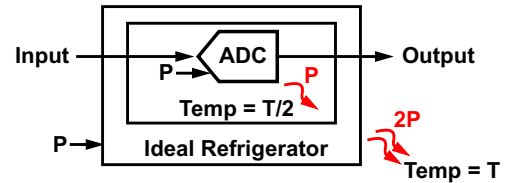
State-of-the-Art FOM



11

DR-P Trade-Off: Part 1b

- **Can increase DR by 3 dB by reducing T by a factor of 2:**



- **But this also costs twice the power**

8

Resulting FOM

- **Use a dB scale:**
$$FOM = (DR)_{dB} + 10 \log \frac{BW}{P}$$
- **For a given FOM, factors of 2 in BW or P are equivalent to a 3-dB change in DR**
- **Should really include T, but since T is usually 300K, omit it**
Steyaert et al. like
$$FOM = \frac{4kT \times DR \times 2BW}{P}$$

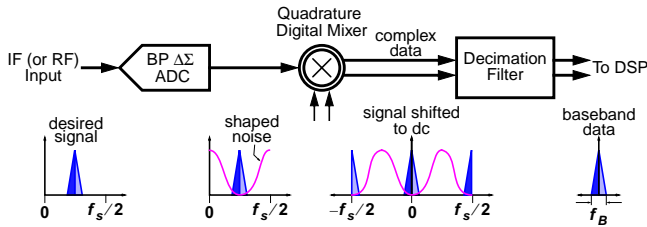
10

References

- [1] Y. Yang, A. Chokhawala, M. Alexander, J. Melanson, and D. Hester, "A 114 dB 68 mW chopper-stabilized stereo multi-bit audio A/D converter," *ISSCC Digest of Technical Papers*, pp. 64-65, Feb. 2003.
- [2] L. Yao, M. Steyaert and W. Sansen, "1V 88dB 20kHz $\Sigma\Delta$ modulator in 90nm CMOS," *ISSCC Digest of Technical Papers*, pp. 80-81, February 2004.
- [3] S. Rabii, and B. A. Wooley, "A 1.8-V digital-audio sigma-delta modulator in 0.8 μ m CMOS," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, pp. 783-796, June 1997.
- [4] K. Vleugels, S. Rabii, and B. A. Wooley, "A 2.5-V sigma-delta modulator for broadband communications applications," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1887-1899, Dec. 2001.
- [5] R. H. M van Veldhoven, "A tri-mode continuous-time $\Sigma\Delta$ modulator with switched-capacitor feedback DAC for a GSMEDGE/CDMA2000/UMTS receiver," *ISSCC Digest of Technical Papers*, pp. 60-61, Feb. 2003.
- [6] M. Moyal, M. Groepl, H. Werker, G. Mitteregger and J. Schambacher, "A 700/900mW/channel CMOS dual analog front-end IC for VDSL with integrated 11.5/14.5dBm line drivers," *ISSCC Digest of Technical Papers*, pp. 416-417, Feb. 2003.
- [7] C. R. Grace, P. J. Hurst and S. H. Lewis, "A 12b 80MS/s pipelined ADC with bootstrapped digital calibration," *ISSCC Digest of Technical Papers*, pp. 460-461, Feb. 2004.
- [8] B. Hernes, A. Briskemyr, T. N. Andersen, F. Telsta, T. E. Bonnerud and O. Moldsvor, "A 1.2V 220MS/s 10b pipeline ADC implemented in 0.13 μ m Digital CMOS," *ISSCC Digest of Technical Papers*, pp. 256-257, Feb. 2004.
- [9] G. Geelen and E. Paulus, "An 8b 600MS/s 200mW CMOS folding A/D converter using an amplifier preset technique," *ISSCC Digest of Technical Papers*, pp. 254-255, Feb. 2004.
- [10] R. Taft, C. Menkus, M. R. Tursi, O. Hidri, V. Pons, "A 1.8V 1.6GS/s 8b self-calibrating folding ADC with 7.26 ENOB at Nyquist frequency," *ISSCC Digest of Technical Papers*, pp. 252-253, Feb. 2004.

12

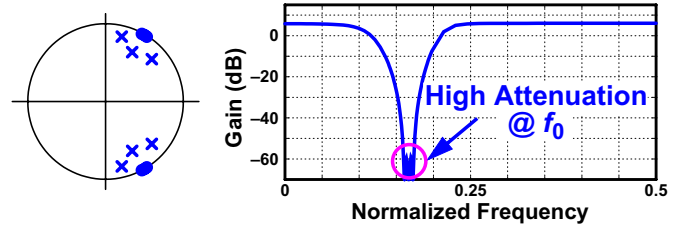
A Bandpass $\Delta\Sigma$ ADC System



- ADC outputs noise-shaped data
- DSP translates signal to baseband and removes out-of-band noise

13

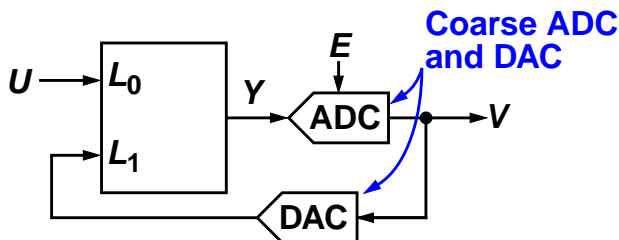
Bandpass NTF



- NTF attenuates quantization noise in the band of interest

14

Generic $\Delta\Sigma$ ADC



$$Y = L_0 U + L_1 V$$

$$V = Y + E$$

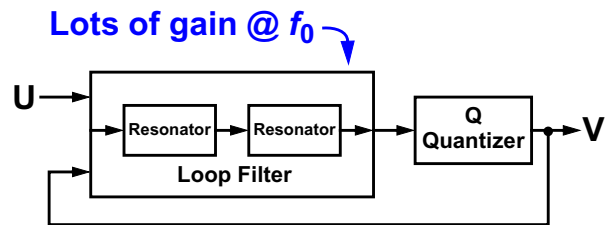
$$\Rightarrow V = GU + HE, \text{ where } H = \frac{1}{1 - L_1}, G = L_0 H$$

inverse relations: $L_1 = 1 - 1/H, L_0 = GH$

- Poles of L_1 are the zeros of H

15

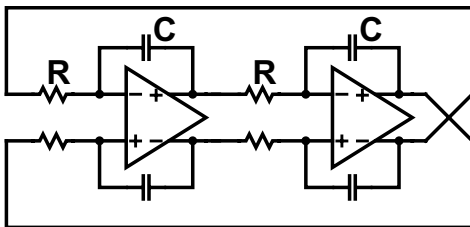
A Bandpass $\Delta\Sigma$ ADC



- Quantization noise is suppressed at frequencies where the loop gain is large
- Need high-Q resonances to get deep nulls

16

Active-RC Resonator

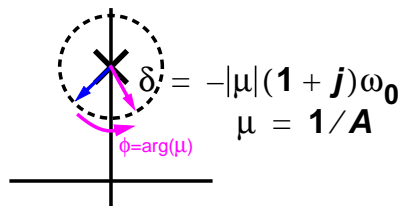


- + Amenable to integration; Readily tuned over several octaves
- Amplifier drives R and C

17

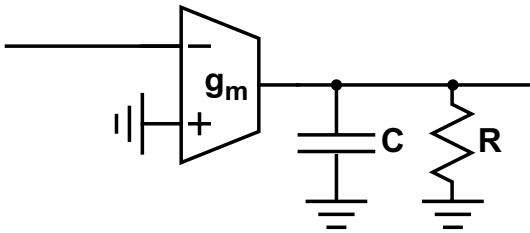
Amplifier Gain and Phase

- Finite gain degrades Q
- Phase lag enhances Q
- Analysis shows $\phi = 45^\circ$ yields high Q, independent of amplifier gain



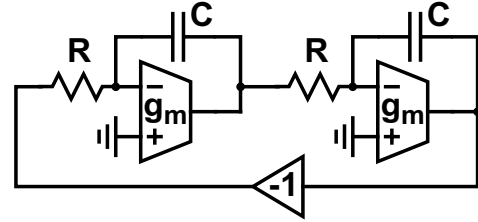
18

A Circuit With $\phi = 45^\circ @ f_0$



19

Resulting High-Q Resonator

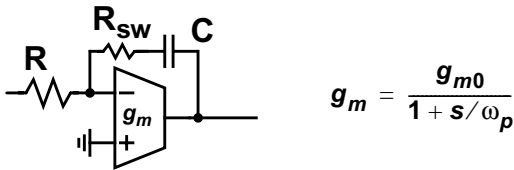


- Amplifier load yields $45^\circ @ f_0$
- Finite gm shifts the pole frequency, but does not degrade Q!

20

Finite g_m Bandwidth & Non-zero Switch Resistance

- Switch resistance degrades Q
- Finite gm bandwidth enhances Q

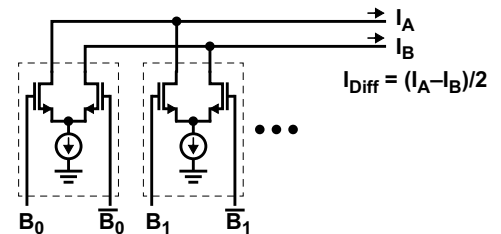


$$g_m = \frac{g_{m0}}{1 + s/\omega_p}$$

- Cancellation occurs if $R_{sw} = \frac{2\omega_0}{g_{m0}(\omega_p)}$

21

Current-Mode DAC (IDAC)



- Excellent spectral performance
“-80 dBc IMD to 300 MHz”
[Schofield et al., ISSCC 2003]

22

IDAC SNR/Power Limit

- Assume square-law operation
i.e. $I_{FS} = K(\Delta V)^2$.
- The power of a -3-dBFS signal is
 $S^2 = (0.5(I_{FS}/2)^2)/2 = K^2(\Delta V)^4/16$
- While the noise in bandwidth B is
 $N^2 = (4kTBK\Delta V)/3$

$$\Rightarrow \left(\frac{S}{N}\right)^2 = \frac{3I_{FS}\Delta V}{64kTB}$$

23

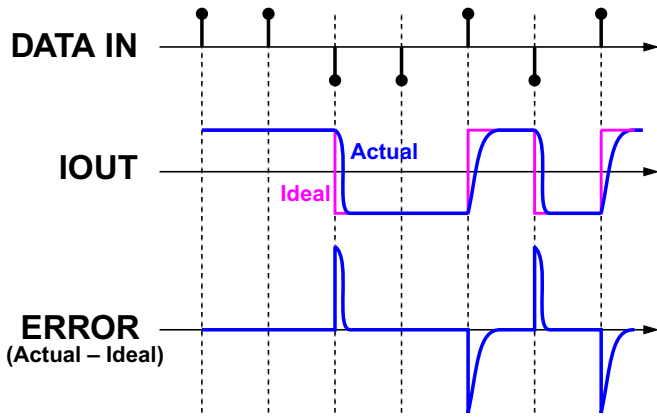
IDAC SNR/Power Limit (cont'd)

$$\left(\frac{S}{N}\right)^2 = \frac{3I_{FS}\Delta V}{64kTB}$$

- “DAC SNR is proportional to the power allocated to its current sources”
- For example, to get $SNR = 100$ dB with $B = 5$ MHz and $\Delta V = 300$ mV requires (at least) $I_{FS} = 15$ mA

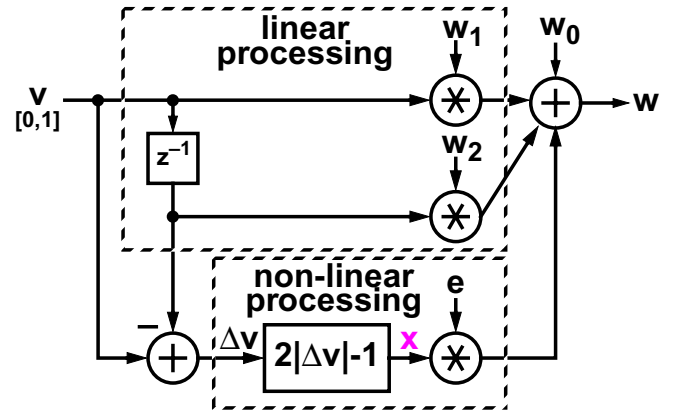
24

Switching Dynamics



25

Model of Dynamic Nonlinearity



26

Model Equations

$$\begin{bmatrix} w_0 \\ w_1 \\ w_2 \\ e \end{bmatrix} = \begin{bmatrix} \frac{3}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ \frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4} \end{bmatrix} \begin{bmatrix} w_{00} \\ w_{01} \\ w_{10} \\ w_{11} \end{bmatrix}$$

where w_{00} , w_{01} , w_{10} and w_{11} are the output waveforms in response to 00, 01, 10 and 11 data inputs.

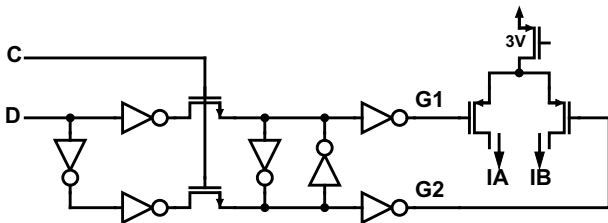
$$e = 0.25[(w_{01} + w_{10}) - (w_{00} + w_{11})]$$

27

Zero error if the rise and fall waveforms are perfectly complementary

28

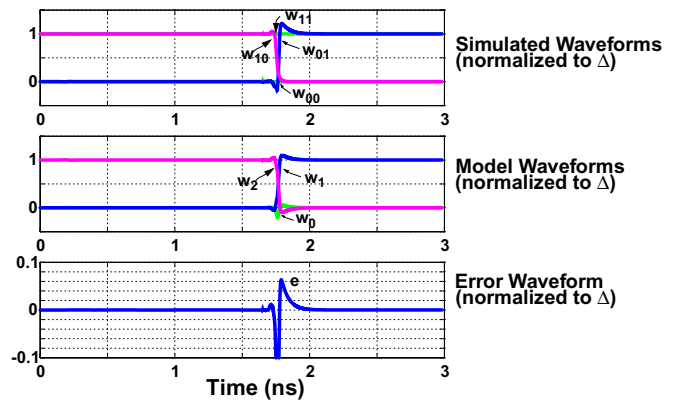
DAC Example



- 3V PMOS for low noise
- Symmetric drive for symmetric switching

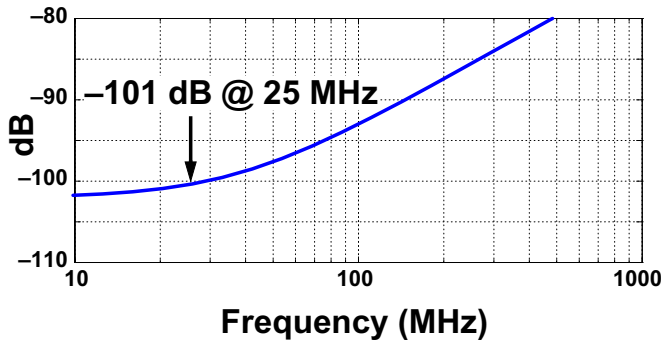
29

Simulated Single-Ended W*



30

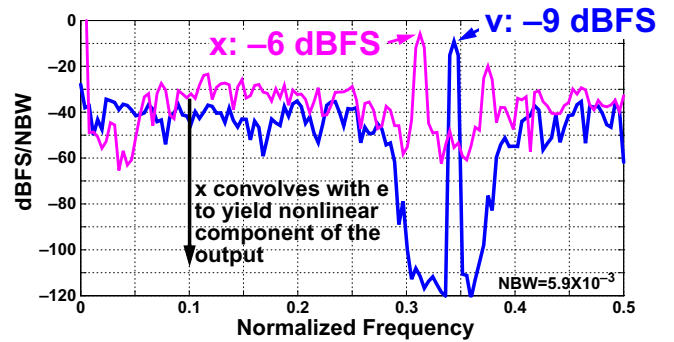
Fourier Transform of E



31

Example Spectra in Model

33-level v sequence; $f_0 = f_s/3$; no MS



32

E.g. SFDR Calculation

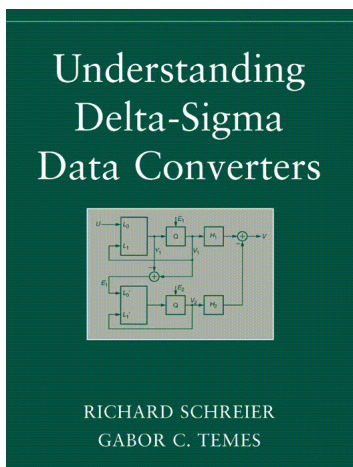
- The signal level is $-9 \text{ dBFS} - 2 \text{ dB} = -11 \text{ dBFS}$
- The spur level (in the absence of any differential cancellation) will be $-6 \text{ dBFS} - 101 \text{ dB} = -107 \text{ dBFS}$
- Thus, the SFDR will be 96 dB
Need only 4 dB of differential cancellation to reach SFDR = 100 dB
- Calculating the impact of element dynamics on SNR is done similarly

33

Conclusions

- 1 3 dB is a factor of 2 (in BW, DR, or P).
- 2 An active-RC resonator can achieve high Q despite several circuit non-idealities.
- 3 Current-mode DACs can have near-perfect spectral performance up to several tens of MHz.

34



35