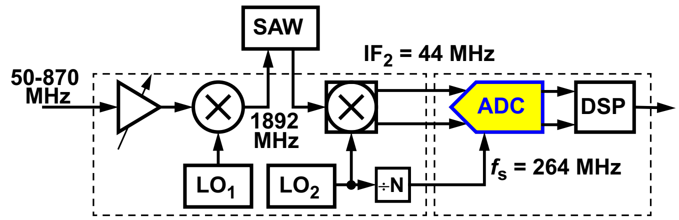
A Quadrature Bandpass ΔΣ ADC for a Multi-Standard TV Tuner

R. Schreier

High-Speed Converters Group
Analog Devices, Wilmington, MA

University of Toronto
Cider Seminar
Oct. 19 2006

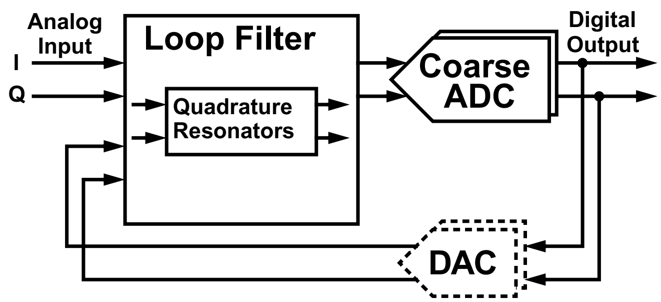
TV Tuner System



- Dual-conversion super-heterodyne receiver with an ADC at second IF
- ADC input is current-mode I&Q at 44 MHz
  BW = 8.5 MHz

A Quadrature ΔΣ ADC Is:

[Jantzi 1997]



- A ΔΣ ADC with quadrature everything
  NTF and STF are complex

Worry List

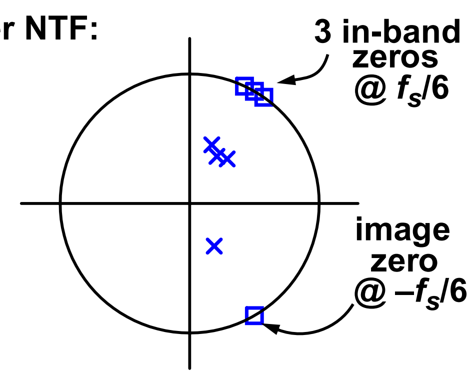
1 DAC linearity and noise at high f_s
⇒ Current-mode DAC, mismatch-shaping

2 Resonator Accuracy: f_0 and Q
⇒ Coming soon!

3 Path Matching
⇒ Large devices, symmetric/merged layout

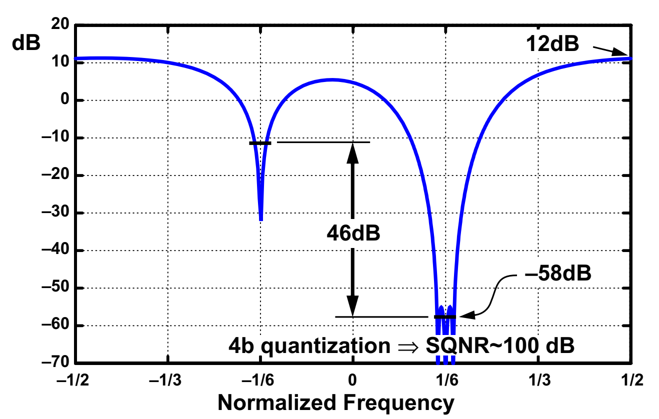
Ideal NTF– Poles and Zeros

4^{th}-order NTF:

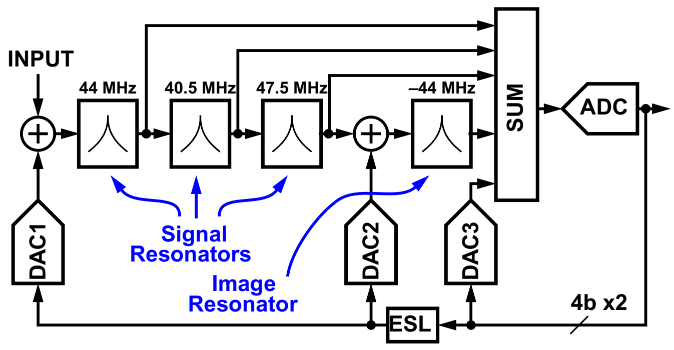


$OSR = f_s/f_B = 31$

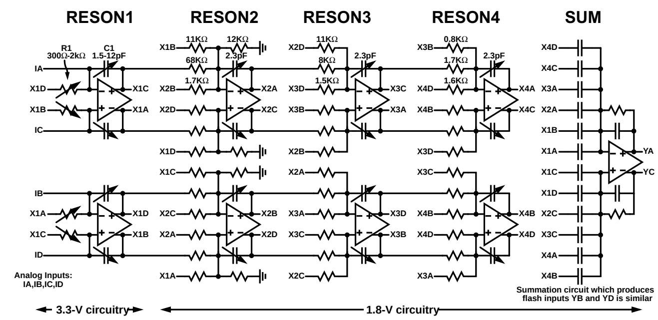
NTF Magnitude



ADC Architecture

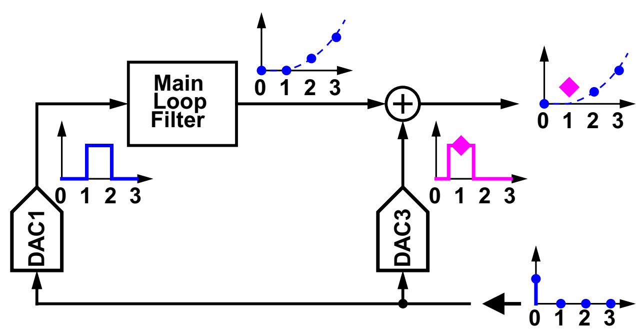


Loop Filter Schematic

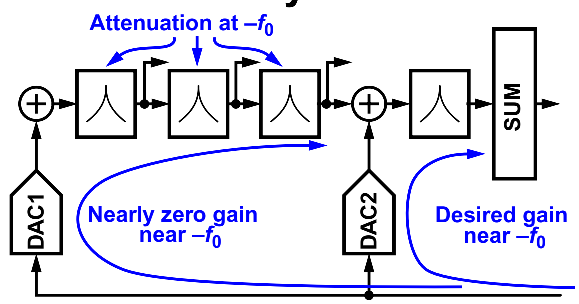


Why DAC3?

- DAC3 allows any LF/NTF to be realized
  - Even though DAC1 has 1 clock cycle of delay
  - DAC3 supplies the missing point

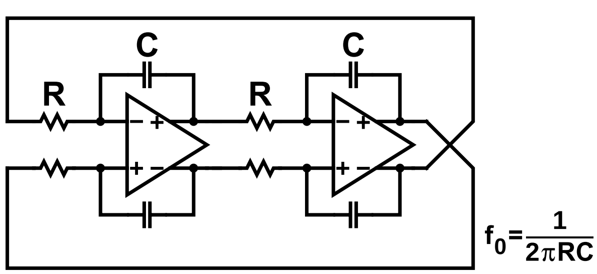


Why DAC2?



- DAC2 provides a low-attenuation feedback path for signals in the vicinity of $-f_0$
  - Thereby resolving a near singularity in the coefficient calculation procedure

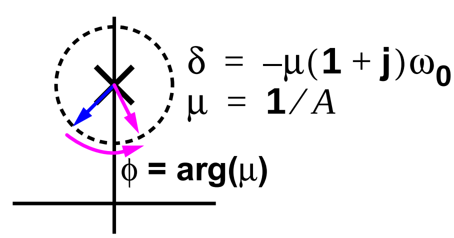
Resonator Structure



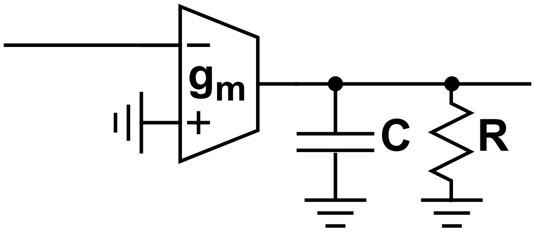
- Tuned by adding positive feedback to make an oscillator and adjusting C until the desired resonance is achieved
  - Amplifier drives both R and C ⇒ trouble?

Amplifier Gain and Phase

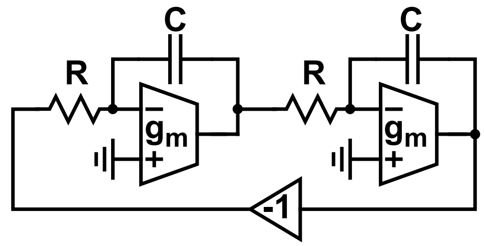
- Finite gain degrades Q
- Phase lag enhances Q
- Analysis shows ϕ = 45º yields high Q, regardless of amplifier gain



An Amplifier with ϕ = 45º @ f_0:



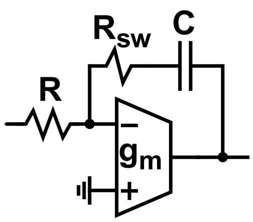
Resulting High-Q Resonator



- Amplifier load yields ϕ = 45º @ f_0
- Finite g_m shifts the pole frequency, but does not degrade Q!

Finite g_m Bandwidth & Non-Zero Switch Resistance

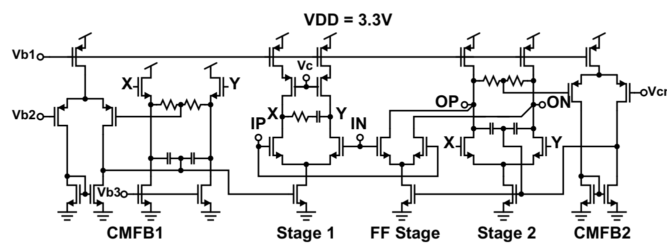
- Switch resistance degrades Q
- Finite gm bandwidth enhances Q



$$g_m = \frac{g_{m0}}{1 + s/\omega_p}$$

- Cancellation occurs if $R_{sw} = \frac{2\omega_0}{g_{m0}\omega_p}$

1st Resonator's Amplifier

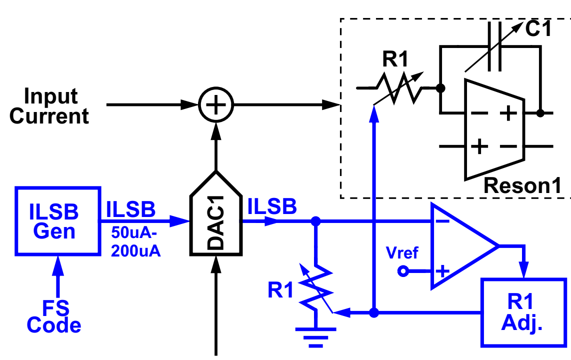


- 2-stage amplifier with feedforward stage and all-NMOS signal path

Gain-Scaling

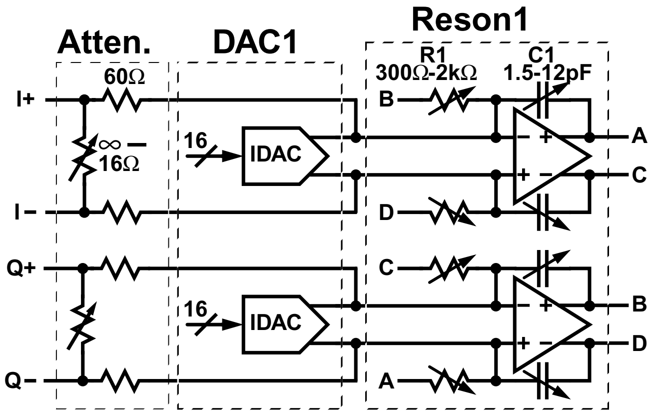
- 12-dB gain range implemented by scaling DAC1's LSB over a 4:1 range
- At the minimum LSB setting, DAC1's noise is 6 dB lower than at the maximum LSB setting
- Changes in DAC gain are counteracted by inverse change in Reson1 gain
  - Keeps gain of DAC1-Reson1 independent of LSB setting
- The gain-scaling burden is on the front end
  - No other circuits need to be adjusted

Gain-Scaling Arrangement



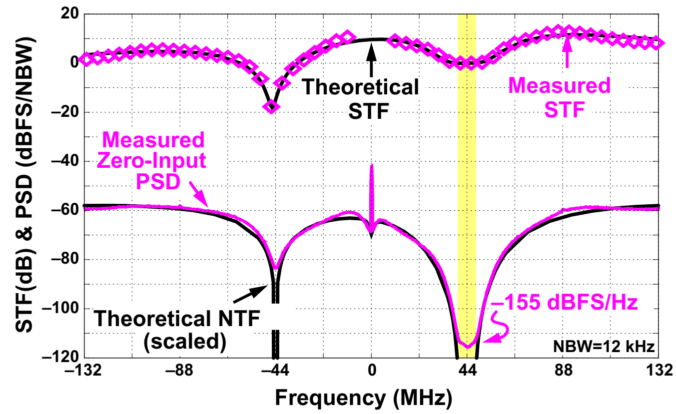
- Gain of DAC1+Reson1 kept constant

ADC Front-End



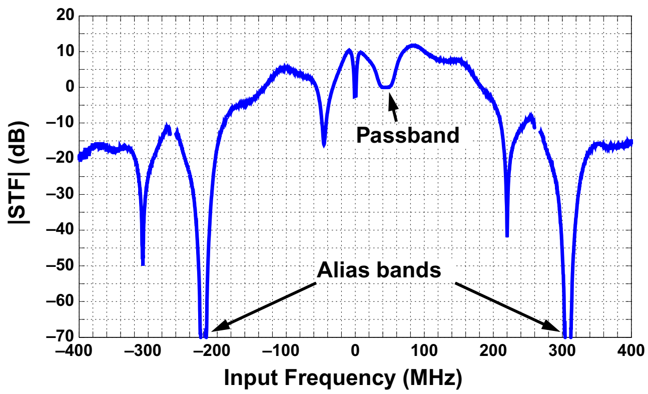
19

Results: STF & NTF



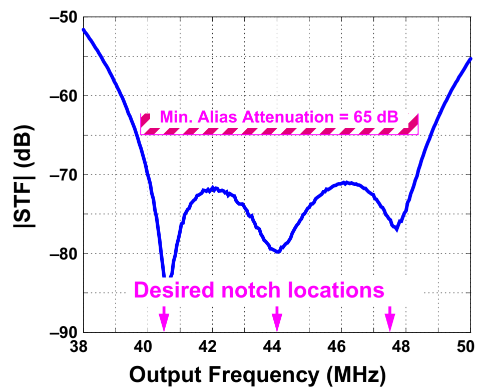
20

Wideband STF



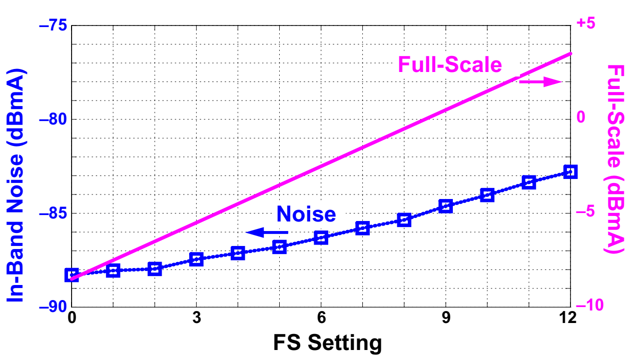
21

STF in +1 Alias Band



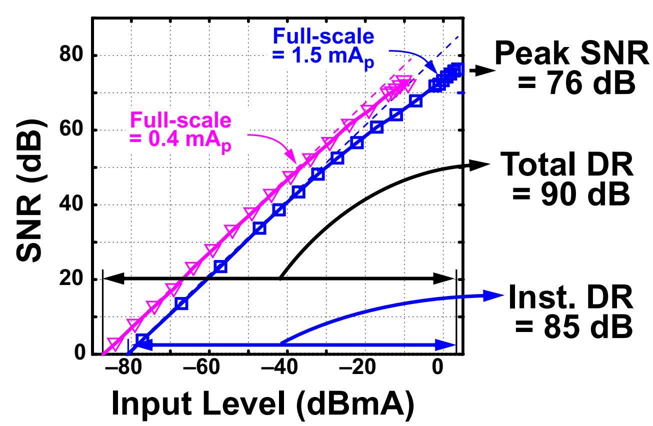
22

Noise vs. Full-Scale Setting



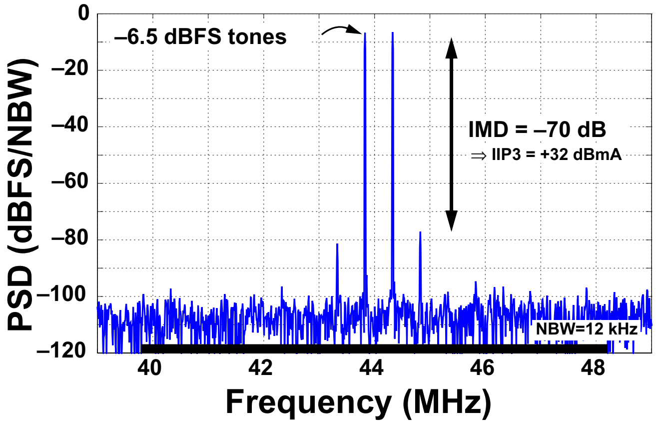
23

SNR vs. Input Level



24

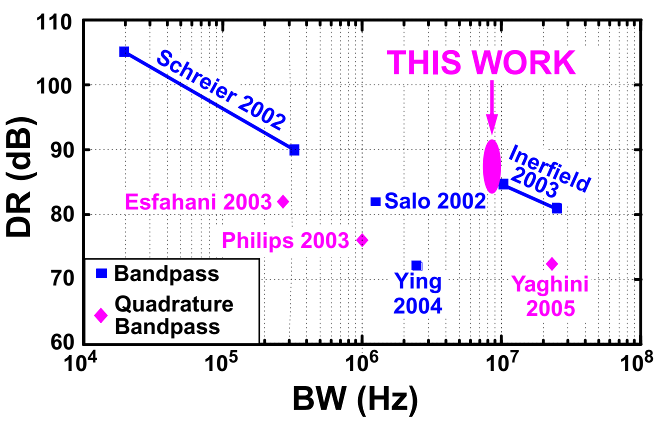
Two-Tone Spectrum



Performance Summary

Bandwidth	8.5	MHz
Center Frequency	44	MHz
Clock Frequency	264	MHz
Inst. Dynamic Range	85	dB
Full-Scale Range	12	dB
Total Dynamic Range	90	dB
Area in 0.18um CMOS	2.5	mm^2
Power Consumption	375	mW

Performance Comparison



Conclusions

- A feedforward implementation of a Quadrature Bandpass ΔΣ ADC needs an extra DAC
  An input attenuator is a good idea too.
- High Q resonance can be achieved by
  1. Using a simple g_m instead of a true op amp
  2. Balancing finite g_m bandwidth and non-zero switch resistance

  Measured Q > 40
- Gain-scaling extends DR