Lab 1: Common-source Amplifiers

Introduction

The common-source amplifier is one of the basic amplifiers in CMOS analog circuits. Because of its very high input impedance, relatively high gain, low noise, speed, and simplicity, common-source amplifiers find different applications from sensor signal amplification to RF low-noise amplification. Good understanding of this amplifier is essential not only for good design of one but also for analysis of other advanced circuits such as differential amplifiers which you see later in this course.

In this lab, you are to design, simulate, and implement NMOS- and PMOS-based common-source amplifiers with a resistive load shown in Figure 1. They will be designed for different requirements such as gain, swing and supply voltage.

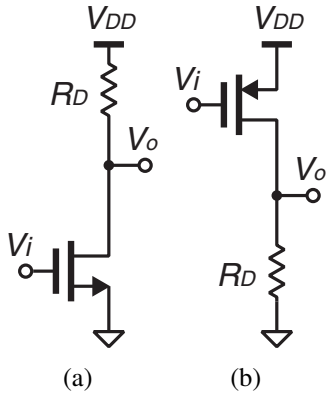

Figure 1: (a) NMOS and (b) PMOS common-source amplifiers.

Preparation

Go through the following preparation steps.

1. Take a look at the two different design approaches given below for the NMOS common-source amplifier shown in Figure 1a.

   Design for the maximum output swing with an arbitrary I_D: For a given I_D and known device parameters V_{ov} can be approximated by using the transistor large signal model active equation ($V_{ov} = \sqrt{2I_D/\mu C_{ox}W/L}$). The maximum swing possible is $V_{DD} - V_{ov}$. In order to use the maximum swing, the output node , V_O, should be placed in the middle of the swing

range: $V_O = (V_{DD} + V_{ov})/2$. This also requires $I_D R_D = (V_{DD} - V_{ov})/2$ and thus $R_D = (V_{DD} - V_{ov})/2I_D$. Since $g_m = 2I_D/V_{ov}$, $A_v = -g_m R_D = (-2I_D/V_{ov}) \cdot (V_{DD} - V_{ov})/2I_D = -(V_{DD} - Vov)/V_{ov}$ assuming $R_D << r_o$.

Design procedure for the maximum gain with an arbitrary I_D and output swing: For a given I_D and known device parameters V_{ov} can be approximated by using the transistor large signal model active equation ($V_{ov} = \sqrt{2I_D/\mu C_{ox} W/L}$). Since $g_m = 2I_D/V_{ov}$ and $R_D = (V_{DD} - V_O)/I_D$, small signal gain can be written as $A_v = -g_m R_D = (-2I_D/V_{ov}) \cdot (V_{DD} - V_O)/I_D = -2(V_{DD} - V_O)/V_{ov}$ assuming $R_D << r_o$. For the maximum gain possible, V_O should be minimum, leading to $V_O = V_{ov} + V_{swing}/2$.

2. Design common-source amplifiers for the criteria shown in Table 1. Perform hand analysis to fill in the blanks in Table 1 using the device parameters shown in Table 2. **Be careful** the design procedures given above are for NMOS common-source amplifier. You may need some modifications in the equations for the PMOS common-source amplifier.

3. Perform a DC operating point simulation for the amplifiers designed above. Note that the transistor models used in simulation are far more complicated and accurate than the simple square law used for hand analysis. Therefore, some deviation from the hand analysis comes with no surprises.

4. Perform a DC sweep to plot V_o, I_D, and $dV_o/dV_i (= A_v)$ versus V_i in the same plot window. V_i should be swept from 0 V to V_{DD}.

5. Label and comment on the plots to clearly show the the small-signal gain (A_v), V_i, and output swing for the I_D specified in Table 1.

6. Perform a transient simulation to show V_o versus time. Use a sinusoidal voltage source at 1 kHz with 10-mV_{pp} amplitude as the input source. Make sure that the input and thus the output are biased at the voltages found in the previous step. Verify the small-signal gain found in the previous step.

7. Organize the results for presentation to your TA in a report. You should also bring your LTSpice simulation files with a memory stick for presentation to your TA. Please name your files in the following format: *lab1_..._surname1_surname2*. Computers are provided in the laboratory room.

Lab - Part I: LTSpice Simulation Challenge

The first part of this lab will be an LTSpice simulation challenge that will be announced at the beginning of the lab session by your TA. You will work in groups of two and have 50 minutes to finish. Completing the preparation part of the lab and general knowledge of the course should be enough to finalize this part.

Table 1: Hand analysis table

V_{DD} (V)	Type	Gain	Swing (V_{pp})	V_{ov} (V)	I_D (A)	g_m (A/V)	V_o (V)	R_D (Ω)	A_v (V/V)
5.0	NMOS	-	max		1 m				
5.0	PMOS	-	max		0.5 m				
1.2	NMOS	max	0.2		0.5 m				

Table 2: NMOS and PMOS device parameters

Type	Device	V_T (V)	$\mu_{n/p}C_{ox}W/L$ (mA/V^2)
NMOS	ALD1101	0.71	4.49
PMOS	ALD1102	-0.65	-2.10

Lab - Part II: Common-Souce Amplifier Implementation

Do the following for the first two common-source amplifiers designed by hand analysis. A minimum parts list for this lab is shown in Table 3. Resistors will be supplied in the laboratory.

1. Measuring V_o versus V_i

Repeat the following for the first two common-source amplifiers designed in the preparation.

1. Implement the common-source amplifier on the breadboard. Connect a 50-Ω resistor across the input and the ground as shown in Figure 2 . This resistor is important for the voltage reading of the signal generator to be correct. Most of the signal generators have a 50-Ω output impedance and the voltage reading is correct only if its load is 50 Ω. **You will need this 50-Ω termination many times in future labs when you use a signal generator although it won't be explicitly shown in lab manuals.**

2. Configure the signal generator for a triangular wave with 0 V to V_{DD} swing at 100 Hz. Make sure to do this step without connecting the transistor to the signal generator but with the 50-Ω resistor connected, as an excessive gate voltage can permanently damage the transistor.

3. Connect the input signal to the transistor and measure the input (V_i) and output (V_o) simultaneously using both of the input channels of the oscilloscope. Use the input signal as the

Table 3: Minimum parts list

Part	Description	Quantity
ALD1101	NMOS transistor	1
ALD1102	PMOS transistor	1
-	10-kΩ multi-turn potentiometer	1

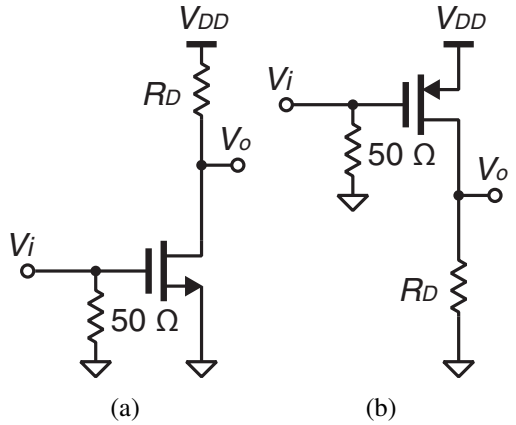

Figure 2: (a) NMOS and (b) PMOS common-source amplifiers with a 50-Ω input impedance.

trigger source. Adjust the horizontal scale to display roughly two periods of the triangular wave and adjust the vertical scale of each input to maximize the displayed signal swing without clipping. Make sure that V_i is swinging 0 V to V_{DD}.

4. Enable the XY plot mode of the oscilloscope to plot V_o versus V_i. Determine and record the input and output bias voltage that meets the I_D requirement in Table 1, and calculate the small-signal gain around that point. Sketch a V_o versus V_i curve and label important points. How does this compare with the simulation and hand analysis?

5. Organize the results for presentation to your TA.

2. Sinusoid testing

Repeat the following for the first two common-source amplifiers designed in the preparation.

1. Disconnect the signal source from the circuit, and configure the signal source for 1-kHz 10-mV_{pp} sinusoid.

2. Place the input bias circuit on the breadboard as shown in Figure 3, and tune the potentiometer for the input bias voltage found in the previous step. **This input bias circuit is used many times in future labs** so make sure you feel comfortable with it.

3. Connect the signal source to the breadboard and show both the input and output on the oscilloscope. How does the gain compare with hand analysis and simulation?

4. Organize the results for presentation to your TA.

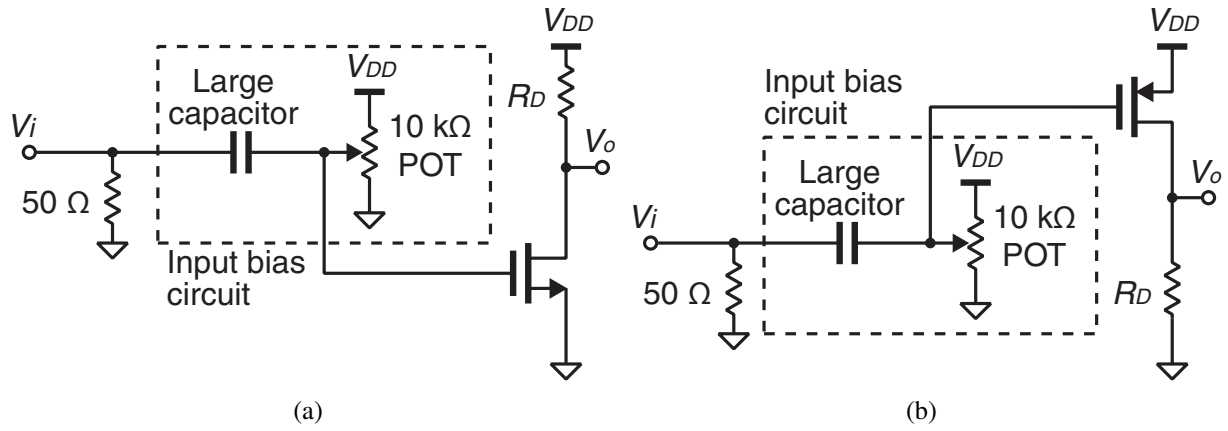

Figure 3: (a) NMOS and (b) PMOS common-source amplifiers with an input bias circuit.