A 16kb 1T1C FeRAM Testchip Using Current-Based Reference Scheme

Joseph Wai Kit Siu, Yadollah Eslami, Ali Sheikholeslami, P. Glenn Gulak,

Toru Endo[1], and Shoichiro Kawashima[1]

Department of Electrical and Computer Engineering,

University of Toronto, Toronto, Canada

1. Fujitsu Laboratories Limited, Atsugi, Japan

Abstract

A 16kb 1T1C FeRAM testchip is designed and fabricated in a 0.35μm FeRAM process. The testchip uses a reference generation scheme that balances fatigue evenly between memory cells and reference cells, hence providing the 1T1C cell with 2T2C robustness to fatigue. The testchip achieves an access time of 62ns at 3V.

Introduction

Reference generation is an essential component of 1T1C Ferroelectric Random Access Memory (FeRAM) design. The conventional approach of using a fixed reference voltage (V_{ref}) for the entire memory array [1] does not track the ferroelectric process variation across the chip, nor the ferroelectric-material degradation with time. On the other hand, generating a V_{ref} separately for each column of the memory array at the time of data retrieval [2][3] reduces the effect of process variation on the sensing signal but fatigues reference cells at a rate different from that of memory cells [3]. This paper presents measurement results from a 256x64-bit 1T1C FeRAM testchip that features: 1) a reference scheme that balances the fatigue effect evenly between the memory cells and the reference cells by generating a reference current (I_{ref}) and sharing it with a row (instead of a column) of memory cells, and 2) a current-steering sense amplifier implementing this scheme. The testchip has been designed and fabricated in a 0.35μm CMOS process with added planar ferroelectric capacitors.

Reference Generation

Fig. 1 compares two reference schemes: one using a reference cell per column and the other using a reference cell per row of the memory array. Assuming a total of n rows being accessed sequentially, the reference row at the bottom of the array will be accessed, and hence fatigued, n times more than a typical memory row. On the other hand, a reference cell per row of the memory cell is accessed at exactly the same rate as the memory cells, and hence is fatigued at exactly the same rate. This is expected to increase the 1T1C FeRAM lifetime by the same factor n.

Fig. 2 shows an implementation of a reference column pair, RBL and $\overline{RBL}$, in association with a set of eight memory columns. RBL and $\overline{RBL}$ are each connected to a memory cell, one of which always stores a "1" and the other a "0". The voltage developed on a typical BL, V_1 for a stored "1", and V_0 for a stored "0", will be identical to those of RBL and $\overline{RBL}$, independent of the access rate of memory cells, since they all share the same WL and PL. The voltage developed on BL (V_x), RBL (V_1), and $\overline{RBL}$ (V_0), are converted by a set of

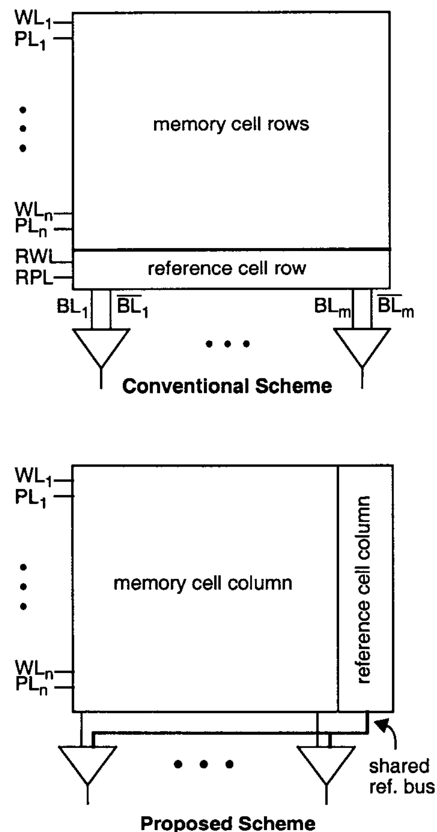

Fig. 1: Reference Generation in 1T1C FeRAM

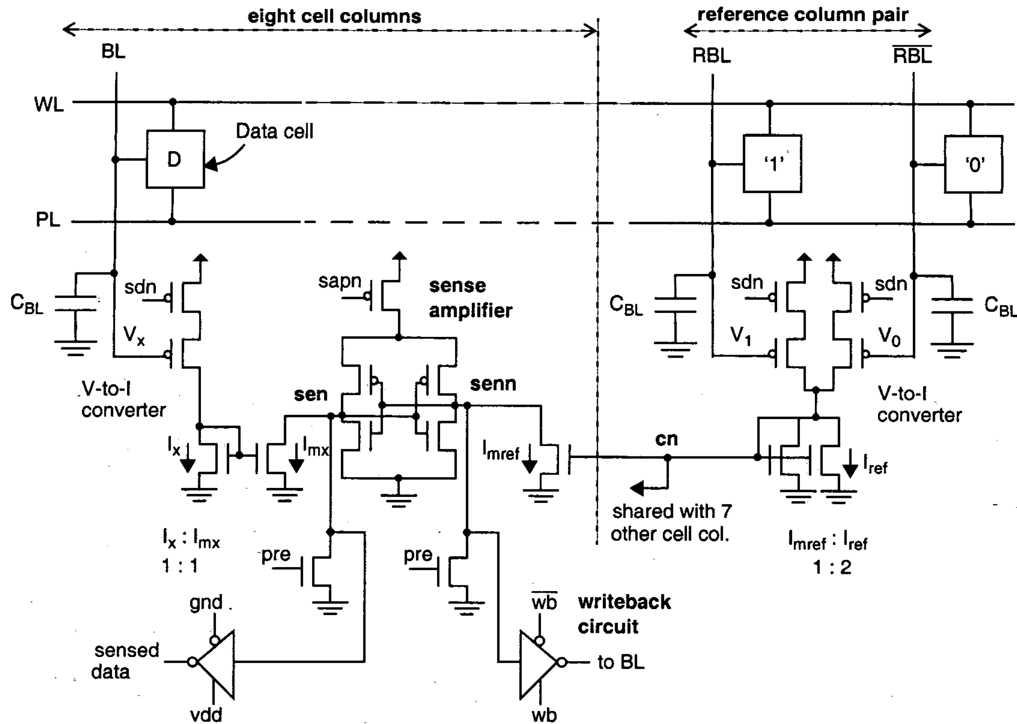

Fig. 2: Sensing scheme for 1T1C FeRAM

identical PMOS transistors to I_x, I_1, and I_0 respectively. I_1 and I_0 are summed in the reference column, then mirrored at half amplitude to the sense amplifiers in eight neighboring columns to generate I_{mref}, ideally halfway between I_1 and I_0. Similarly, I_x is mirrored in each bitline to generate I_{mx}. By activating sdn, I_{mx} and I_{mref} begin sinking charge from opposite drain nodes (sen and senn) of a cross-coupled PMOS pair, and compete to pull their respective nodes down. Eventually, one node is pulled to ground and the other one is pulled to V_{DD}. Results of HSPICE simulation, shown in Fig. 3, illustrate critical currents and node voltages in the sense amplifier as functions of time. In reading data '1', I_{mx} is smaller than I_{mref}. Therefore, node 'sen' in Fig. 2 is charged up faster than its complement 'senn' and regenerates to V_{DD}. In reading data '0', I_{mx} is larger than I_{mref}, pulling node 'sen' to ground. The sense operation is completed in less than 6ns from the time of activating sdn.

Testchip Architecture

The proposed sensing scheme has been implemented in a 256x64-bit testchip. In order to test the sensing scheme and the sense amplifier over a range of bitline capacitance (C_{BL}) and ferroelectric cell capacitance (C_{FE}), we have implemented four distinct bitline lengths and four distinct sizes of cell capacitor. The shortest bitline corresponds to 64

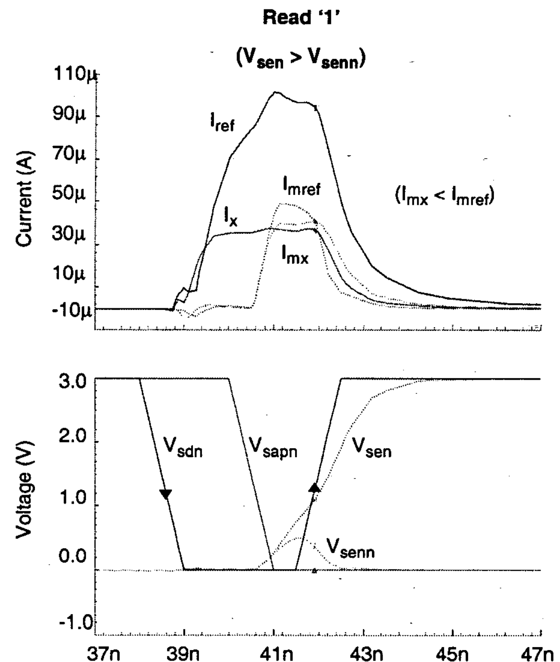

Fig. 3: Simulation results of the sense amplifier

rows of 1T1C cells while the longest bitline corresponds to 256 rows of 1T1C cells. As a result, C_{BL} can take one of four values: from one to 4 times the minimum C_{BL}. Similarly, C_{FE} can take one of four values: from one (1X) to 4 times (4X) the minimum cell capacitance (1X: $1\mu m^2$ area). Using an extra row-address bit, up to three rows can be accessed in a set of four consecutive rows, hence C_{FE} up to 8X can be tested. Overall, a total of 32 different combinations of C_{BL} and C_{FE} are available on the testchip for experimentation purposes. The circuit shown in Fig. 4 is used to either monitor the bitline voltage or to overwrite the inputs to the sense amplifier for sensitivity measurement. The circuit demonstrates a measured linear V_{in}—V_{out} relationship over an input voltage range of 0V to 2.1V when a 3V power supply is used.

Simulation and Measurement Results

Fig. 5 shows both simulated and measured values of V_{RBL}, $V_{\overline{RBL}}$, and ΔV_{BL} over the entire range of C_{BL}/C_{FE} implemented in the testchip. Measured V_{RBL} has a range of 0.6V to 1.9V and measured $V_{\overline{RBL}}$ has a range of 0.2V to 1.8V. Fig. 6 plots the voltage-measurement results for V_{RBL} and $V_{\overline{RBL}}$ along with direct measurement results of the sense amplifier using the overwrite circuitry. All data points from bitline voltage measurement fall outside ± 0.4V region of the ideal reference line (V_{RBL} = $V_{\overline{RBL}}$ or ΔV_{BL}=0), leaving enough margin to reliably detect the bit value. To ensure that this margin is large enough to compensate for sense-amplifier non-idealities (including input offset, noise, and gain error due to mismatches between the two current mirrors), the meta-stability region of the amplifier was also measured. As shown in Fig. 6, the meta-stability region of the amplifier falls well within the ± 0.4V margin band.

Extensive measurement results confirm that the sensing scheme functions successfully. The sense amplifier is operational over the entire range of V_{RBL} and $V_{\overline{RBL}}$. Measurement results show an access time of 62.5ns and a cycle time of 130ns (both multiples of 6.25ns, which is the minimum time step of the tester used). Simulation results suggest an access time of 50ns and a cycle time of 100ns, all at V_{DD} = 3V.

Speed-Area Trade-off

Referring to Fig. 2, the sensing speed of this design is limited by the capacitive load at the common node "cn" of the reference current mirror, which is proportional to the number of columns (M) mirroring I_{ref}. The testchip uses M = 8. A larger M implies higher capacitance at node "cn" and, hence, a longer rise time for the voltage at "cn". A smaller M implies a shorter rise time and, hence, an increased speed at the expense of additional silicon area to include more reference columns in the array.

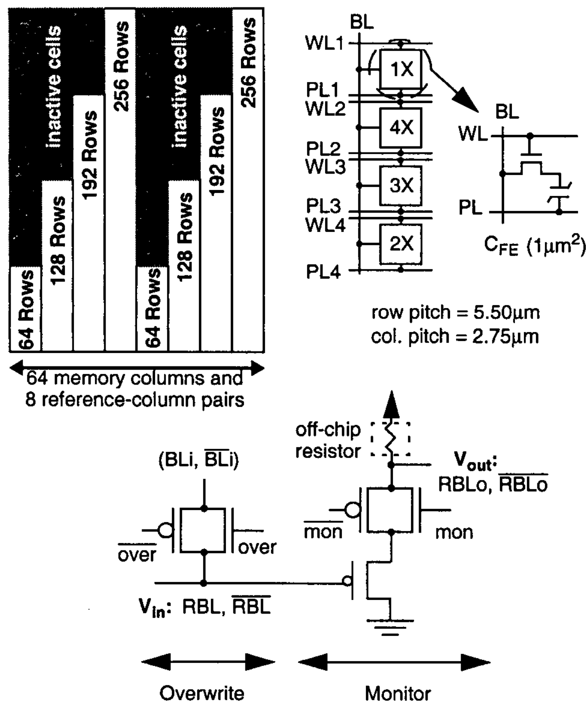

Fig. 4: Testchip architecture: memory core, monitor, and overwrite circuit

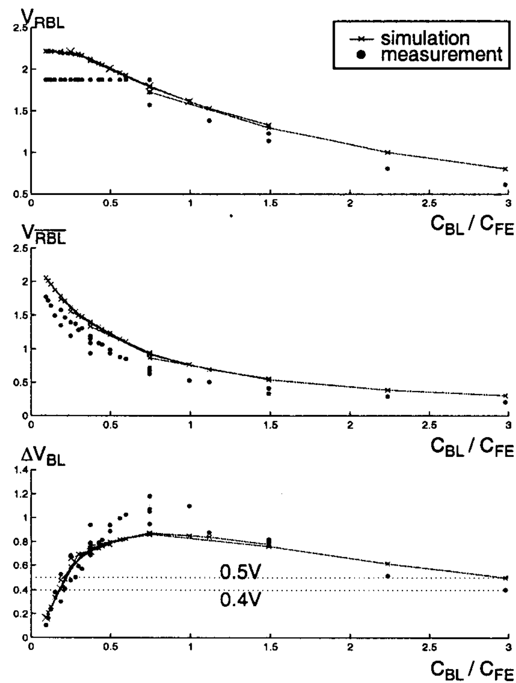

Fig. 5: Simulation and measurement results: bitline voltage as a function of C_{BL}/C_{FE}

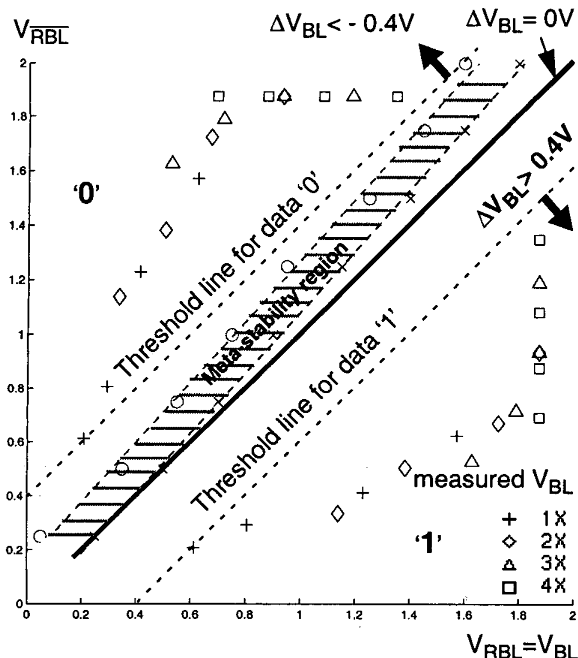

Fig. 6: Measured characteristics of the sense amplifier

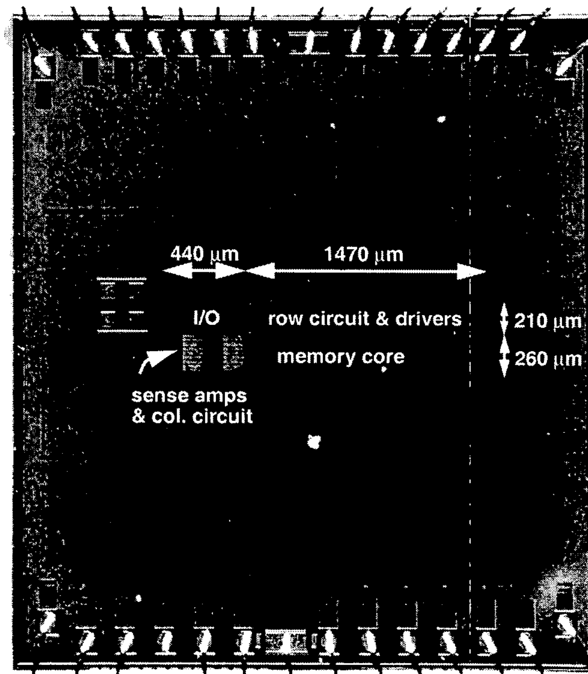

Fig. 7: Chip Micrograph

Referring to Fig. 3, the control signal V_{sapn} must be activated after "cn" has reached its peak value; otherwise a read error may occur. We have performed various simulations on this circuit to verify circuit functionality and to determine the critical M for typical timing of V_{sdn} and V_{sapn}. Simulation results for the cases of M = 16, M = 32, and M = 64 confirm correct read operation despite the slower rise time for I_{ref} ; I_{mref} and I_{mx} show little change compared to the case of M = 8. When M is increased to 128, however, both I_{ref} and I_{mref} are slowed down significantly, to a point where the stored data is erroneously sensed. This is due to I_{ref} not reaching its peak value before deactivating sdn. In order to remedy this situation, both activating sapn and deactivating sdn must be further delayed until I_{ref} has reached its peak value. Simulation results confirm that by delaying sapn and sdn by 1.5ns, the sense amplifier correctly detects the bit value. This delay is the trade-off for reducing area overhead from 4% to 2%.

Conclusions

Table 1 summarizes the testchip features shown in Fig. 7. The testchip measurement results confirm the functionality of the current-based reference scheme and the current-steering sense amplifier. The testchip achieves an access time of 62.5ns at 3V power supply.

Table 1: Chip Characteristics

Technology	0.35mm, 3-metal, PZT-film
Organization	256x64-bit
Chip Size	0.47mm x 1.91mm = 0.90mm^2
Supply Voltage	3V
Access Time	62.5ns (measured at 3V, 25 °C)
Cycle Time	130ns (measured at 3V, 25 °C)

Acknowledgements

The authors thank Dr. Yoshihiro Arimoto of Fujitsu Labs, Atsugi, Japan, for his support and guidance. Further, the authors acknowledge generous funding of Fujitsu Labs, Atsugi, Japan, and NSERC of Canada.

References

[1] B. Jeon, M. Choi, Y. Song, S. Oh, Y. Chung, K. Suh, and K. Kim, "A 0.4 µm 3.3V 1T1C 4Mb nonvolatile ferroelectric RAM with fixed bit-line reference voltage scheme and data protection circuit," ISSCC Dig. Tech. Papers, pp. 272-273, 2000.

[2] T. Sumi, N. Moriwaki, G. Nakane, T. Nakakuma, Y. Judai, Y. Uemoto, Y. Nagano, S. Hayashi, M. Azuma, E. Fujii, S. Katsu, T. Otsuki, L. McMillan, C. P. de Araujo, and G. Kano,, "A 256kb nonvolatile ferroelectric memory at 3V and 100ns," ISSCC Dig. Tech. Papers, pp. 268-269, 1994.

[3] A. Sheikholeslami and P. G. Gulak, "A survey of circuit innovations in ferroelectric random-access memories," Proceedings of The IEEE, Vol. 88, No. 5, pp. 665-689, May 2000.