7.4   A Blind Baud-Rate ADC-Based CDR

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ADC-based receivers process the received data in the digital domain, eliminating the need for much of the analog front end. In addition, a feed-forward blind architecture [1,2] eliminates the feedback loop between digital and analog domains so that the ADC and digital CDR can be designed and simulated independently. Previous works [1,2] sampled the incoming data at 2 samples per UI and at 1.45 samples per UI to achieve 5Gb/s and 6.875Gb/s, respectively. To further increase the data rate to 10Gb/s, we sample at baud rate (1 sample per UI). Existing baud-rate architectures [3] rely on a *phase-tracking* clock to sample at the middle of the data eye. This paper presents a *blind* baud-rate CDR, fabricated in 65nm CMOS. At 10Gb/s, the CDR demonstrates a high-frequency jitter tolerance of 0.19UI with ±300ppm of frequency offset. Also, the CDR demonstrates successful operation with 1000ppm offset, which amounts to sub-baud-rate sampling.

Figure 7.4.1 illustrates the main challenge in the blind baud-rate sampling approach. Given an ideal channel, the data eye is open when sampled with a phase range spanning 1UI. However, with blind sampling, frequency offset between the data and receiver clock will cause the baud-rate sampling phase to shift continuously across a 1UI window. When the sampling occurs near the boundary, any high-frequency jitter may shift the sampling outside the 1UI phase range, resulting in the loss of data bits (i.e., zero jitter tolerance). To increase jitter tolerance, we introduce a controlled amount of ISI in the data by using a rectangular filter implemented as an integrate-and-dump (I&D) circuit [4] in the receiver front end. A 1UI rectangular filter, convolved with the ideal channel, spreads the pulse response to 2UI. If we have a perfect DFE to cancel all post-cursor ISI, then the eye would be open for a range of 1.5UI. If the blind samples shift beyond the 1UI window, there is still a remaining jitter margin of $0.5UI_{pp}$. A 2UI rectangular filter increases this margin to $1UI_{pp}$ and results in a symmetric eye opening with respect to the blind sampling window. For these reasons, we choose a 2UI I&D circuit in our design.

Figure 7.4.2 shows the receiver, including an analog front end and digital CDR. The front end consists of four interleaved I&D and ADC blocks, each operating at 2.5GS/s. The I&D circuit integrates over 1UI intervals and samples the result, which the ADC converts into 5b digital values that are demuxed into 16 parallel samples. The digital CDR adds adjacent 5b 1UI I&D samples to synthesize 6b 2UI I&D samples. Since our ADC resolution is limited to 5 bits, if we were to obtain 2UI I&D samples directly in the analog domain and feed them to the ADC, we would have lost the added resolution.

The digital CDR contains a feedback loop including a data interpolator, a speculative 2-tap DFE, a speculative Mueller-Muller phase detector (MMPD), and a conventional 2nd-order loop filter. The data interpolator estimates the desired sample at the average interpolation phase (φ_{avg}) by linearly combining neighbouring blind samples. Given a negative frequency offset (i.e., data slower than baud rate), the interpolated sample is dropped each time the phase completes a 1UI rotation. A positive frequency offset would result in cases where no blind sample exists between two desired samples; the interpolator resolves these cases by interpolating twice between the two closest blind samples. The DFE compensates for post-cursor ISI from the channel and I&D filter. As shown in Fig. 7.4.1, recovering data from an ideal channel and 2UI I&D filter would require one DFE tap; a more attenuative channel may require more taps (we use two taps in this design). The DFE is implemented speculatively to reduce feedback loop latency. DFE adaptation is not included in this design. The MMPD is described later in Fig. 7.4.4.

Figure 7.4.3 shows the circuit details of the 1UI I&D front end. This circuit introduces controlled ISI into the ADC input and also operates as a frequency-scalable anti-aliasing filter [4]. The I&D block consists of a single source-degenerated transconductance stage that integrates the signal on the input capacitance of the ADCs. Four clock pulses synchronize I&D block operation across 3 phases: integrate, hold, and reset. Any skew between the clock phases would cause jit-

ter tolerance degradation in one of two ways. First, clock skew would appear effectively as high-frequency periodic jitter. Second, the interleaved I&D blocks would experience a gain mismatch because the integration is performed over the pulse width. For these reasons, a variable delay of up to 20ps is included in each of the four CML-to-CMOS converters in order to compensate for clock skew.

Figure 7.4.4 shows the details of the speculative MMPD [5,6]. The maximum vertical eye opening occurs when the main cursor, h_0, is at time T—this is our desired sampling phase. This sampling phase results in a post-cursor ISI equal to the main cursor and zero pre-cursor ISI, which allows us to fully benefit from the DFE and to minimize the need for an FFE. To identify this desired phase location, we estimate the MMPD function, $F = h_0-h_1$, at every sample and force it to zero through the feedback loop. Since our actual sampling phase is blind, we force the desired phase on the interpolating phase.

It is known [5] that h_0 and h_1 can be estimated by the expected values, $E[x_kA_k]$ and $E[x_kA_{k-1}]$, respectively, where x_k is the data sample (in our design, the interpolated I&D sample) and A_k is the recovered bit. To reduce loop latency, we estimate h_0 by the expected value of $x_{k-1}A_{k-1}$. The resulting MMPD output, $(x_{k-1}-x_k)A_{k-1}$, can be evaluated speculatively; the PD output is ready in the same cycle that A_{k-1} becomes available.

Figure 7.4.5 shows the measurement results of the combined I&D and ADC front end at DC (left) and at 10Gb/s through an eye diagram with a PRBS-7 input (right). The DC transfer characteristic shows the gain errors before and after skew correction. We are able to reduce the relative gain error by adjusting the phase delays between the four divided clocks, as described in Fig. 7.4.3. The right diagram shows the eye after the 1UI I&D and ADC blocks (the 2UI I&D is performed in the digital domain). Since four ADCs are interleaved in this design, we have superimposed four output eyes to construct the worst-case eye diagram. Despite the mismatch between the interleaved front-end blocks, the digital CDR is able to recover the data as we will see in Fig. 7.4.6. Since the 2UI I&D produces a null at the Nyquist frequency (5GHz), this design is not limited by the channel attenuation at Nyquist frequency. Instead, we are limited by the combined channel and I&D attenuation at half the Nyquist frequency (i.e., 2.5GHz), which is a less-restrictive constraint. In our measurements, the total attenuation at 2.5GHz is approximately 10dB.

Figure 7.4.6 shows the jitter tolerance curve for 10Gb/s PRBS-7 input for cases of zero and ±300ppm frequency offset with a worst-case high-frequency jitter tolerance of $0.19UI_{pp}$. In addition, we demonstrate successful operation when sampling below the baud rate by including a jitter tolerance curve for +1000ppm frequency offset. This offset is close to loop filter limit for this design.

Figure 7.4.7 shows the die micrograph. The I&D circuit, ADC (including demux), and digital CDR consume 1.7mW, 109mW, and 111.6mW, respectively.

References:
[1] H. Yamaguchi, et al., "A 5Gb/s transceiver with an ADC-based feedforward CDR and CMA adaptive equalizer in 65nm CMOS," *ISSCC Digest of Tech. Papers*, pp.168-169, Feb. 2010.
[2] O. Tyshchenko, et al., "A Fractional-Sampling-Rate ADC-Based CDR with Feedforward Architecture in 65nm CMOS," *ISSCC Digest of Tech. Papers*, pp. 166-167, Feb. 2010
[3] M. Harwood, et al., "A 12.5Gb/s SerDes in 65nm CMOS Using a Baud-Rate ADC with Digital Receiver Equalization and Clock Recovery," *ISSCC Digest of Tech. Papers*, pp. 436-437, 591, Feb. 2007.
[4] T. Tahmoureszadeh, et al., "A combined anti-aliasing filter and 2-tap FFE in 65-nm CMOS for 2x blind 2-10Gb/s ADC-based receivers," *Custom Integrated Circuits Conference (CICC)*, pp.1-4, Sept. 2010.
[5] K. Mueller and M. Muller, "Timing Recovery in Digital Synchronous Data Receivers," *IEEE Trans. on Communications*, pp. 516-531, May, 1976.
[6] A. Joy, et al., "Analog-DFE-based 16Gb/s SerDes in 40nm CMOS that operates across 34dB loss channels at Nyquist with baud rate CDR and 1.2Vpp voltage-mode driver," *ISSCC Digest of Tech. Papers*, pp.350-351, Feb. 2011.

Pulse Response with Blind Baud-Rate Samples

Vertical eye opening with ideal DFE (h_0-h_{-1})

Ideal channel (no I&D)

h_{-1}: Pre-cursor
h_0: Main cursor
h_1: 1st post-cursor

h_0
h_{-1}
h_1

$0UI_{pp}$ jitter tolerance at boundary (No margin)

Ideal channel + 1UI I&D

h_0
h_1
h_{-1}

$0.5UI_{pp}$ jitter tolerance at boundary

Ideal channel + 2UI I&D

h_0
h_1
h_{-1}

$1UI_{pp}$ jitter tolerance at boundary

0   T   2T   3T
Time

-1   0   1
Sampling Phase (UI)

1UI blind range

Faded arrows and dots show possible sampling phases due to frequency offset.
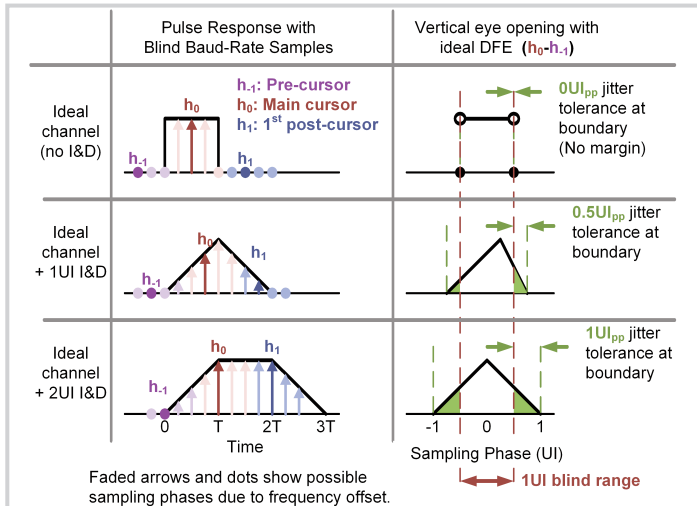
Figure 7.4.1: Comparison of theoretical worst-case jitter tolerance given ideal channel, 1UI I&D, and 2UI I&D. Blind baud-rate samples can shift across a 1UI range due to frequency offset.

Blind CK_{RX} (5GHz)
÷2   4   2.5GHz   ÷4   625MHz
10Gbps Data   Channel   1UI I&D   5-bit ADC   4:16   Digital CDR A_k

Digital CDR
Average interpolation phase (Φ_{avg})   5b
16x5b   x2   16x6b   +   16x6b   +   16x7b   Data Interpolator   17x13b   ÷8   17x10b   MM PD   16x11b   Digital Loop Filter
-31
z^{-1}
÷16   17x9b   Speculative 2-tap DFE   17x1b A_k
x_k

Convert to signed integer
Add 1UI I&D samples to form 2UI samples ≡ 2UI I&D
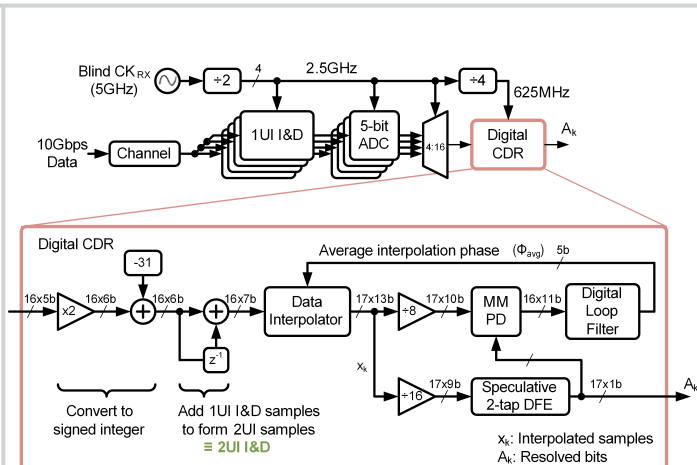x_k: Interpolated samples
A_k: Resolved bits

Figure 7.4.2: System block diagram of interleaved analog front end (1UI I&D and ADC) and digital CDR. Adjacent 1UI I&D samples are added in the digital CDR to form 2UI I&D samples.
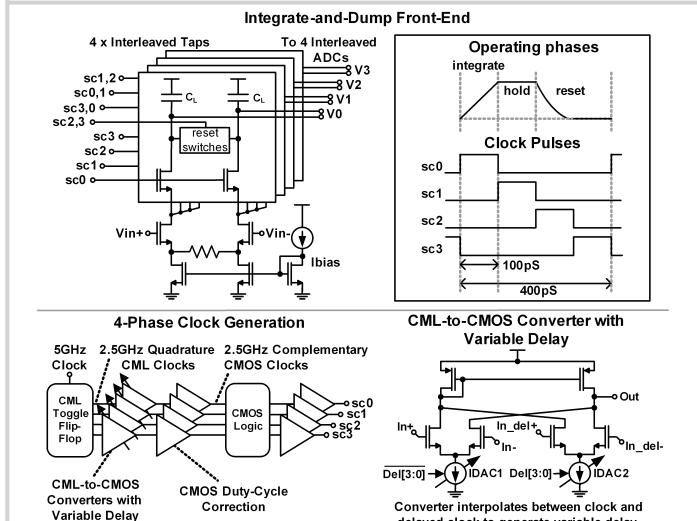
Integrate-and-Dump Front-End

4 x Interleaved Taps   To 4 Interleaved ADCs
sc1,2   sc0,1   sc3,0   sc2,3 C_L C_L V3   V2   V1   V0
reset switches
sc3   sc2   sc1   sc0
Vin+   Vin-   Ibias

Operating phases
integrate   hold   reset

Clock Pulses
sc0   sc1   sc2   sc3
100pS
400pS

4-Phase Clock Generation

5GHz Clock   2.5GHz Quadrature CML Clocks   2.5GHz Complementary CMOS Clocks
CML Toggle Flip-Flop   CMOS Logic   sc0   sc1   sc2   sc3
CML-to-CMOS Converters with Variable Delay   CMOS Duty-Cycle Correction

CML-to-CMOS Converter with Variable Delay
Out
In+   In_del+   In-   In_del-
Del[3:0]   IDAC1   Del[3:0]   IDAC2
Converter interpolates between clock and delayed clock to generate variable delay.

Figure 7.4.3: Implementation of integrate-and-dump (I&D) circuit and 4-phase clock generator. C_L is the input capacitance of the ADC.

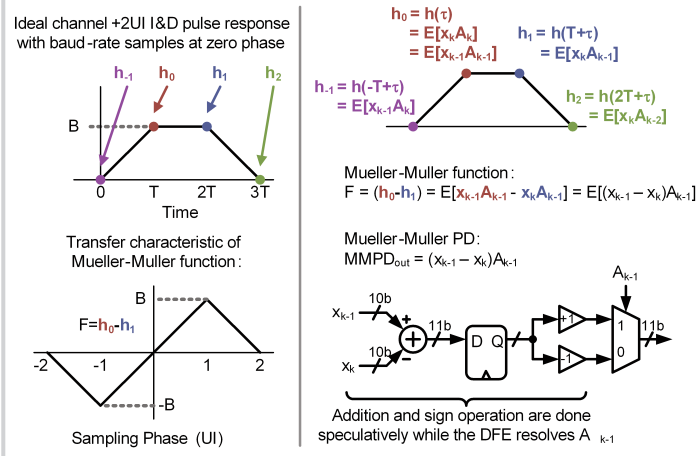Ideal channel +2UI I&D pulse response with baud-rate samples at zero phase

h_{-1} h_0 h_1 h_2
B
0   T   2T   3T
Time

$h_0 = h(\tau)$
$= E[x_k A_k]$
$= E[x_{k-1} A_{k-1}]$

$h_1 = h(T+\tau)$
$= E[x_k A_{k-1}]$

$h_{-1} = h(-T+\tau)$
$= E[x_{k-1} A_k]$

$h_2 = h(2T+\tau)$
$= E[x_k A_{k-2}]$

Mueller-Muller function:
$F = (h_0 - h_1) = E[x_{k-1} A_{k-1} - x_k A_{k-1}] = E[(x_{k-1} - x_k) A_{k-1}]$

Transfer characteristic of Mueller-Muller function:
B
$F = h_0 - h_1$
-2   -1   1   2
Sampling Phase (UI)
-B

Mueller-Muller PD:
$MMPD_{out} = (x_{k-1} - x_k) A_{k-1}$

A_{k-1}
x_{k-1} 10b   +   11b   D Q   -1   1   0   11b
x_k 10b

Addition and sign operation are done speculatively while the DFE resolves A_{k-1}

Figure 7.4.4: Design and implementation of the speculative Mueller-Muller phase detector (MMPD).

Before Skew Correction
Average ADC Output Code
ADC 0   ADC 1   ADC 2   ADC 3
-400   -200   0   200   400

After Skew Correction
Average ADC Output Code
ADC 0   ADC 1   ADC 2   ADC 3
-400   -200   0   200   400
DC Input Voltage (mVpp Differential)

1UI I&D Digital Output
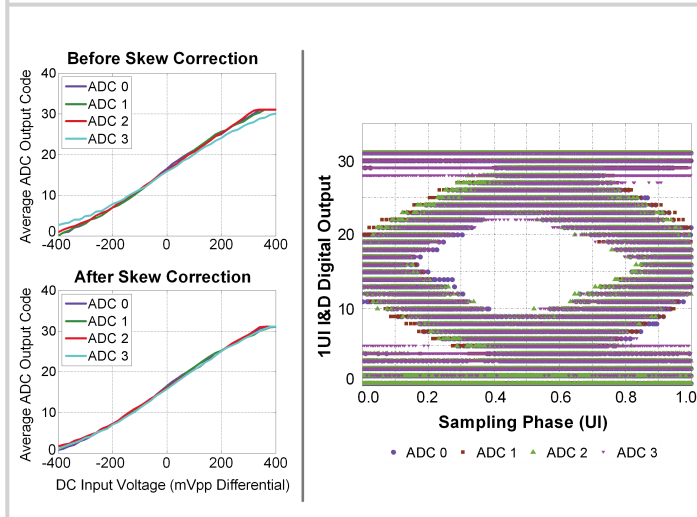0.0   0.2   0.4   0.6   0.8   1.0
Sampling Phase (UI)
ADC 0   ADC 1   ADC 2   ADC 3

Figure 7.4.5: Measured DC transfer curves of analog front end and eye diagram of 1UI I&D samples.

Jitter Tolerance (UIpp)
10.00   1.00   0.10   0.01
100kHz   1MHz   10MHz   100MHz
Jitter Frequency

-300ppm (TX slower than RX)
0ppm
300ppm
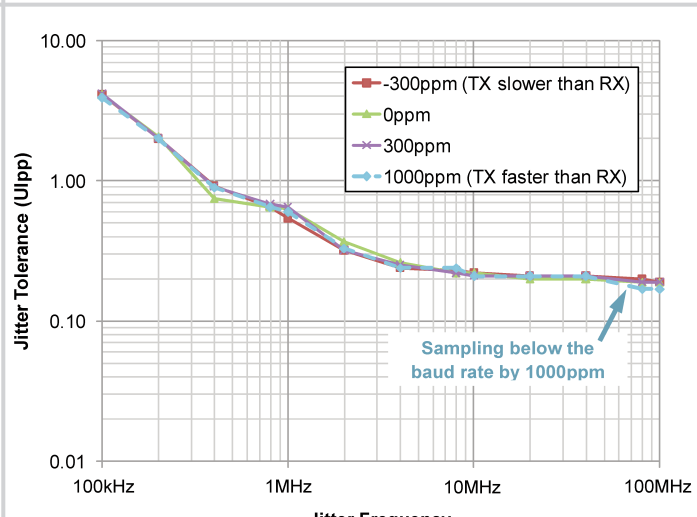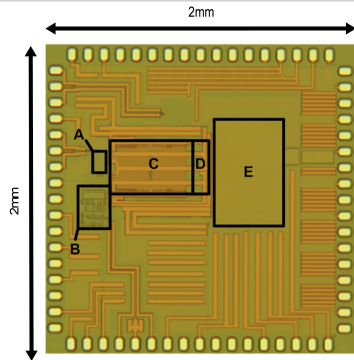1000ppm (TX faster than RX)

Sampling below the baud rate by 1000ppm

Figure 7.4.6: Measured jitter tolerance for 10Gb/s PRBS-7 with 10^{-12} BER, channel: 48" SMA cable.

7

Process	65nm CMOS
Data Rate	10Gb/s
Supply	1.2V

		Block description	Area (mm^2)
Analog front end	A	I&D	0.0119
	B	Clock generator	0.0378
	C	5-bit ADC	0.1960
Digital back end	D	4:16 Demux	0.0294
	E	Digital CDR	0.2860

Figure 7.4.7: Die micrograph.