7.4 A Blind Baud-Rate ADC-Based CDR

Clifford Ting1, Joshua Liang1, Ali Sheikholeslami1, Masaya Kibune2, Hirofaka Tamura3

1University of Toronto, Toronto, Canada, 2Fujitsu Laboratories, Kawasaki, Japan

ADC-based receivers process the received data in the digital domain, eliminating the need for much of the analog front end. In addition, a feed-forward blind architecture [1,2] eliminates the feedback loop between digital and analog domains so that the ADC and digital CDR can be designed and simulated independently. Previous works [1,2] sampled the incoming data at 2 samples per UI and at 1.45 samples per UI to achieve 5Gb/s and 6.875Gb/s, respectively. To further increase the data rate to 10Gb/s, we sample at baud rate (1 sample per UI). Existing baud-rate architectures [3] rely on a phase-tracking clock to sample at the middle of the data eye. This paper presents a blind baud-rate CDR, fabricated in 65nm CMOS. At 10Gb/s, the CDR demonstrates a high-frequency jitter tolerance of 0.19U of ±300ppm of frequency offset. Also, the CDR demonstrates successful operation with 1000ppm offset, which amounts to sub-baud-rate sampling.

Figure 7.4.1 illustrates the main challenge in the blind baud-rate sampling approach. Given an ideal channel, the data eye is open when sampled with a phase range spanning 1UI. However, with blind sampling, frequency offset between the data and receiver clock will cause the baud-rate sampling phase to shift continuously across a 1UI window. When the sampling occurs near the boundary, any high-frequency jitter may shift the sampling outside the 1UI phase range, resulting in the loss of data bits (i.e., zero jitter tolerance). To increase jitter tolerance, we introduce a controlled amount of ISI in the data by using a rectangular filter implemented as an integrate-and-dump (I&D) circuit [4] in the receiver front end. A 1UI rectangular filter, convolved with the ideal channel, spreads the pulse response to 2UI. If we have a perfect DFE to cancel all post-cursor ISI, then the eye would be open for a range of 1.5UI. If the blind samples shift beyond the 1UI window, there is still a remaining jiter margin of 0.5UIpp. A 2UI rectangular filter increases this margin to 1UIpp and results in a symmetric eye opening with respect to the blind sampling window. For these reasons, we choose a 2UI I&D circuit in our design.

The digital CDR contains a feedback loop including a data interpolator, a speculative 2-tap DFE, a speculative Mueller-Muller phase detector (MMPD), and a conventional 2nd-order loop filter. The data interpolator estimates the desired sample at the average interpolation phase ($\phi_{avg}$) by linearly combining neighbouring blind samples. Given a negative frequency offset (i.e., data slower than baud rate), the interpolated sample is dropped each time the phase completes a 1UI rotation. A positive frequency offset would result in cases where no blind sample exists between two desired samples; the interpolator resolves these cases by interpolating twice between the two closest blind samples. The DFE compensates for post-cursor ISI from the channel and I&D filter. As shown in Fig. 7.4.1, recovering data from an ideal channel and 2UI &D filter would require one DFE tap; a more attenuative channel may require more taps (we use two taps in this design). The DFE is implemented speculatively to reduce feedback loop latency. DFE adaptation is not included in this design. The MMPD is described later in Fig. 7.4.4.

Figure 7.4.3 shows the circuit details of the 1UI I&D front end. This circuit introduces controlled ISI into the ADC input and also operates as a frequency-scalable anti-aliasing filter [4]. The I&D block consists of a single source-degenerated transconductance stage that integrates the signal on the input capacitance of the ADCs. Four clock phases synchronize I&D block operation across 3 phases: integrate, hold, and reset. Any skew between the clock phases would cause jitter tolerance degradation in one of two ways. First, clock skew would appear effectively as high-frequency periodic jitter. Second, the interleaved I&D blocks would experience a gain mismatch because the integration is performed over the pulse width. For these reasons, a variable delay of up to 20ps is included in each of the four CML-to-CMOS converters in order to compensate for clock skew.

Figure 7.4.4 shows the details of the speculative MMPD [5,6]. The maximum vertical eye opening occurs when the main cursor, $h_0$, is at time $T$—this is our desired sampling phase. This sampling phase results in a post-cursor ISI equal to the main cursor and zero pre-cursor ISI, which allows us to fully benefit from the DFE and to minimize the need for an FFE. To identify this desired phase location, we estimate the MMPD function, $F = h_0 - h_1$, at every sample and force it to zero through the feedback loop. Since our actual sampling phase is blind, we force the desired phase on the interpolating phase.

It is known [5] that $h_0$ and $h_1$ can be estimated by the expected values, $E[x_k A_k]$ and $E[x_k A_{k+1}]$, respectively, where $x_k$ is the data sample (in our design, the interpolated I&D sample) and $A_k$ is the recovered bit. To reduce loop latency, we estimate $h_0$ by the expected value of $x_k A_k$. The resulting MMPD output, $(h_0 - h_1) = (x_k - x_{k+1}) A_k$, can be evaluated speculatively; the PD output is ready in the same cycle that $A_k$ becomes available.

Figure 7.4.5 shows the measurement results of the combined I&D and ADC front end at DC (left) and at 10Gb/s through an eye diagram with a PRBS-7 input (right). The DC transfer characteristic shows the gain errors before and after feed-forward correction. We are able to reduce the relative gain error by adjusting the phase delays between the four divided clocks, as described in Fig. 7.4.3. The right diagram shows the eye after the 1UI I&D and ADC blocks (the 2UI I&D is performed in the digital domain). Since four ADCs are interleaved in this design, we have superimposed four output eyes to construct the worst-case eye diagram. Despite the mismatch between the interleaved front-end blocks, the digital CDR is able to recover the data as we will see in Fig. 7.4.6. Since the 2UI I&D produces a null at the Nyquist frequency (5GHz), this design is not limited by the channel attenuation at Nyquist frequency. Instead, we are limited by the combined channel and I&D attenuation at half the Nyquist frequency (i.e., 2.5GHz), which is a less-restrictive constraint. In our measurements, the total attenuation at 2.5GHz is approximately 10dB.

Figure 7.4.6 shows the jitter tolerance curve for 10Gb/s PRBS-7 input for cases of zero and ±300ppm frequency offset with a worst-case high-frequency jitter tolerance of 0.19Upp. In addition, we demonstrate successful operation when sampling below the baud rate by including a jitter tolerance curve for +1000ppm frequency offset. This offset is close to loop filter limit for this design.

Figure 7.4.7 shows the die micrograph. The I&D circuit, ADC (including demux), and digital CDR consume 1.7mW, 109mW, and 111.6mW, respectively.

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References:
Figure 7.4.1: Comparison of theoretical worst-case jitter tolerance given ideal channel, 1UI I&D, and 2UI I&D. Blind baud-rate samples can shift across a 1UI range due to frequency offset.

Figure 7.4.2: System block diagram of interleaved analog front end (1UI I&D and ADC) and digital CDR. Adjacent 1UI I&D samples are added in the digital CDR to form 2UI I&D samples.

Figure 7.4.3: Implementation of integrate-and-dump (I&D) circuit and 4-phase clock generator. C\textsubscript{i} is the input capacitance of the ADC.

Figure 7.4.4: Design and implementation of the speculative Mueller-Muller phase detector (MMPD).

Figure 7.4.5: Measured DC transfer curves of analog front end and eye diagram of 1UI I&D samples.

Figure 7.4.6: Measured jitter tolerance for 10Gb/s PRBS-7 with 10^{-12} BER, channel: 48” SMA cable.
Figure 7.4.7: Die micrograph.