29.2 A 235mW CT 0-3 MASH ADC Achieving -167dBFS/Hz NSD with 53MHz BW

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The trend for ADCs in wireless communication infrastructure is increased bandwidth with little or no relaxation in noise density or power consumption. The historical expectation of system designers is a noise spectral density (NSD) of -157dBFS/Hz with a power consumption of 0.5W. This expectation is a difficult one to meet with existing ADC architectures when the system bandwidth is 100MHz as demanded by standards such as LTE-A. The 0-3 continuous-time (CT) MASH [1-2] ADC described in this paper allows a direct-conversion receiver with the requisite bandwidth to be constructed, with 10dB lower noise than established benchmarks.

As shown in Fig. 29.2.1, the ADC consists of two stages: a residue-producing front end and a third-order feed-forward CT $\Delta\Sigma$ back end. The front end consists of a 16-step flash quantizer whose output V0 drives a 16-element current-mode DAC, IDAC0. The difference between the input current and the IDAC0 current is a residue signal that is digitized by the $\Delta\Sigma$ back end. The back end contains a 6-step flash quantizer whose output V1 drives the remaining 6-element current-mode DAC, IDAC1. A feed-forward structure is employed in the back end so that its sole feedback DAC is merged with IDAC0 into a single IDAC. As a consequence of this arrangement, the virtual ground established at the input of A1 by the $\Delta\Sigma$ loop ensures that in the high-gain region the output of IDAC is a faithful representation of the input signal. For a discrete-time implementation, V0 + V1 can be written as:

$$V0 + V1 = U + E0 + (-E0) * STF + E1 * NTF = U + (E0 + E1) * NTF$$

In the above equation, E0 and E1 are the quantization noise of FLASH0 and FLASH1, respectively, while STF and NTF are the signal and noise transfer functions of the $\Delta\Sigma$ back end. By virtue of the feed-forward topology of the loop filter, STF = 1 – NTF, which results in the final expression in the above equation. As this expression indicates, the signal transfer function of the system is unity and the NTF shapes E0 + E1. The digital signal V0 + V1 is therefore as faithful a representation of the input signal as NTF is small and IDAC is accurate. Furthermore, the system is free of out-of-band STF peaks even though the loop filter uses a feed-forward topology. Since the full scale (FS) of the back end is large enough to accommodate ~1LSB of front end over-load, the system can process input signals above the FS of the front-end flash quantizer. Also note that when the loop filter is implemented with CT circuitry, the system possesses inherent anti-aliasing despite the fact that sampling occurs in FLASH0 provided the additional aliasing component does not overload the $\Delta\Sigma$ back end.

Since the effective FS of the $\Delta\Sigma$ back end is a fraction (6/22) of the full ADC's FS, the band-edge gain of the first integrator is high (20dB) and thus the power efficiency of the ADC is maximized. Within the $\Delta\Sigma$ modulator, an R-C all-pass summer is utilized to provide wide-band summation in front of FLASH1. The LSBs of FLASH1 and the output swings of A1 to A3 are adjusted to allow such a passive summation.

A feed-forward amplifier is adopted in this design to achieve high bandwidth for given power and load requirements. Figure 29.2.2 shows the schematic of a single amplifier slice. A third-order topology is picked to achieve sufficient gain (~30dB) in the $\Delta\Sigma$ loop passband with large output swing (~0.9$V_{diff,p-p}$). The input stage is realized as a telescopic amplifier to achieve high voltage gain and low input-referred thermal noise. The signal swings at O1P and O1N are kept under tens of mV and their common-mode voltage is set to be the bias voltage for PMOS input pair M7-M8 of the second stage. M3 and M4 act as the direct feed-forward input pair for the second stage. Negative Miller compensation is applied to M3-M4 to reduce the capacitive loading on the input nodes. The outputs of the second stage, O2P and O2N, are used to drive the NMOS input pair M5-M6 of the third stage. A direct feed-forward input is applied to PMOS input pair M9-M10 through AC coupling. Compared to the second-order loop through M3-M4 and M5-M6, the first-order loop via M9-M10 has much less common-mode degeneration in order to improve common-mode stability. In addition, the source node of M1-M2, VS1, contains the common-mode voltage of the differential input and is used to drive M13 at high frequencies to further enhance common-mode stability. A1 contains 16 slices of the amplifier as shown in Fig. 29.2.2 while A2 and A3 contain 2 slices each. In post-layout simulations, each amplifier (A1-A3) achieves an in-band gain of 31 dB with a unity-gain frequency of 8.6 GHz.

A fully complementary current-steering DAC is used to implement IDAC. Figure 29.2.3 shows the schematic of a single IDAC element. Thick-oxide devices M1 and M8 together with cascode core devices M2 and M7 provide accurate P and N currents that are steered by the switching quad consisting of core devices M3 to M6. M1 and M8 are sized for static matching while M2 to M7 are sized for speed and desired output impedance across process corners. 1.8V and –1.0V supplies are utilized to provide large voltage headroom for both current sources to minimize thermal noise. Shown in the DAC timing diagram, the flash output data, T, is generated after the rising edge of the clock signal CK and gets latched at the end of the clock period by a pulse signal, CKD. This timing arrangement gives almost one clock period for the flash regeneration and logic delays in the feedback path. The one clock period delay in the flash-DAC path is compensated by the direct feedback to the input of FLASH1 provided through the VDAC element as shown in Fig. 29.2.1.

The ADC is fabricated in a digital 28nm bulk CMOS process with a 0.9V core supply voltage. The active area of the ADC is about 0.9mm by 1.0mm. The ADC is clocked at 3.2GHz and draws a combined DC power of 235mW from the 0.9/1.8/–1.0V power supplies. The effective signal bandwidth is 53.3MHz with an OSR of 30. The top and middle plots in Fig. 29.2.4 show the measured spectra of the combined output, V0 + V1, with a –2dBFS input tone at 30MHz. The bottom plot in Fig. 29.2.4 gives the measured spectra with two –8dBFS input tones at 30MHz and 32MHz. The IMD3 and IMD2 are –67.5dB and –66.3dB, respectively. Figure 29.2.5 shows the measured SNR as a function of the input signal amplitude. A peak SNR of 83.2dB is achieved at –2dBFS input. The measured passband noise floor with small input signal is at –167.2dBFS/Hz or –90dBFS integrated, resulting in a dynamic range (DR) of 88dB. The corresponding thermal-noise figure-of-merit (FOM) is thus 171.6dB. With a single-tone signal at 15MHz, the achieved peak SNDR is 71.4dB at –15dBFS input. The SNDR performance is believed to be limited by the timing skew and transition error among the 22 DAC elements in IDAC. Figure 29.2.6 compares this work with CT $\Delta\Sigma$ ADCs recently published at ISSCC. Figure 29.2.7 shows the microphotograph of the test chip. This work achieves a higher DR and thermal-noise FOM than others with a bandwidth of more than 50MHz.

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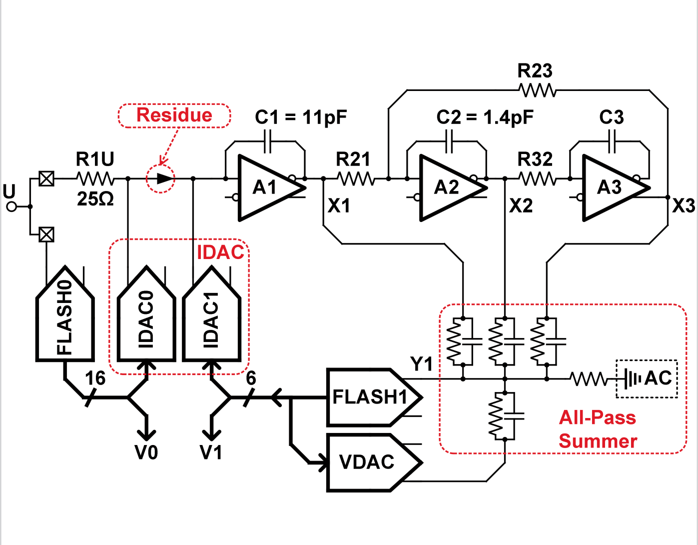

Figure 29.2.1: Single-ended representation of the 0-3 MASH CT ΔΣ ADC.

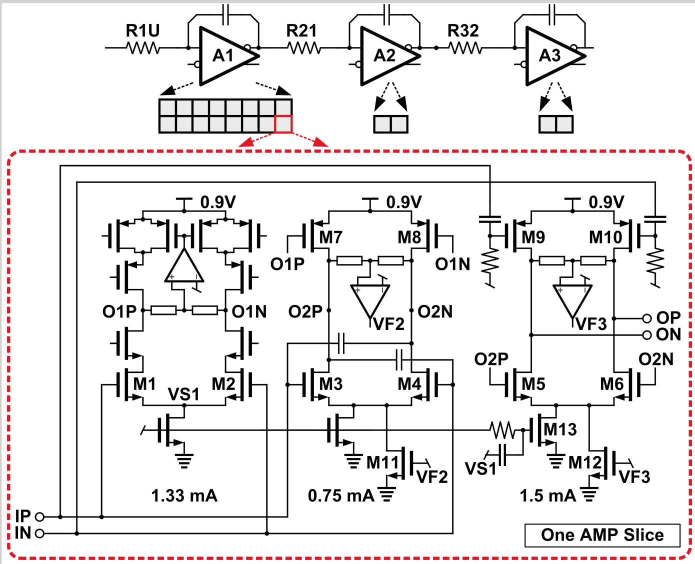

Figure 29.2.2: Amplifier slice allocation and slice schematic.

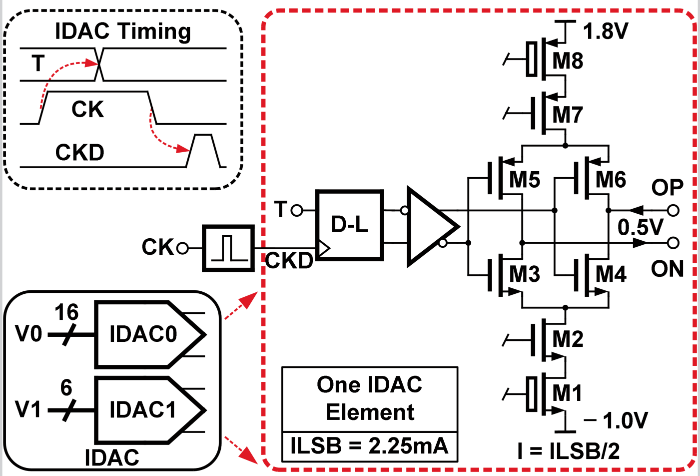

Figure 29.2.3: Schematic and timing diagram of the fully-complementary IDAC.

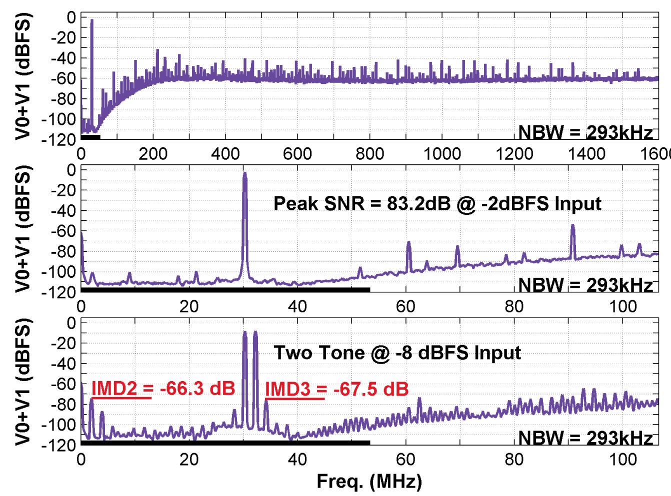

Figure 29.2.4: Measured spectra (top) -2dBFS tone at 30MHz, (middle) -2dBFS tone at 30MHz zoomed in, (bottom) -8dBFS tones at 30MHz and 32MHz.

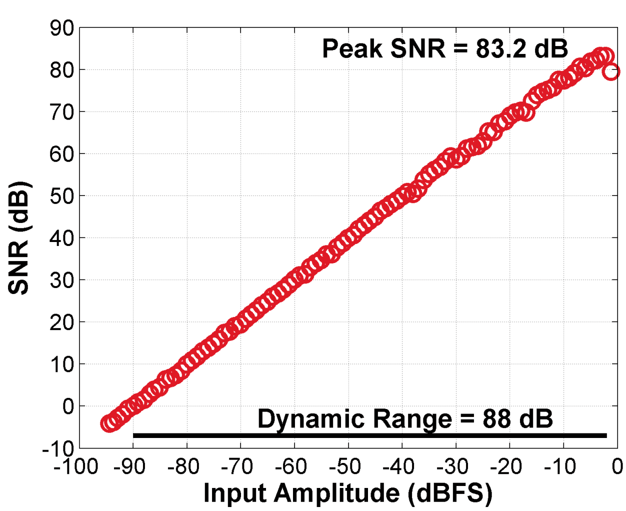

Figure 29.2.5: Measured SNR as a function of input signal amplitude at 30MHz.

Publication	This Work		[3]	[4]	[5]	[6]
			ISSCC 12	ISSCC 12	ISSCC 12	ISSCC 13
CMOS L_{MIN}	**28nm**		90nm	65nm	45nm	28nm
Active Area	**0.9mm^2**		0.12mm^2	5.5mm^2	0.49mm^2	0.08mm^2
Supply Voltages	**0.9/1.8/–1.0V**		1.2V	1.2/±2.5V	1.4/1.8V	N.A.
Sampling Rate	**3.2GHz**		3.6GHz	4.0GHz	6.0GHz	0.64GHz
Power (*P*)	**235mW**		15mW	750mW	20mW	3.9mW
OSR	**35**	**30**	50	26.6	50	17.7
Bandwidth (*BW*)	**45.7MHz**	**53.3MHz**	36MHz	75MHz	60MHz	18MHz
*DR**	**90dB**	**88dB**	80dB*	79dB	62dB	78.1dB
SNRmax	**84.6dB**	**83.1dB**	76.4dB	N.A.	61.5dB	N.A.
SNDRmax	**72.6dB**	**71.4dB**	70.9dB	N.A.	60.6dB	73.6dB
$(DR-1.76)/6.02$	**14.7**	**14.3**	13	12.5	10	12.7
$DR+10\log_{10}(BW/P)$	**172.9dB**	**171.6dB**	173.8dB	158.2dB	156.8dB	174.7dB
$P/(2BW\cdot 2^{(DR-1.76)/6.02})$	**96.7fJ**	**107fJ**	25.5fJ	686fJ	162.8fJ	16.5fJ

* *DR* is measured as the input signal range corresponding to 0 dB SNR and peak SNR

Figure 29.2.6: Comparison of this work with state-of-the-art CT ΔΣ ADCs.

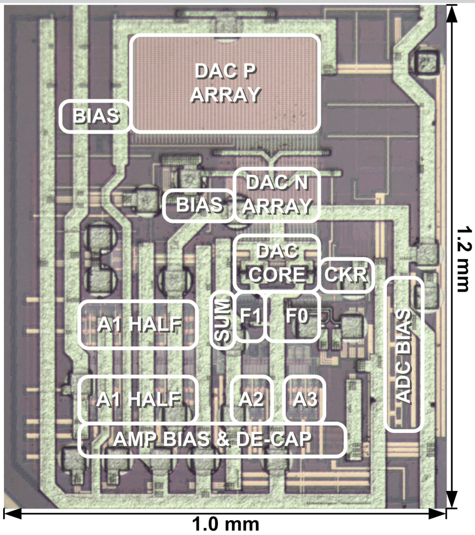

Figure 29.2.7: Microphotograph of the 0-3 MASH ADC test chip in 28nm CMOS.