A Current-Based Reference-Generation Scheme for 1T-1C Ferroelectric Random-Access Memories

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***Abstract*—A reference generation scheme is proposed for a 1T-1C ferroelectric random-access memory (FeRAM) architecture that balances fatigue evenly between memory cells and reference cells. This is achieved by including a reference cell per row (instead of per column) of the memory array. The proposed scheme converts the bitline voltage to current and compares this current against a reference current using a current-steering sense amplifier. This scheme is evaluated over a range of bitline lengths and cell sizes in a 16-kb test chip implemented in a 0.35-μm FeRAM process. The test chip measures an access time of 62 ns at room temperature using a 3-V power supply.**

***Index Terms*—1T-1C, ferroelectric memory, memory circuit design, nonvolatile, reference generation, sensing scheme.**

I. Introduction

AMONG THE family of nonvolatile memories, ferroelectric random access memories (FeRAMs) are well known for their low-power and fast-write operations [1]. These two features have given FeRAMs an advantage over flash memories and electrically erasable programmable read-only memories (EEPROMs) in applications such as contactless smart cards, digital cameras, and dynamically programmable gate arrays [2]. The density of FeRAMs, however, still lags behind those of EEPROMs and flash memories. This is partly due to FeRAMs using two transistors and two capacitors in each storage cell, known as *2T-2C cell* [1]. A 2T-2C cell allows for both the data and its complement to be stored in the same cell, providing robustness to process variations and ease of sensing to data retrieval. A more area-efficient FeRAM, however, uses only one transistor and one capacitor per storage cell, known as *1T-1C cell*. Fig. 1 illustrates the two cells along with provisions for their data sensing. The 2T-2C cell is self-referenced, storing the reference data (the data complement) alongside the data in the same cell, in every cell of the array. The 1T-1C cell occupies only half of the area of the 2T-2C cell, but requires instead a reference for data sensing. A reference cell, shared among several cells, generates a reference voltage $V_{\rm ref}$ or a reference current $I_{\rm ref}$. Ideally, $V_{\rm ref}$ must be halfway between V_0 and V_1 to provide equal sense margins for stored "0" and stored "1," where V_0 and V_1, respectively, refer to the bitline voltage corresponding to a stored "0" and a stored "1." Generating a close-to-ideal $V_{\rm ref}$, however, is not without challenge, considering that only approximate values of V_0 and V_1 are known in advance, and that these values are subject to process variations and ferroelectric-material degradation with time. Similarly, an ideal $I_{\rm ref}$ must be halfway between I_0 and I_1, the cell currents associated, respectively, with a stored "0" and a stored "1."

In Section II, we will briefly review and compare the conventional scheme of reference generation against our current-based reference-generation scheme [3]. Section III describes the details of a 256×64-bit 1T-1C FeRAM test chip that implements our proposed scheme along with a current-steering sense amplifier. Section IV provides the simulation and measurement results of the reference scheme as implemented. We have further simulated the reference scheme using HSPICE in conjunction with a parallel-element macromodel [4] in Section V to determine the robustness of this scheme to process variations and to other design parameters. Finally, Section VI presents our conclusions for this work.

II. Reference Generation

Ideally, a reference voltage is halfway between V_0 and V_1 (as shown in Fig. 1) and tracks changes of V_0 and V_1 with time. This implies that a fixed value of $V_{\rm ref}$ could be used across the chip [5] only if this fixed value provides enough sensing margin across the chip and over time, a condition difficult to meet in today's ferroelectric materials [6]. Two less demanding solutions to reference generation are shown in Fig. 2(a) and (b).

Fig. 2(a) depicts a 1T-1C memory array with folded-bitline architecture where one reference cell is shared among all cells on the same bitline (column). Whenever an odd row is selected (by activating WL_O and PL_O), the odd reference row is also selected by activating RWL_O and RPL_O. In this method, $V_{\rm ref}$ is generated separately for each column at the time of data retrieval [7]. This reduces the effect of columnwise process variation on the sensing signal, but fatigues the reference cells at a rate different from that of the memory cells in that column. For example, if n cells in a column are accessed sequentially, an identical reference cell in that column is accessed n times and, hence, fatigued n times faster than the actual data cells in the column, reducing the effective lifetime of the FeRAM memory by a factor of n. In contrast, Fig. 2(b) shows a 1T-1C memory array where the reference cells are shared among all the cells

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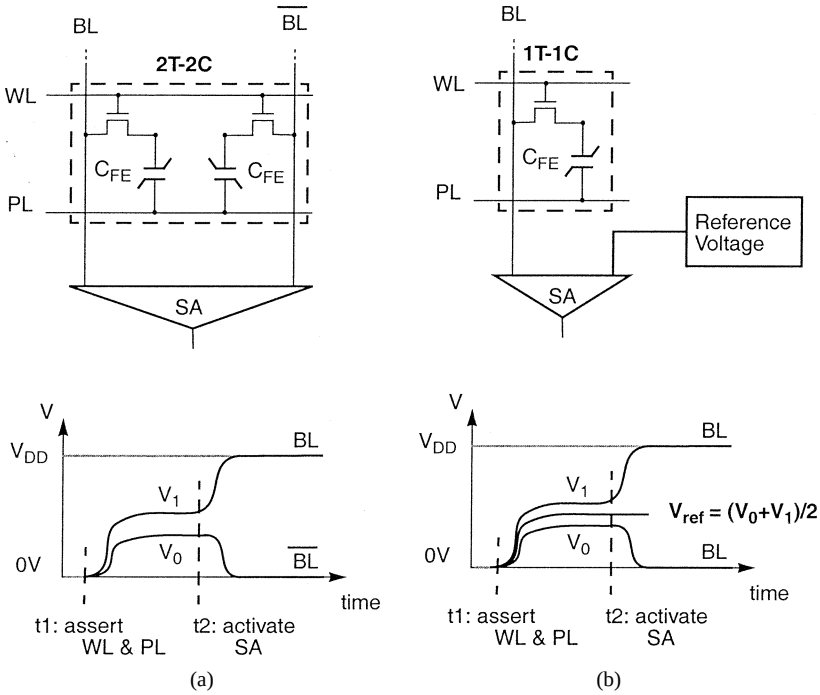


Fig. 1. Reference voltage generation for (a) 2T-2C architecture and (b) 1T-1C architecture. A 2T-2C cell is self-referenced. A 1T-1C cell occupies half the silicon area of a 2T-2C cell, but requires a reference voltage.

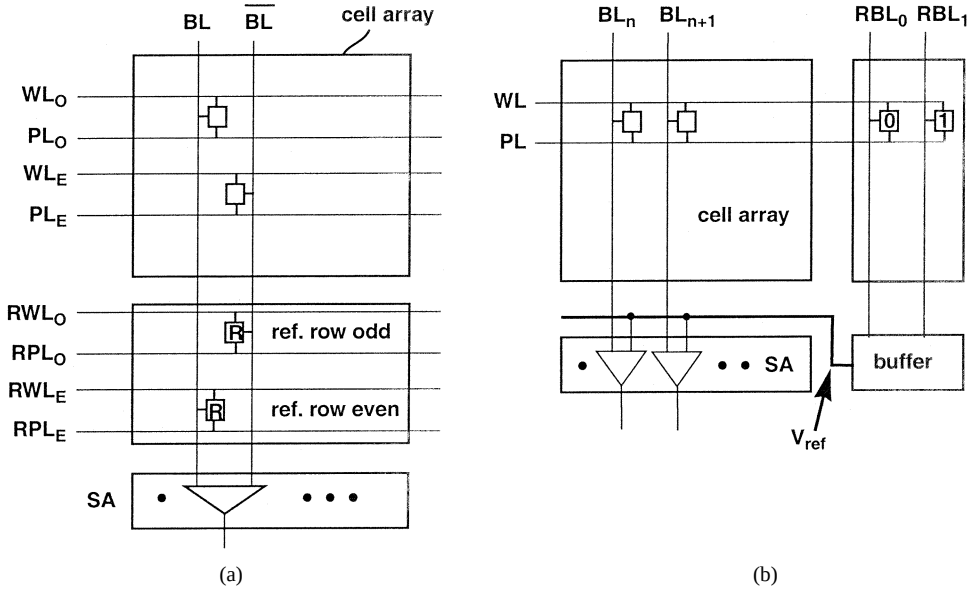


Fig. 2. Reference generation schemes. (a) Sharing reference cells among cells in a column. (b) Sharing reference cells among cells in a row.

on the same wordline (row). Whenever a row is selected (by activating WL and PL), two reference cells on the same row are automatically selected, creating V_0 and V_1 on two reference bitlines (RBL and $\overline{\text{RBL}}$). In this method, V_{ref} is generated separately for each row of the memory array at the time of data retrieval [8], [9]. This reduces the effect of rowwise process variation on the sensing signal, and more importantly, fatigues the reference cells at exactly the same rate as those of the data cells in the same row.

The generated V_{ref} in Fig. 2(b) needs to be shared among the sense amplifiers of the neighboring columns. This requires buffering of V_{ref} subject to two constraints: 1) the added buffer must fit together with the sense amplifiers in the tight pitch of the memory array, and 2) the added buffer must maintain the capacitive balance among all the bitlines and the two reference bitlines.

One way to satisfy the above-mentioned constraints is to convert V_{ref} into current and mirror that current locally to each neighboring column for sensing. This is the basis of our current-based reference-generation read scheme. Fig. 3 shows an implementation of this idea, using two reference cells per eight data columns. RBL and $\overline{\text{RBL}}$ are each connected to a memory cell, one storing a "1" and the other storing a "0." During read access, V_x (V_0 or V_1) appears on BL, V_1 on RBL, and V_0 on $\overline{\text{RBL}}$. The voltages V_x on BL, V_1 on RBL, and V_0 on $\overline{\text{RBL}}$ are then converted to currents I_x, I_1, and I_0, respectively, by iden-

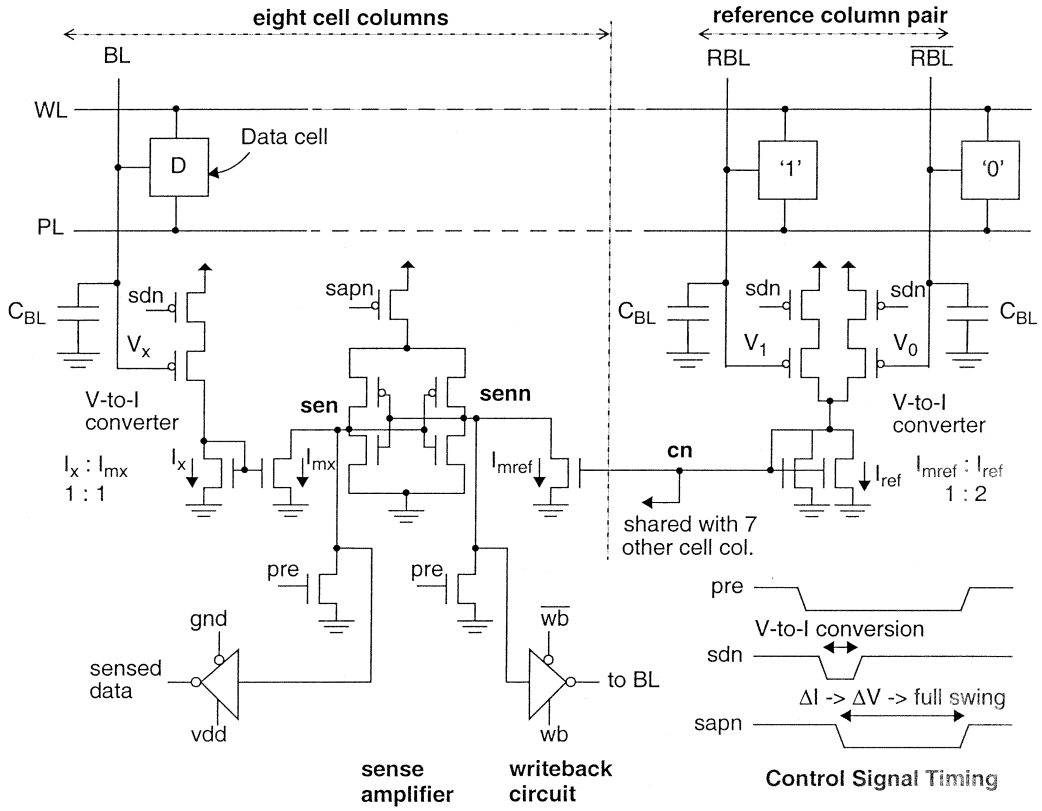


Fig. 3. Proposed current-based sensing scheme for 1T-1C FeRAM.

tical pMOS transistors. I_1 and I_0 are further added together and mirrored with half amplitude to provide $I_{m\text{ref}}$ (the arithmetic average of I_0 and I_1) to each of the eight neighboring-column sense amplifiers. The number of sense amplifiers that share this reference current determines the speed of memory read access. We discuss this issue in more detail in Section V.

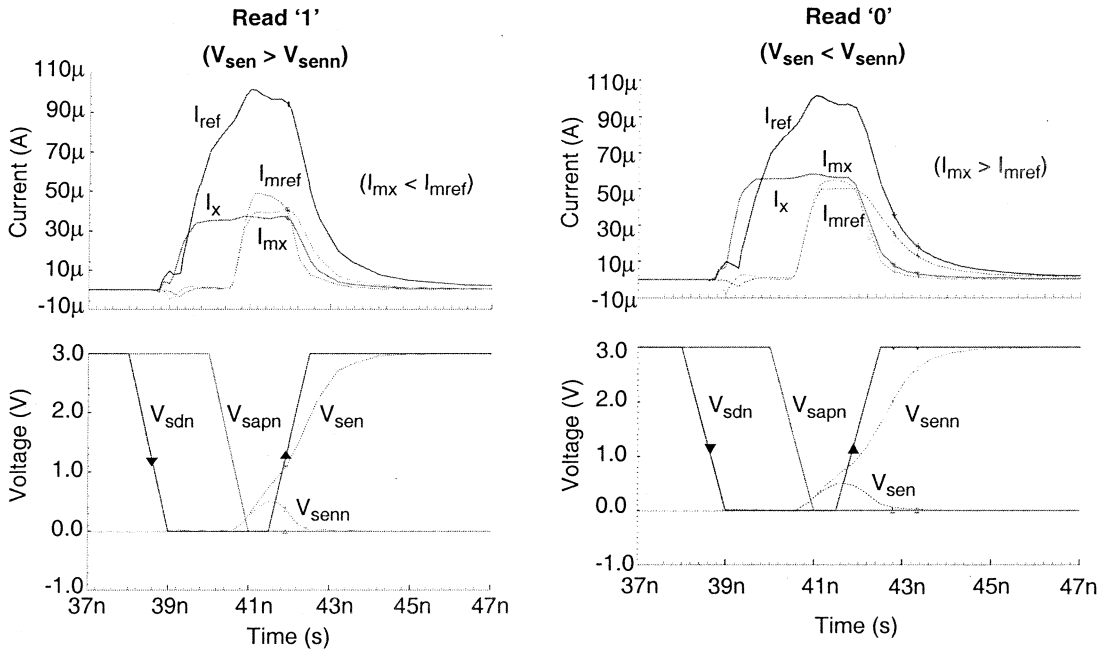
Similar to I_{ref}, I_x for each column is also mirrored to provide I_{mx} to the column sense amplifier. Since I_x is either I_1 or I_0 and I_0 is larger than I_1 (because $V_0 < V_1$), I_{mx} is either smaller than $I_{m\text{ref}}$ (for a stored "1") or greater than $I_{m\text{ref}}$ (for a stored "0"). Once the currents are set up, the sense amplifiers for all columns are turned on and the currents I_{mx} and $I_{m\text{ref}}$ compete to pull down their corresponding nodes, sen and senn. The side with smaller current will regenerate to V_{DD}, forcing the other side to ground (GND). The read, as described, is destructive, and must be followed by a write-back operation. This is achieved by using an inverter controlled by wb and $\overline{\text{wb}}$, as shown in Fig. 3. This inverter reinforces the appropriate data on the bitline during the write-back cycle.

Fig. 4 shows the control signals and the critical currents and voltages of the sense amplifier as functions of time. After precharging nodes sen and senn to GND and rising the selected WL and PL to V_{DD}, the detection process starts with the activation of the sdn signal that converts the voltages on BL, RBL, and $\overline{\text{RBL}}$ to currents. Once the currents are set up, the sense amplifiers are activated by asserting the sapn signal. If the stored data is a "1," I_{mx} will be smaller than $I_{m\text{ref}}$, causing the voltage on node sen to rise faster than the voltage on node senn. V_{sen} continues to rise to V_{DD} while V_{senn} reverses course and moves toward GND due to the feedback in the sense amplifier. The opposite is true for a stored "0" case with the voltages on nodes sen and senn finally settling to GND and V_{DD}, respectively. In both cases, the sense operation is completed in less than 6 ns from the time of activating sdn.

III. Test-Chip Architecture

The proposed sensing scheme is implemented in a test chip with a 256 × 64-bit cell array, shown in Fig. 5. In order to test the sensing scheme and the sense amplifier over a range of bitline capacitance (C_{BL}) and ferroelectric cell capacitance (C_{FE}), we have implemented four distinct bitline lengths and four distinct sizes of cell capacitor. The shortest bitline corresponds to 64 rows of 1T-1C cells, while the longest bitline corresponds to 256 rows of 1T-1C cells. As a result, C_{BL} can take one of four values, that is, from one to four times the minimum C_{BL}. Also, a group of four consecutive rows implements four distinct sizes of ferroelectric capacitors: from one (1-μm^2 area) to four times the minimum cell capacitance. Using an extra row-address bit, as described later in this section, up to three rows can be accessed in a set of four consecutive rows, hence, C_{FE} up to 8 × can be tested. Overall, 32 different combinations of C_{BL} and C_{FE} are available on the test chip for experimentation purposes.

To keep the coupling effects of the neighboring bitlines the same as in a production chip, the column pitch is kept constant at its minimum across the chip. The row pitch is also fixed (at 5.5 μm) to accommodate the largest cell. To keep the memory array homogeneous, the whole memory array is designed in a rectangular form, with all memory cells in place. To mimic shorter bitlines, some memory cells are not connected to the



(a) (b)

Fig. 4. Simulation results of the proposed sensing scheme. (a) Reading stored "1." (b) Reading stored "0."

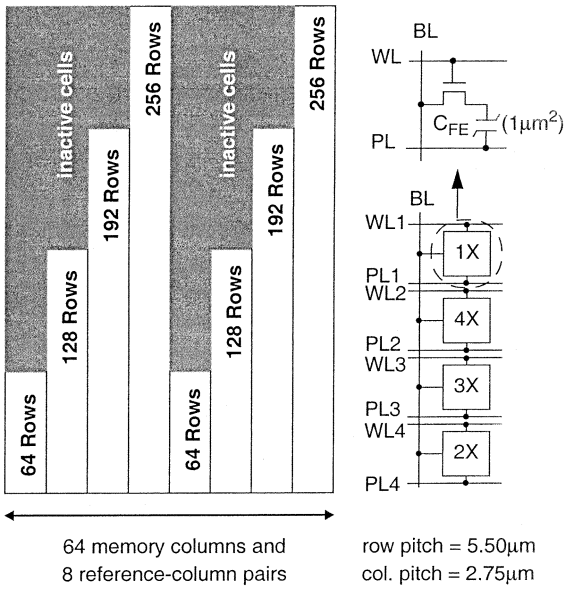


Fig. 5. Test-chip architecture featuring four distinct bitline lengths and four distinct cell sizes.

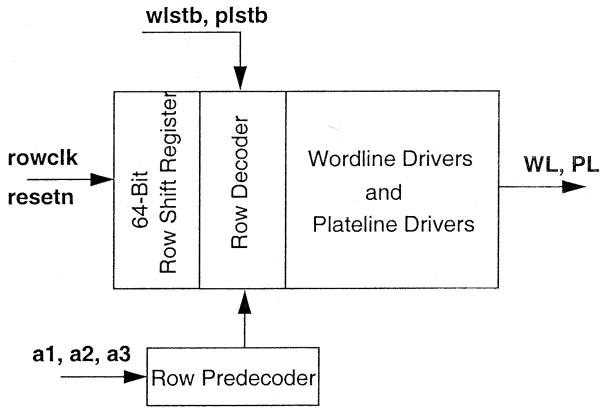


Fig. 6. Test-chip architecture: row-access block diagram.

bitlines and never accessed. These cells are marked as inactive cells in Fig. 5. Each sense amplifier is laid out in a span of four column pitches, sharing this space with three other sense amplifiers. Each sense amplifier is fed by a reference signal from one side and by its corresponding bitline from the other side.

A simple addressing scheme is used for both rows and columns of the memory array. The block diagram of the row addressing circuit is shown in Fig. 6. The 256 rows are divided into 64 blocks of four rows each. A block is addressed using a 64-bit shift register containing a single "1" and 63 "0"s. The shift register is initially reset to "000…001" pointing to the first block. The lone "1" is shifted to the proper bit location using a shift-clock signal. Once a block of rows is identified, a predecoder uses two address bits to select one of four rows in the block. A third address bit is used to simultaneously activate more than one row in a block. This allows us to connect to bitline a range of cell capacitors from 1 to $8\times$. A similar 16-bit shift register is used to identify a block of four columns among a total of 16 column blocks. A column predecoder decodes two column-address bits to select a column among four columns in the column block.

A monitor circuit is used in each column to monitor the voltages of selected bitlines during a read cycle. The monitor circuit, shown on the right-hand side of Fig. 7(a), consists of a pMOS transistor that buffers the bitline (RBL is shown as an example) and a transmission gate that selects the buffered value for off-chip monitoring at the pin labeled as $V_{\rm out}$. This pin is connected externally via a pullup resistor to V_{DD}. The measured and simulated input–output characteristics of the monitor circuit when a 3-V supply is used is shown in Fig. 7(b), demonstrating a linear $V_{\rm out}$–$V_{\rm in}$ relationship over a range of 0–2.1 V of $V_{\rm in}$.

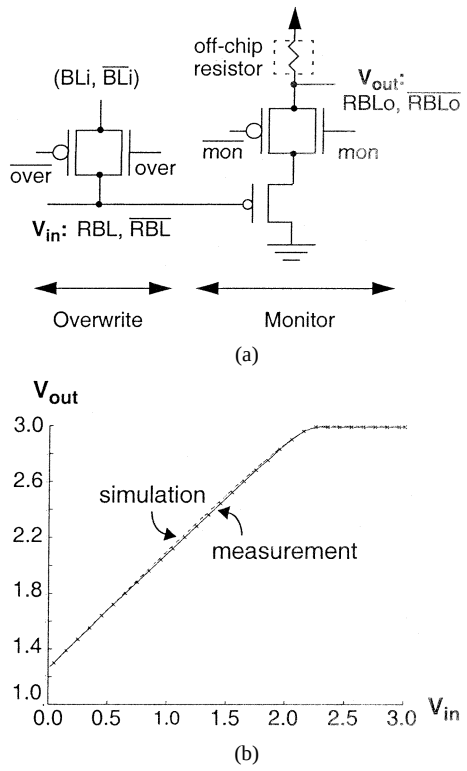


Fig. 7. (a) Monitor and overwrite circuitry. (b) Monitor circuit simulated and measured characteristics.

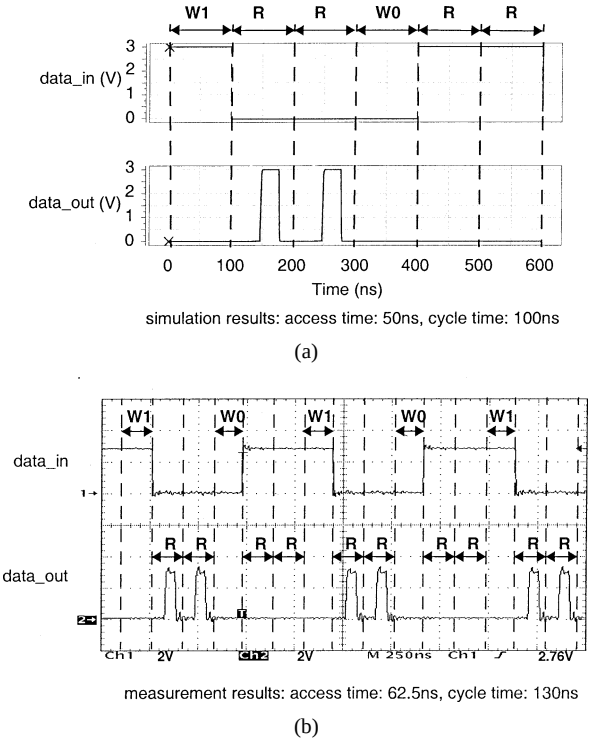


Fig. 8. (a) Simulation results and (b) measurement results confirm successful write operations, read operations, and write-back operations across the chip.

An overwrite circuit, shown on the left-hand side of Fig. 7(a), can overwrite an externally provided voltage on a selected bitline for sense-amplifier sensitivity measurements. The circuit consists of a transmission gate that is activated when the over signal is asserted, connecting the externally provided BLi and $\overline{\text{BLi}}$ signals to the selected bitline.

IV. Simulation and Measurement Results

Three sets of simulation and measurement were performed with the following objectives: 1) to identify functional cells among various cell sizes and bitline lengths; 2) to determine the range of bitline voltage and its effect on the sense amplifier operations; and 3) to determine the sense-amplifier sensitivity. We present these results in the following.

A cell is considered functional if we can successfully write into the cell and read from the cell. Since read is destructive, a successful read implies a successful write-back into the cell. As shown in Fig. 8, a sequence of six memory operations is devised to confirm the cell functionality, that is, writing a "1" into the cell followed by two consecutive reads, then writing a "0" into the cell followed by two consecutive reads. The first read after write verifies the corresponding write. A consistent second read verifies successful write-back during the first read. Our measurement results confirm that the cell functionality is unaffected by the range of cell size and bitline length implemented in this test chip. However, the bitline voltage available for sensing is directly related to the ratio $C_{\text{BL}}/C_{\text{FE}}$, as we discuss next.

We have simulated and measured $V_{\text{RBL}}(V_1)$, $V_{\overline{\text{RBL}}}(V_0)$, and $\Delta V_{\text{BL}}[(V_1 - V_0)/2]$ as functions of $C_{\text{BL}}/C_{\text{FE}}$, over a range of $C_{\text{BL}}/C_{\text{FE}}$ implemented in the test chip. The results are shown in Fig. 9. V_{RBL} and $V_{\overline{\text{RBL}}}$ have their maximum values at minimum $C_{\text{BL}}/C_{\text{FE}}$, corresponding to the smallest bitline and largest C_{FE}. Also, as expected, both V_{RBL} and $V_{\overline{\text{RBL}}}$ are monotonically decreasing functions of $C_{\text{BL}}/C_{\text{FE}}$. In contrast, ΔV_{BL} has a peak at around $C_{\text{BL}}/C_{\text{FE}} = 0.75$. Measured V_{RBL} has a range of 0.6–1.9 V and measured $V_{\overline{\text{RBL}}}$ has a range of 0.2–1.8 V. Except for very small C_{BL} or very large $C_{\text{FE}}(C_{\text{BL}}/C_{\text{FE}} < 0.25)$, ΔV_{BL} is always larger than 0.2 V, providing a good sense margin for the sense amplifier. Moreover, in the vicinity of the maximum ΔV_{BL}, both V_{RBL} and $V_{\overline{\text{RBL}}}$ are larger than 0.5 V, providing a good common-mode voltage for the sense-amplifier operation.

To determine the range of V_{BL}, V_{RBL}, and $V_{\overline{\text{RBL}}}$ for which the sense amplifier correctly detects a "1" and a "0," we have applied a fixed voltage (in the 0.2–2 V range) to V_{BL} and V_{RBL} while sweeping $V_{\overline{\text{RBL}}}$ over the same range. Ideally, the sense amplifier should resolve any $\Delta V_{\text{BL}} < 0$ as "0" and any $\Delta V_{\text{BL}} > 0$ as "1," where $\Delta V_{\text{BL}} = V_{\text{BL}} - (V_{\text{RBL}} + V_{\overline{\text{RBL}}})/2)$ or, equivalently, $\Delta V_{\text{BL}} = (V_{\text{RBL}} - V_{\overline{\text{RBL}}})/2$, since we have chosen $V_{\text{BL}} = V_{\text{RBL}}$. Our measurement results, however, indicate a region, specified as the *metastability region* in Fig. 10, as the dividing region between "0" and "1" regions. The metastability region falls below $\Delta V_{\text{BL}} = -0.2$ V (corresponding to $V_{\text{RBL}} - V_{\overline{\text{RBL}}} = -0.4$ V) and above $\Delta V_{\text{BL}} = 0.2$ V (corresponding to $V_{\text{RBL}} - V_{\overline{\text{RBL}}} = 0.4$ V). This should be compared against measured V_{RBL} and $V_{\overline{\text{RBL}}}$ that correspond to actual data points over the entire range of $C_{\text{BL}}/C_{\text{FE}}$, as shown in Fig. 9. These data points and their complements, as shown in Fig. 10, fall outside the metastability region and, therefore, result in correct sensing of "0" and "1."

Extensive measurement results confirm that the sensing scheme correctly functions over the entire range of V_{RBL} and

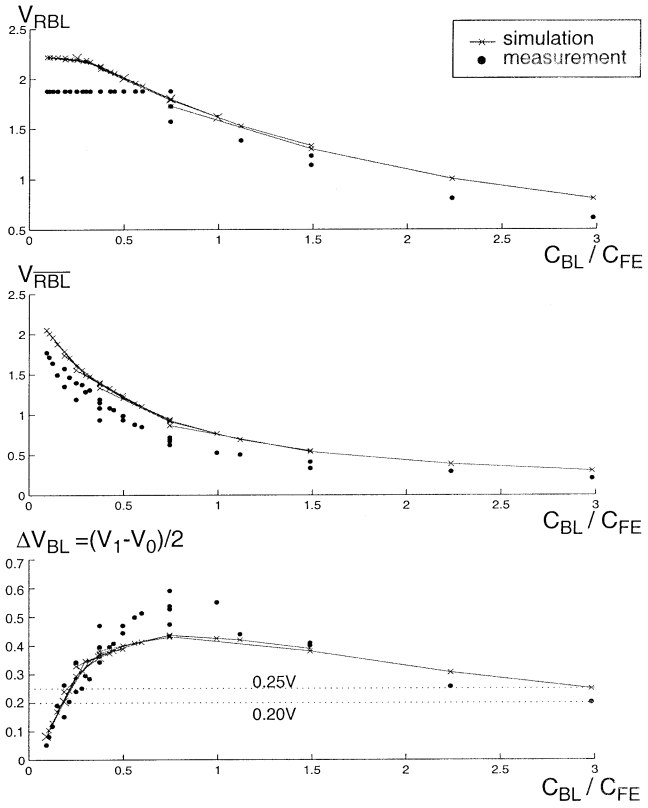


Fig. 9. Simulation and measurement results: single-ended and differential bitline signals as functions of $C_{\rm BL}/C_{\rm FE}$.

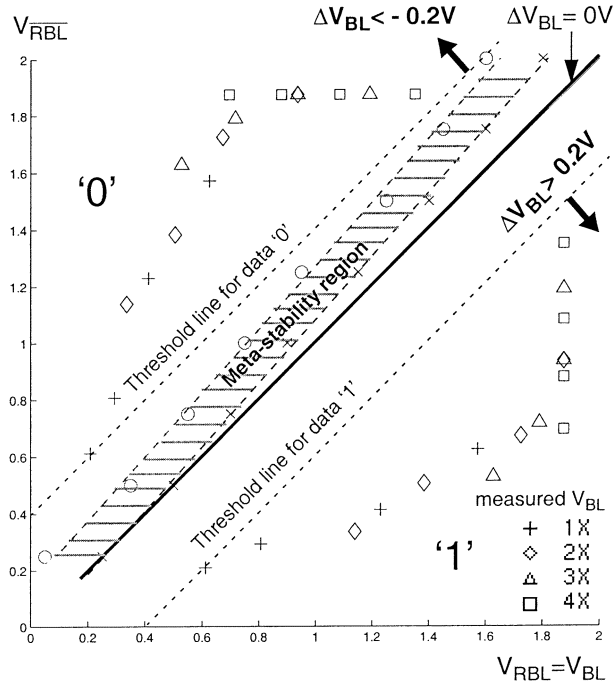


Fig. 10. Measured characteristics of the sense amplifier.

$V_{\overline{\rm RBL}}$. Measurement results show an access time of 62.5 ns and a cycle time of 130 ns (both multiples of 6.25 ns, which is the minimum time step of the tester used). Simulation results suggest an access time of 50 ns and a cycle time of 100 ns, all at $V_{DD} = 3$ V and room temperature.

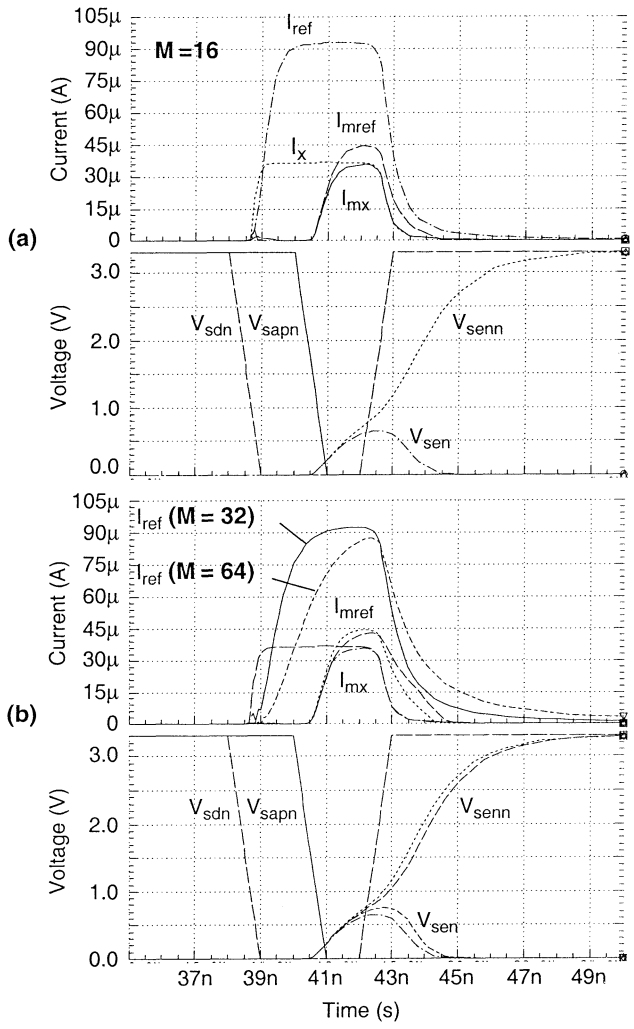


Fig. 11. Simulation results for the proposed sense amplifier (a) using 16 columns per reference column ($M = 16$), and (b) using 32 ($M = 32$) and 64 columns ($M = 64$) per reference column.

V. Discussion

As briefly mentioned in Section II, the access time of the current-based sensing scheme depends on the number of sense amplifiers sharing the same $I_{m\rm ref}$. Referring to Fig. 3, this is due to increasing the capacitance of the common node cn which is proportional to the number of data columns M sharing the same $I_{m\rm ref}$. The test chip uses $M = 8$. A larger M implies higher capacitance at cn and, hence, a longer rise time for the voltage at cn. A smaller M implies a shorter rise time and, hence, an increased speed at the expense of additional silicon area to include more reference columns in the array.

Referring to Fig. 4, the control signal $V_{\rm sapn}$ must be activated after cn has reached its peak value; otherwise, a read error may occur. We have performed various simulations on this circuit to verify circuit functionality and to determine the critical M for typical timing of $V_{\rm sdn}$ and $V_{\rm sapn}$. Simulation results for the cases of $M = 16$, $M = 32$, and $M = 64$, shown in Fig. 11, confirm correct read operation despite the slower rise time for $I_{\rm ref}$. $I_{m\rm ref}$ and I_{mx} show little change compared to the case of $M = 8$.

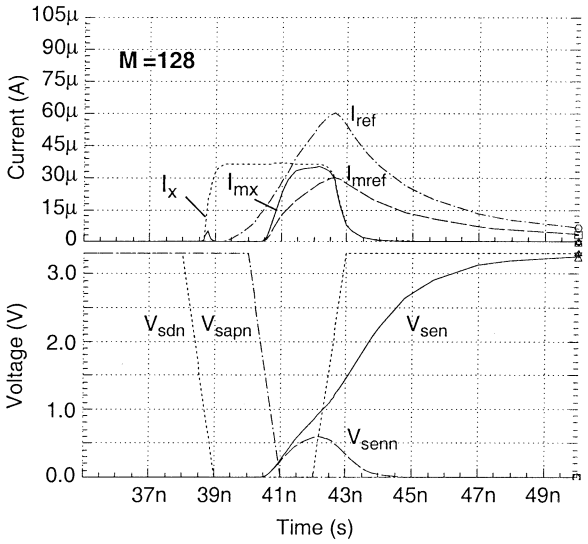


Fig. 12. Simulation results for the proposed sense amplifier with $M = 128$. The erroneous results of sensed data suggests delaying of $V_{\rm sapn}$ with respect to $V_{\rm sdn}$.

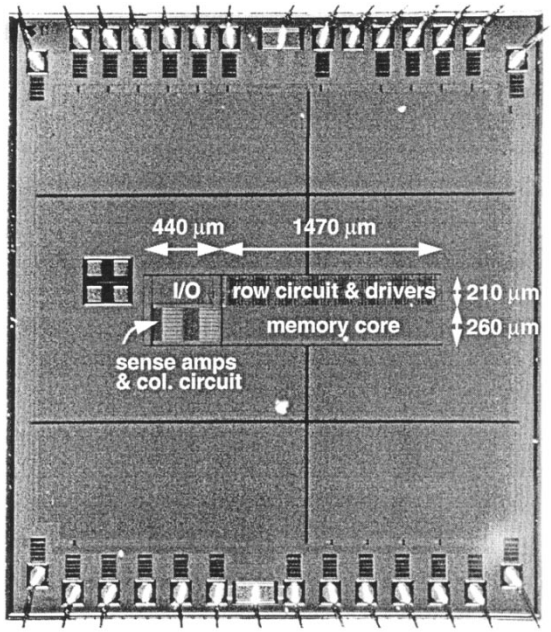


Fig. 13. Test-chip micrograph.

When M is increased to 128, however, both $I_{\rm ref}$ and $I_{m\rm ref}$ are slowed down significantly (refer to Fig. 12), to a point where the stored data is erroneously sensed. This is due to $I_{\rm ref}$ not reaching its peak value at the time of deactivating $\rm sdn$. In order to remedy this situation, both activating $\rm sapn$ and deactivating $\rm sdn$ must be further delayed until $I_{\rm ref}$ has reached its peak value. Simulation results confirm that by delaying $\rm sapn$ and $\rm sdn$ by 1.5 ns, the sense amplifier correctly detects the bit value. This delay is the tradeoff for reducing area overhead from 4% to 2%.

A test-chip micrograph is shown in Fig. 13. The wiring to bonding pads is not seen in the micrograph because the active

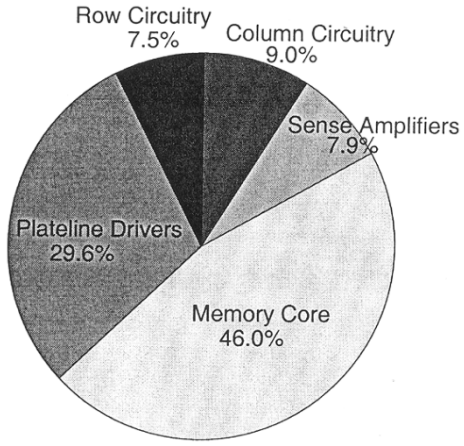


Fig. 14. Layout-area distribution of various blocks in the test chip.

TABLE I
TEST-CHIP CHARACTERISTICS

Technology	0.35mm, 3-metal, PZT-film
Organization	256x64-bit
Chip Size	0.47mm x 1.91mm = 0.90mm^2
Supply Voltage	3V
Access Time	62.5ns (measured at 3V, 25 ^{o}C)
Cycle Time	130ns (measured at 3V, 25 ^{o}C)

area of the chip is covered by dummy metal patterns. This is to avoid thinning of the sparse metal wires during the patterning process. The solid black lines on the periphery connect the core to the V_{DD} ring, the GND ring, and to the pads. The pie chart in Fig. 14 shows the distribution of the silicon area dedicated to each block of the test chip. The fraction of the total area occupied by the plateline drivers is quite noticeable in this figure: it is close to 30% of the total area. This large area is required to move highly capacitive platelines in this scheme. To reduce this area, the sensing scheme must be modified to either keep the plateline small, as in [10], or keep the plateline constant, as in [11]–[13].

VI. CONCLUSION

We have demonstrated successful operation of a current-based reference-generation scheme, along with a current-steering sense amplifier, for 1T-1C FeRAM. We have achieved this through simulation and measurement results of a 16-kb test chip implemented in a 0.35-μm FeRAM process.

Our measurement results indicate that there is a relatively wide range of $C_{\rm BL}/C_{\rm FE}$ for which the memory cells are functional, although there is a smaller range for which the sensing voltage is close to its peak value. Also, the current-based sensing scheme can be used in various settings of area–speed tradeoff. The main features of the test chip, at one pair of reference columns per eight data columns, are summarized in Table I.

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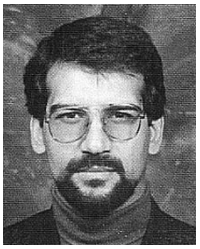

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