A Continuous-Time 0–3 MASH ADC Achieving 88 dB DR With 53 MHz BW in 28 nm CMOS

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***Abstract*—We present design and measurement details for a 0–3 multi-stage noise-shaping (MASH) ADC that achieves a dynamic range of 88 dB over 53 MHz signal bandwidth. The ADC utilizes a zeroth-order front-end, i.e., a 17-level flash ADC, to perform a coarse quantization and a third-order 7-level continuous-time ΔΣ back-end to digitize the residue error of the front-end. The ADC achieves the high thermal noise power efficiency of a continuous-time feedforward ΔΣ modulator and the flat signal transfer function of a flash ADC. The test chip, implemented in a 28 nm CMOS process, clocks at 3.2 GHz. The average noise spectral density with small input signals is –167 dBFS/Hz and the dynamic range is 88 dB. The test chip ADC consumes a total power of 235 mW from triple power supplies of 0.9/1.8/–1.0 V. The thermal-noise figure-of-merit, defined as FOM = DR + 10log$_{10}$ (BW/P) is 171.6 dB.**

***Index Terms*—Delta-sigma, MASH, continuous-time, CTDS, ADC, 0-X MASH, CT MASH.**

I. Introduction

THE demand for higher data rates in wireless communications translates into higher bandwidth requirements for analog-to-digital converters (ADCs) inside cellular base-station receivers. The increased interest in multi-in-multi-out (MIMO) systems also drives the demand for multiple ADCs in a single package. In addition, the constant drive to reduce the system-level complexity and component cost of base stations limits the package options for ADCs and therefore limits their power consumption. As a result, the ADCs inside such systems are expected to achieve better power efficiency despite the increased bandwidth. The expectation for the noise spectral density (NSD) of such ADCs is approximately −160 dBFS/Hz. Achieving a lower NSD increases the dynamic range (DR) of the ADC, which in turn allows the receiver chain to be simplified and reduces system costs further. The net effect of these trends is that the ADCs in cellular base-station receivers are expected to have wider bandwidth and lower noise, but also increased power efficiency.

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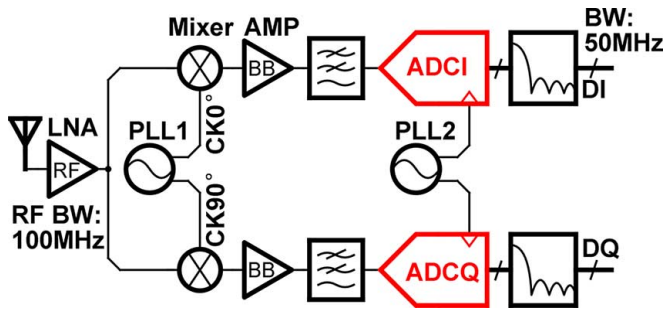

Fig. 1. A direct-conversion LTE-A cellular base-station receiver.

Fig. 1 shows a direct-conversion cellular base-station receiver for the long-term-evolution advanced (LTE-A) standard where the target radio-frequency (RF) bandwidth is 100 MHz. The RF signal is amplified by a low-noise amplifier (LNA) and then down-converted by a quadrature mixer. The baseband signals are low-pass filtered before being sampled by ADCs. Each ADC needs to provide a high DR (>80 dB) with 50 MHz bandwidth and a power consumption less than 0.3 W to allow a higher system-level integration.

An ADC architecture that can meet these specifications is a continuous-time (CT) ΔΣ ADC [1]–[11] with a feedforward (FF) loop filter [2], [3], [8], [11]. Fig. 2 illustrates a typical CT FF ΔΣ ADC where a single digital-to-analog converter (DAC) is used to feed the flash ADC output back to the input. This type of ΔΣ ADC is power-efficient because its input integrator forms the lowest-order, and hence highest-gain, feedback loop of the modulator [12]. Since high front-end gain suppresses the noise from the back-end stages, the bulk of the ADC's power budget can be allocated to the front end. This advantage is especially important for a modulator having a relatively low over-sampling-ratio (OSR). Unfortunately, the signal transfer function (STF) of a CT FF ΔΣ ADC typically exhibits peaking [12]. For example, Fig. 3 shows the STF and NTF (noise transfer function) of a third-order CT FF ΔΣ ADC with $||\mathrm{NTF}||_\infty = 6$ dB; the sampling rate is 3.2 GHz and the signal bandwidth is 53 MHz for an OSR of 30. Since the magnitude of the STF is greater than 0 dB from 200 MHz to 1.5 GHz, out-of-band signals with levels below the ADC's full-scale can saturate the ΔΣ loop. Since filtering of near-band blockers is costly, the out-of-band blocker tolerance is often compromised when a standard FF ΔΣ ADC is used. In this paper, we describe a 0-X FF multi-stage noise-shaping (MASH) ADC that addresses the peaking STF issue of a CT FF ΔΣ ADC while retaining the high power efficiency of that architecture. The paper is organized as follows: Section II describes the operation of a 0-X FF MASH ADC

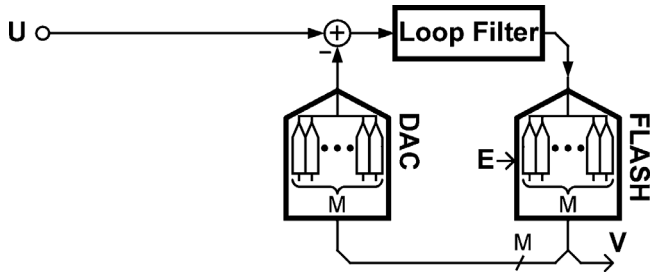

Fig. 2. A $\Delta\Sigma$ ADC with a feedforward loop filter topology.

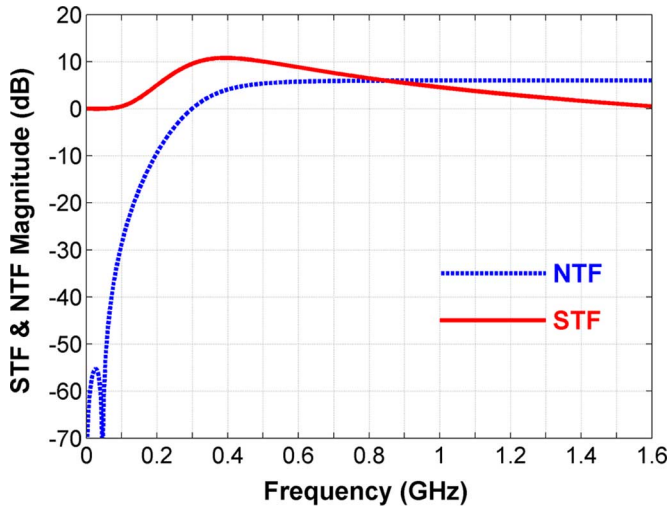

Fig. 3. Simulated STF and NTF of a third-order CT FF $\Delta\Sigma$ ADC clocked at 3.2 GHz.

in discrete-time and uses the insight gained to explain the operation of a continuous-time version. Circuit implementations of the CT 0–3 FF MASH ADC test chip in 28 nm CMOS are presented in Section III. Experimental results are discussed in Section IV followed by conclusions in Section V.

II. 0-X FF MASH ADC

The MASH architecture [13]–[17] avoids the stability problems associated with high-order noise shaping, but can be sensitive to mismatch between the digital transfer function used in the cancelation logic and the corresponding analog transfer function implemented by the analog circuitry [13], [16], [17]. By feeding the output of the second stage back into the first, the Sturdy MASH (SMASH) architecture [14] provides a solution to this problem. The 0-X MASH system [15] with a FF backend (Fig. 4) is a special case of the SMASH architecture and provides advantages of a flat STF and stable operation up to and even beyond the full-scale range of the flash front end. Compared to the structure in Fig. 2, part of the flash ADC (consisting of M0 comparators and denoted as FLASH0 in Fig. 4) has been moved to the front of the ADC. These relocated M0 comparators still drive the same M0 DAC elements as before. The remaining M1 comparators of the flash ADC after the loop filter (denoted as FLASH1) drive the remaining M1 DAC elements.

In order to understand the operation of this system, assume for simplicity that the system operates in discrete-time and that

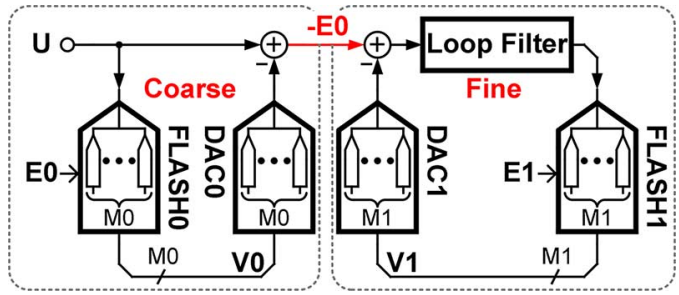

Fig. 4. A 0-X FF MASH ADC.

the flash and DAC blocks are delay-free and have LSB sizes of unity. The output of FLASH0 is

$$V0 = U + E0 \tag{1}$$

where $E0$ is the quantization noise of FLASH0. The FF $\Delta\Sigma$ ADC based back-end digitizes the residue $-E0$ into a digital output $V1$:

$$V1 = -E0 * \mathrm{STF1} + E1 * \mathrm{NTF1} \tag{2}$$

where STF1 and NTF1 are the STF and NTF of the $\Delta\Sigma$ back-end, respectively, and $E1$ is the quantization noise added by FLASH1. Since the back-end stage uses a FF topology with a single input feed-in [12]

$$\mathrm{STF1} = 1 - \mathrm{NTF1} \tag{3}$$

and thus the sum of V0 and V1 is

$$V_{\mathrm{SMASH}} = V0 + V1 = U + (E0 + E1) * \mathrm{NTF1}. \tag{4}$$

Without any further digital processing, simply adding V0 and V1 yields a unity STF for the overall ADC and the sum of the quantization noise from the front-end and the back-end are shaped by the NTF of the $\Delta\Sigma$ back-end. This property is what makes the SMASH architecture sturdy.

Note, however, that the V_{SMASH} output contains $(\mathrm{E0} + \mathrm{E1})$ shaped by the NTF whereas the output of a standard MASH system would only contain E1 shaped by the NTF. The presence of E0 in V_{SMASH} constitutes a 3 dB SQNR penalty in the performance of a SMASH system compared to that of a standard MASH system and thus it is desirable to construct the output

$$V_{\mathrm{MASH}} = z^{-n}V0 + H_d * V1 \approx z^{-n}U + H_d * \mathrm{NTF1} * E1 \tag{5}$$

where H_d is a digital transfer function chosen to approximate $z^{-n}/\mathrm{STF1}$ in the modulator's passband and n is chosen to aid the approximation. To keep the discussion simple, assume $n = 0$ so that H_d is approximately unity. Since H_d deviates from unity only by the small amount needed to cancel the residual E0 term, small errors in the correction terms within H_d only cause small amounts of shaped E0 to appear in the digital output V. For this reason, the sturdiness of the 0-X FF MASH system is similar to that of a SMASH system.

Converting the system of Fig. 4 into continuous-time form mostly follows the standard procedure for converting a discrete-time modulator prototype into continuous-time form.

Exact analysis of the resulting system is somewhat complicated and lacking in insight, so in what follows we will only provide plausibility arguments for the key properties of the CT 0-X FF architecture, namely robustness, an almost-flat STF and alias suppression. Measurements presented in the experimental results section support these arguments.

The robustness of the CT 0-X FF system can be argued by first considering with the V_{SMASH} output, which is the signal that drives the composite DAC at the input of the loop filter. As long as the system is stable, for frequencies that are in the high-gain region of the loop filter the loop will enforce

$$U - \mathrm{DAC} * V_{\mathrm{SMASH}} \approx 0. \tag{6}$$

So to the extent that the composite DAC is linear and the loop gain is large, V_{SMASH} is an accurate representation of the analog input. The same argument that explains the robustness of the MASH output from the robustness of the V_{SMASH} output in the discrete-time case likewise explains why we would expect the same to be true with a continuous-time modulator.

To see why the STF should be flat out to fairly high frequencies, observe that the back end is driven by a residue signal, $-E0$, which ought to be devoid of signal content for frequencies where the sinc response of the DAC is essentially unity. If $E0$ does not contain a signal component, then neither will V1 and thus the signal content at the output V is due solely to the signal content in V0. Since FLASH0 has a transfer function of unity, the STF of the full system is therefore unity. Note that the premise that $E0$ does not contain signal components has implications for the CT implementation. In order for E0 to be free of signal components, the transfer function through FLASH0 and DAC0 must match the transfer function from the input to the input of the back-end modulator. Aside from the obvious need to match the gain of these two paths, the delay must likewise be matched. As will be described in the implementation and measurements section, a 1.5 clock-period analog delay is introduced in the system to compensate for the FLASH0-DAC0 delay. Error in the delay affects the flatness of the STF at high frequencies.

As shown in [18] the alias suppression of a CT MASH system involves contributions from all stages. At first glance it is counter-intuitive that the 0-X system possesses significant alias suppression since FLASH0 subjects the signal to aliasing. To see why the 0-X CT MASH system is nonetheless expected to have strong alias suppression, consider an input frequency in the vicinity of F_s which produces a low-frequency aliasing product (Fig. 5). The aliasing product is applied to the loop via DAC0 and the loop forces DAC1 to produce an opposing signal such that the low-frequency content of the loop filter input is zero. Consequently, the $\mathrm{V0} + \mathrm{V1}$ sum is free of the alias term.

III. Circuit Implementation

A. CT 0–3 FF MASH ADC

Fig. 6 shows the top-level schematic of the CT 0–3 FF MASH ADC. The front-end consists of a 16-step FLASH0 ADC and a 16-element current DAC IDAC0. The input resistor R1U is sized at 25 Ω single-ended to provide a differential input impedance of 50 Ω. The difference between isig, the input

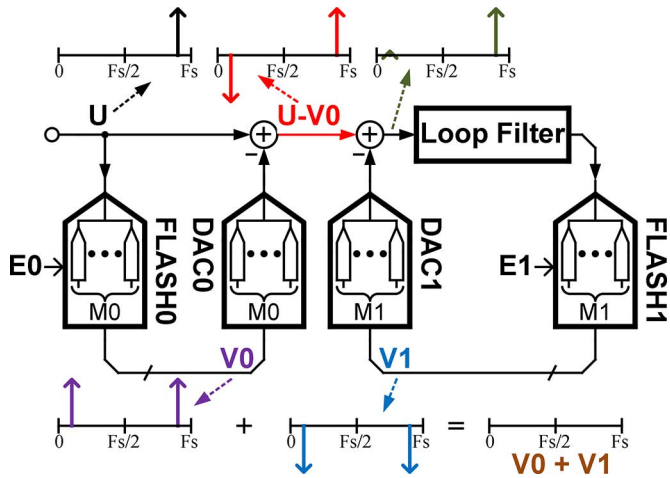

Fig. 5. A CT 0-X FF MASH ADC with near Fs input signal.

signal current flowing through R1U, and idac0, the IDAC0 output current, forms the residue current that is fed to the back-end.

The back-end is a CT third-order FF ΔΣ ADC. The loop filter contains an integrator and a resonator. With a 25 Ω input resistor R1U and an 11 pF integration capacitor C1, the input integrator provides an in-band gain of over 20 dB. This high gain is a benefit of the FF ΔΣ back-end and it ensures a high thermal noise power efficiency. A passive all-pass summer is used to sum the outputs of the three integrators. FLASH1 drives a six-element current DAC, IDAC1, which feeds back to the input. A voltage-mode DAC (VDAC) is used as the direct-feedback path to compensate for the excess loop delay associated with the chosen [1, 2] feedback timing. The VDAC shown in Fig. 6 is implemented with inverters that take the FLASH1 output and drive part of the R-C all-pass summation block.

The two current-mode DACs, IDAC0 and IDAC1, have identical LSB sizes and feed back to the same summing node. IDAC0 and IDAC1 are implemented as a single 22-elements current DAC, IDAC. A closely-placed single DAC implementation with common biasing and clock timing arrangements improves static matching and reduces timing skews between elements inside IDAC0 and IDAC1.

As mentioned in the preceding section, there is a delay associated with the FLASH0-DAC0 path. This delay is defined from the time instant when FLASH0 samples the input U to the middle of the IDAC0 output waveform. This delay is about 1.5Tck when the NRZ IDAC0 is clocked approximately one clock cycle after FLASH0 samples. Without any compensation in the R1U path, the phase difference between isig and idac0 will generate extra signal components on top of the normal quantization residue. This additional signal component is proportional to the delay and the input signal frequency. For example, for an OSR of 30 and a sinusoid input signal at the passband edge that reaches the full-scale of FLASH0, the phase difference between isig and idac0 is 2.5% of the input signal period. The maximum additional signal is only about 1.2 LSBs. However, for a signal at six times the frequency of the passband edge, the maximum additional signal grows to 7 LSBs. Since the ΔΣ back-end has a full-scale of 6 LSBs, it can tolerate at most ±3 LSBs of residue.

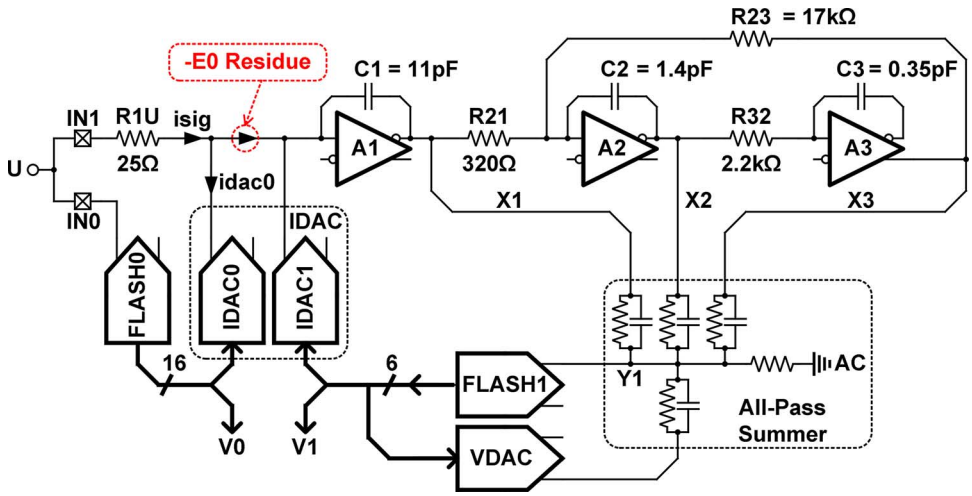

Fig. 6. Schematic of the 0–3 CT FF MASH ADC.

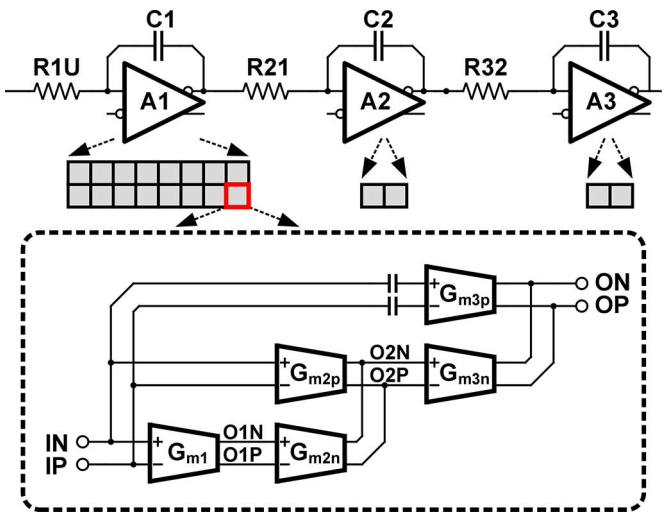

Fig. 7. Feedforward amplifiers inside the third-order loop filter.

Therefore, a matching delay is preferred along the R1U signal path; this delay can be either on-chip or off-chip. As shown in Fig. 6, the ADC has two input ports: IN0 which drives FLASH0 and IN1 which drives the input resistor R1U. This makes it possible to insert an delay element between the input signal U and the IN1 port. The ADC is designed to be clocked at 3.2 GHz and provides a signal bandwidth of 53.3 MHz with an OSR of 30. The ideal STF and the NTF of the FF $\Delta\Sigma$ back-end are illustrated in Fig. 3. The STF exhibits a peaking of about 10 dB at 300 MHz. The third-order NTF has $||\mathrm{NTF}||_\infty = 6$ dB and provides more than 50 dB of in-band noise attenuation. Benefiting from an OSR of 30 and a total of 22 IDAC output levels, the CT 0–3 MASH can tolerate an rms clock jitter of 300 fs in simulation for an 80 dB dynamic range target.

B. Feedforward Amplifiers

The third-order loop filter (Fig. 7) consists of three integrators, each of which uses an amplifier built from a base amplifier slice. This slice-based strategy saves design time but comes at the cost of increased parasitics on internal nodes which must be shorted among the slices. The number of slices used in the amplifiers is 16, 2 and 2. The minimum in-band gain for the three integrators are 20 dB, 16 dB and 11 dB, confirming that the lowest-order path has the highest gain.

Each amplifier slice is a third-order feedforward amplifier. Feedforward amplifiers are favored in CT $\Delta\Sigma$ ADCs because they can achieve high gain at high frequencies with lower power than conventional Miller-compensated multi-stage amplifiers. The fact that a feedforward amplifier does not settle in a clock period is irrelevant since the main requirement in a CT $\Delta\Sigma$ ADC is that the loop filter has high gain in the passband and is linear. The stability of a high-order feedforward amplifier is ensured by making its first-order loop dominate the frequency response near the unity gain region [6], [9], [19], [20].

Fig. 8 shows the detailed schematic of a single feedforward amplifier slice. M1 to M10 in the leftmost portion form a telescopic amplifier which acts as the input stage of the third-order signal path. The outputs of the input stage, O1P and O1N, drive M13 and M14. M11 and M12 form the input stage of the second-order signal path. M15 and M16 act as the output stage for the third-order signal path as well as the second-order signal path. M17 and M18 are driven by the input signal via ac-coupling capacitors and form the first-order signal path. The common-mode (CM) voltages are controlled by CM feedback (CMFB) amplifiers G1, G2 and G3.

CM stability is a serious issue since the CM gain could be high at high frequencies. In Fig. 8, wide-band CMFB amplifiers G2 and G3 suppress CM gain at medium frequencies and CMFB amplifier G1 reduces the CM gain of input stage at low frequencies. The second-order loop through M11–M12 and M15–16 is intentionally implemented with fully-differential pairs in order to use source degeneration to reduce CM gain. In contrast, the CM gain in the first-order loop helps stabilize the CM loop and therefore a pseudo-differential pair M17–M18 is used to maximize its CM gain. M1 and M2 act as a CM source-follower and their source node VS1 contains high-frequency CM information of the output through integration capacitors. This node is then used to drive the gate of M21 at high frequencies to further reduce the CM gain.

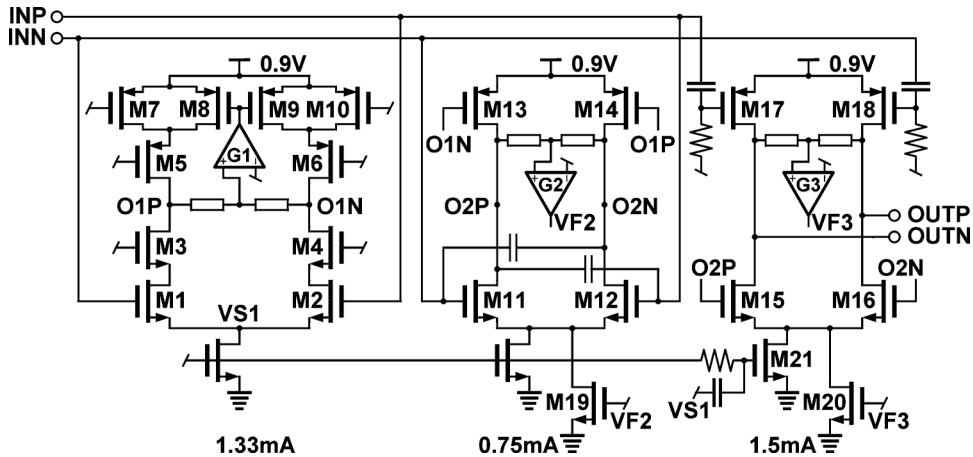

Fig. 8. Schematic of one feedforward amplifier slice.

In each amplifier slice, the core circuit consumes a dc current of 3.55 mA from the 0.9 V power supply. The three CMFB amplifiers, G1, G2 and G3, consume an additional dc current of 400 μA each. The amplifier provides an in-band gain over 30 dB and a unity gain frequency greater than 8.6 GHz with a phase margin of 53 deg. The high-bandwidth helps to reduce potential degradation on system NTF.

C. Complementary Current DAC

Fig. 9 shows the schematic of the complementary current-steering DAC cell [21]. The DAC cell consists of a p-type current source on the top, an n-type current source on the bottom and a current switching quad in the middle. The P and N current sources consist of a thick-gate MOS current source device and a core cascode device. The switching quad is implemented by core HVT devices to ensure the switches remain in saturation when they are switched with full-swing CMOS levels. Compared to a conventional differential current-steering DAC, a complementary DAC requires half of the bias current for a given differential LSB size. In addition, a complementary DAC has a thermal noise advantage because it does not have bias current sources attached to the output nodes. The LSB current in Fig. 9 is 1.125 mA and a $+1.8/-1.0$ V dual power supply is utilized to provide sufficient voltage headroom and thereby achieve low noise. The thermometer-coded data coming from the flash is sampled by an inverter-based D-Latch with a pulse clock signal CKD before driving the current switching quad. The D-Latch and the buffer are implemented with core devices and operate from the 0.9 V core supply.

Fig. 10 shows the timing diagram of the flash-DAC interface that is shared by both FLASH0-IDAC0 and FLASH1-DAC1. CKF is the sampling clock for the flash ADC and sampling occurs on the rising edge. Q is the output of the flash ADC. CKD is the pulsed clock signal that samples Q into DAC. The output of the DAC changes while the flash ADC samples and there is approximately one clock period delay from the sampling of the flash ADC to the DAC output. The impact of this delay on the loop dynamics is compensated through the use of a dedicated direct-feedback (DFB) DAC that applies the flash ADC output back to its input within one clock cycle. This timing arrangement gives about one full clock cycle for the flash-DAC signal path to settle. The CKF edge is made programmable so that the flash-DAC timing can be optimized.

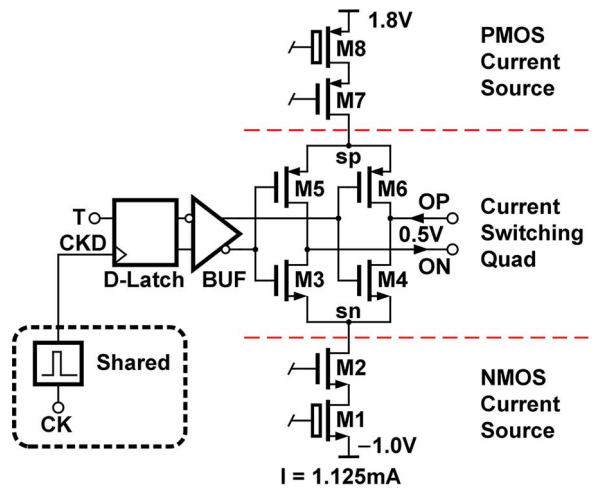

Fig. 9. Schematic of one complementary current DAC cell.

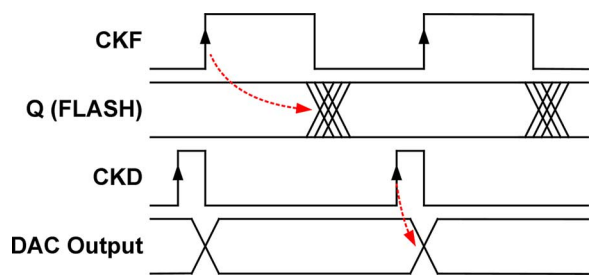

Fig. 10. Timing diagram of the FLASH-DAC interface.

D. Comparators With Enhanced-g_m

Fig. 11 shows the schematic of the comparator used in the flash ADCs. The lower portion of the schematic is the pre-amplifier and the upper portion is the regeneration core. The comparator offsets are calibrated by injecting a pair of small currents into the pre-amplifier. When CK is low, the comparator is in the tracking mode and a difference signal is established on the OUTN and OUTP nodes. When CK is high, the comparator enters the regeneration mode and the output nodes grow into

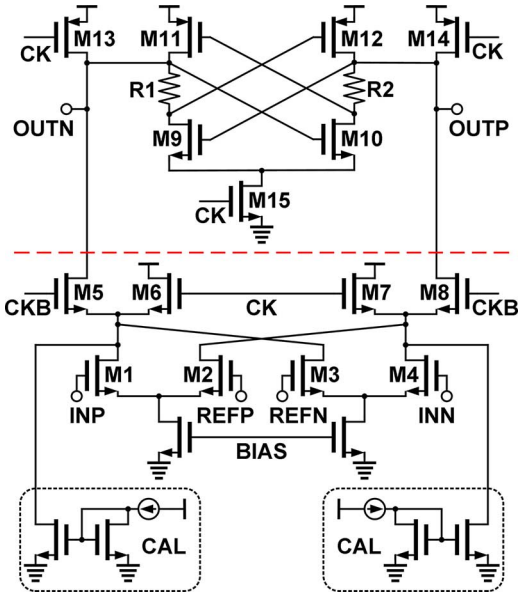

Fig. 11. Schematic of a comparator cell.

logic values. There is another RS latch driven by the regeneration core which is not shown in Fig. 11.

Two resistors, R1 and R2, are inserted into the regeneration core to enhance the g_m of M9 to M12. Without R1 and R2, M9 to M12 behave as simple cross-coupled inverters during regeneration. In this situation, the sum of V_{GS9} and V_{GS11} is VDD minus V_{DS15}, and this limits the over-drive voltages of the regeneration devices and therefore their g_m:

$$V_{GS9} + V_{GS11} = \mathrm{VDD} - V_{DS15} \approx \mathrm{VDD}. \tag{7}$$

With R1 and R2, the sum of V_{GS9} and V_{GS11} is relaxed by the IR drop across R2, V_{R2}:

$$V_{GS9} + V_{GS11} = \mathrm{VDD} + V_{R2} - V_{DS15} \approx \mathrm{VDD} + V_{R2}. \tag{8}$$

This technique increases the g_m of M9 to M11 and hence reduces the initial regeneration time constant τ. Simulations show an improvement of τ from 5.3 ps to 3.7 ps.

Fig. 12 shows the power composition of the prototype CT 0–3 FF MASH ADC. The first amplifier and the current DAC consume about 63% of the total power. This implies a high thermal noise power efficiency as these two blocks together with the passive input resistor R1U dominate the input-referred thermal noise. The ADC draws a total power of 235 mW from the $0.9/+1.8/-1.0$ V supplies.

IV. Experimental Results

The ADC is implemented in a 28 nm bulk HKMG CMOS process. The microphotograph of the test chip die is shown in Fig. 13. The ADC occupies an active chip area of about 0.9 mm^2. Fig. 14 shows the lab setup that is used to evaluate the test chip. A signal generator provides an input signal which is split into two signal paths. The upper signal path goes through some external delay, specifically 10 cm of coax, and then drives the input resistor R1U through the IN1 port. A high-pass filtered (90 MHz corner frequency) dither signal is added to the

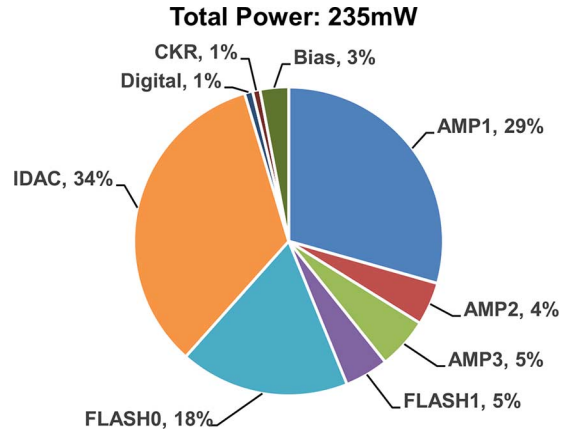

Fig. 12. Power composition of the ADC test chip.

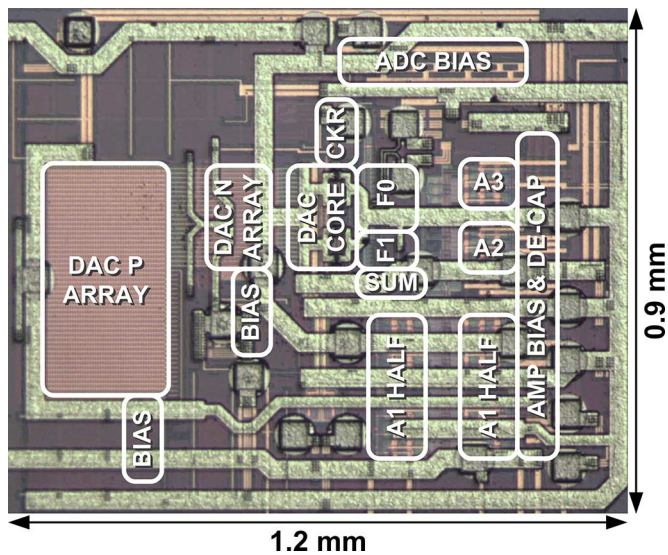

Fig. 13. Microphotograph of the test chip die in 28 nm CMOS.

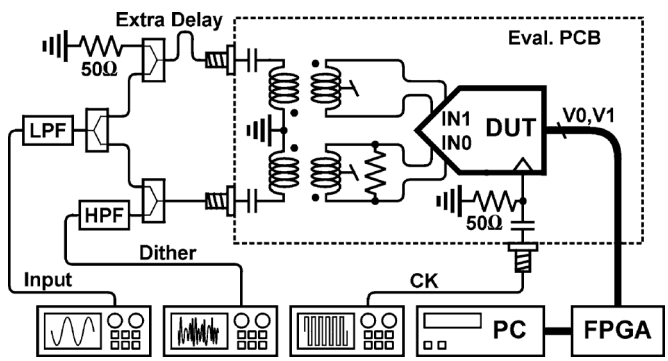

Fig. 14. Schematic of the test setup.

lower signal path and this path is used to drive the FLASH0 input through the IN0 port. The dither signal is a random sequence which yields a spectrum similar to that of a white noise that is slightly higher than the V0 noise floor. The dither signal whitens E0, which otherwise contains strong harmonic terms at specific input signal amplitudes such as 1.5 LSB. The digital outputs of the test chip, V0 and V1, are stored in an on-chip FIFO and transferred to a personal computer (PC) via a serial

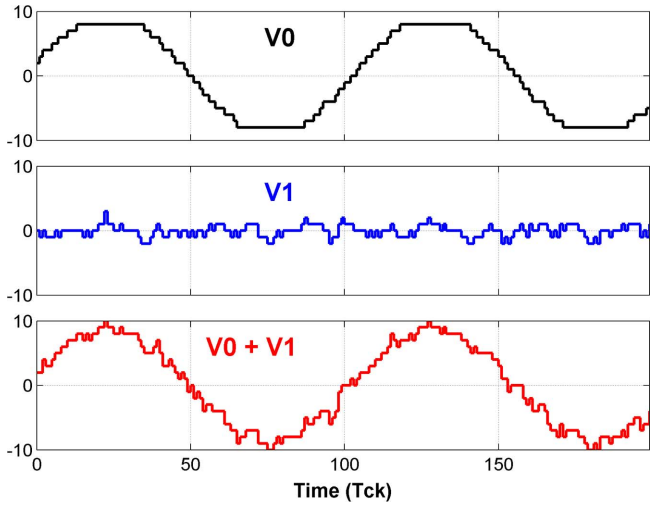

Fig. 15. Measured time domain results with a −2 dBFS input tone at 30 MHz.

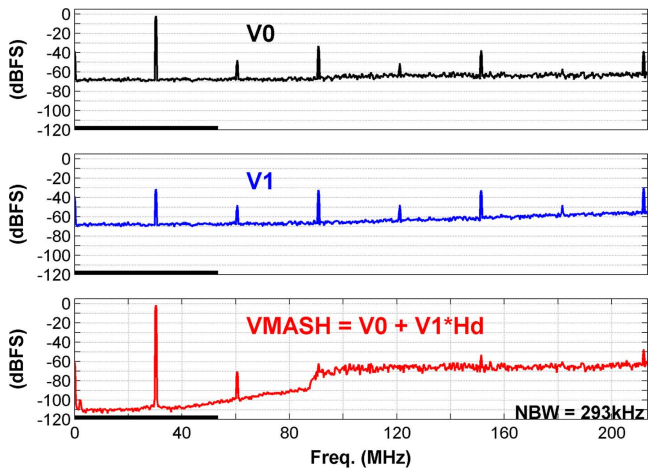

Fig. 16. Measured spectra with a −2 dBFS input tone at 30 MHz.

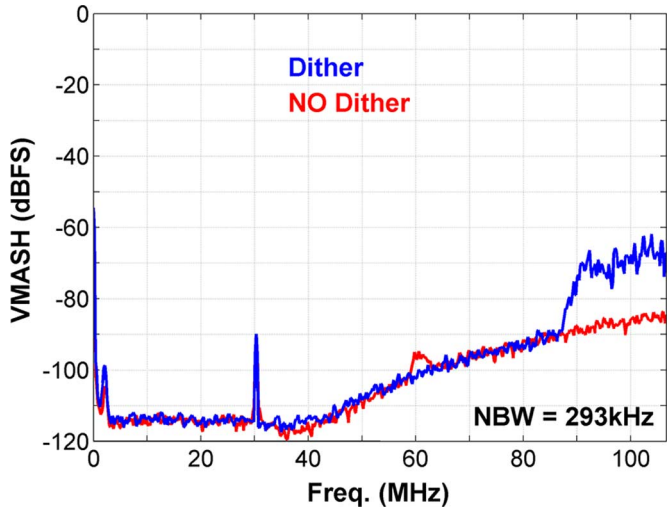

Fig. 17. Measured spectra with a −90 dBFS input tone at 30 MHz.

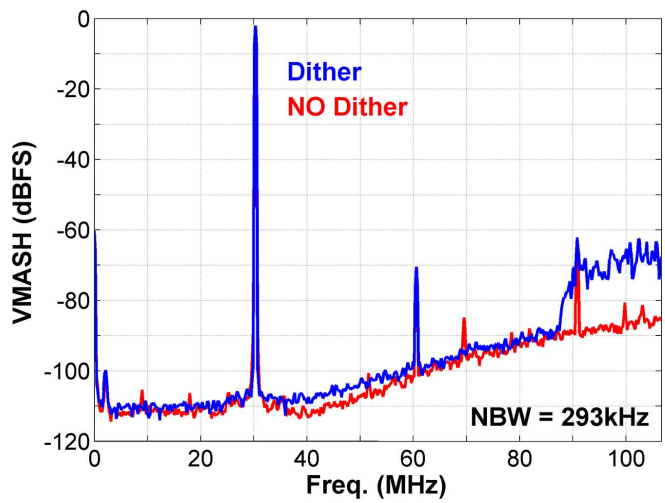

Fig. 18. Measured spectra with a −2 dBFS input tone at 30 MHz.

peripheral interface (SPI) for post processing. Both FLASH0 and FLASH1 are calibrated during power-up using off-chip engines implemented on the PC.

Fig. 15 shows the measured time domain digital waveforms with a −2 dBFS input signal at 30 MHz. The FS of the ADC is defined as the total strength of IDAC which includes the 16 elements from IDAC0 and the 6 elements from IDAC1. As a result, a −2 dBFS input signal already exceeds the FS of FLASH0 and thus V0 (top) exhibits clipping at ±8. V1 (middle) is the output of the third-order ΔΣ back-end. V1 mostly toggles between ±1 with occasional ±2 hits. Since the outer V1 levels are ±3, the back-end is comfortably below overload. The bottom waveform is the sum of V0 and V1, which clearly tracks the input without clipping. Fig. 16 shows the spectra of the ADC with the same input. The thick line on the x-axis marks the [0, 53] MHz signal band. V0 (top) and V1 (middle) have similar noise spectra within the signal band. VMASH (bottom) shows the combined output, using MASH cancellation. The fact that the noise floor of VMASH is 40 dB lower than that of V0 and V1 indicates that at least 99% of E0 is cancelled in the signal band.

Fig. 17 shows the output spectra of the ADC with a −90 dBFS input signal, with and without a dither signal being added to the FLASH0 input. It can be observed that the noise floors of both cases are very close to each other within the signal band. The NSD is flat up to 40 MHz at −170 dBFS/Hz. In both results, there is a tone at 2 MHz. This tone is 5 dB higher in the dithered case and causes the total in-band noise to be 1 dB higher than the non-dithered case. This tone is large even if the dither system is merely powered up (not connected to the test setup) and is believed to be due to the switching power supply used within the dither generator. Figs. 18 and 19 show the zoomed-in spectra with a −2 dBFS input signal at 30 MHz and 15 MHz, respectively. Fig. 20 shows the spectrum with two −8 dBFS input tones around 30 MHz.

Fig. 21 shows the signal-to-noise ratio (SNR) and the signal-to-noise-and-distortion (SNDR) of the ADC versus the input amplitude. The SNR is measured with a 30 MHz input signal while the SNDR is measured with a 15 MHz input signal. Dither is added in both cases. The peak SNR is 83.1 dB and the DR is 88 dB. The peak SNDR, which includes the second-order and third-order harmonics, is 70 dB. The distortion performance of the ADC test chip is believed to be limited by the timing skew and switching error of the IDAC. Fig. 22

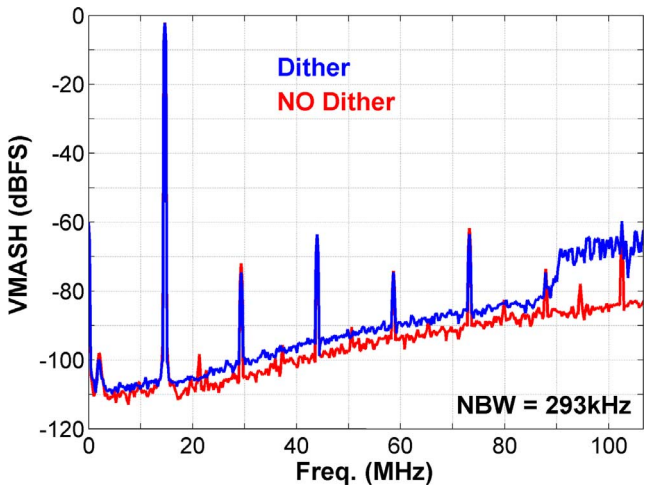

Fig. 19. Measured spectra with a −2 dBFS input tone at 15 MHz.

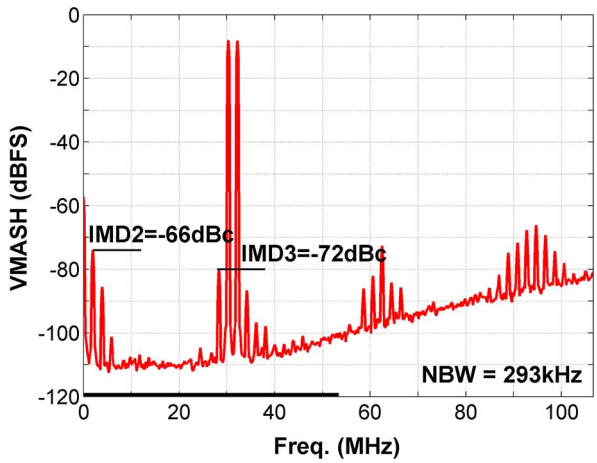

Fig. 20. Measured spectra with two −8 dBFS input tones near 30 MHz.

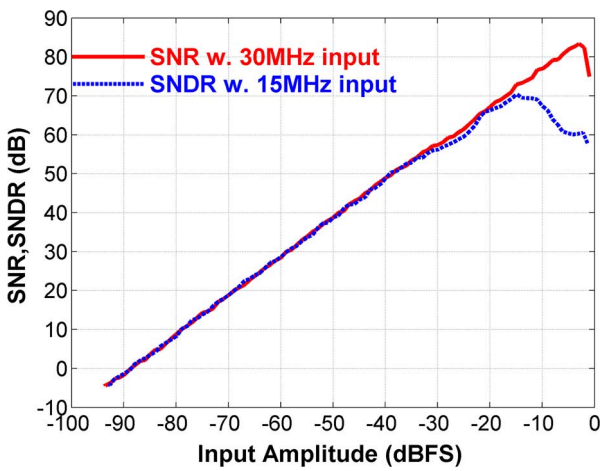

Fig. 21. Measured SNR (SNDR) vs. input amplitude with dither in MASH configuration.

shows the SNR versus input amplitude in MASH and SMASH operation with a 30 MHz input signal. MASH mode shows a 2 dB SNR improvement over SMASH mode, indicating that quantization noise is a significant noise source. Fig. 23 shows

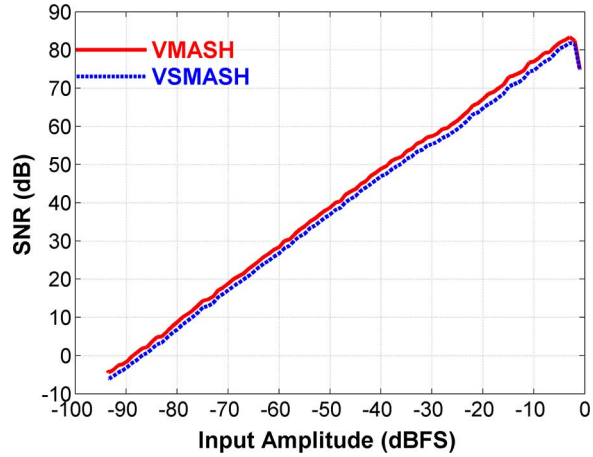

Fig. 22. Measured SNR vs. amplitude of a 30 MHz input with dither.

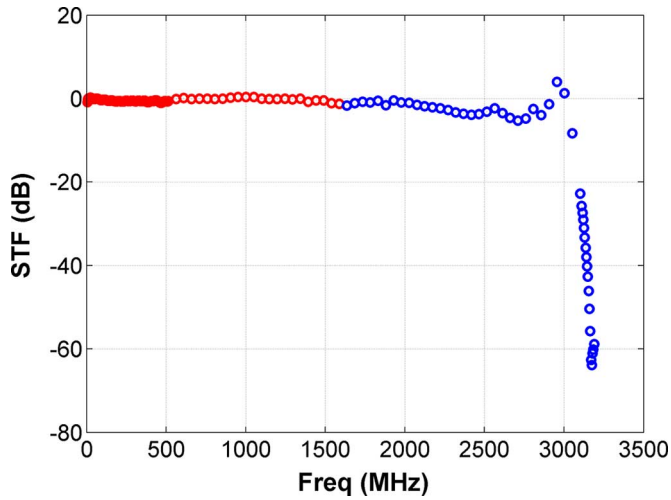

Fig. 23. Measured STF of the 0–3 MASH ADC in MASH configuration; alias STF measured above 1.6 GHz).

the system STF in MASH mode and the alias suppression is about 60 dB. This implies less than 0.1% mismatch between the actual STF1 implemented in the analog domain and the digital equivalent used to compute H_d. Table I compares this work with some recently published CT $\Delta\Sigma$ ADCs and Fig. 24 compares this work with ADCs published at IEEE ISSCC. The vertical axis is the thermal noise figure-of-merit (FOM) defined underneath Table I. This work achieves a FOM of 171.6 dB over 53 MHz bandwidth and has a 10 dB advantage over previous works offering similar bandwidth.

V. Conclusion

In this work, we have shown that a CT 0-X FF MASH ADC has power efficiency and anti-aliasing properties similar to a single-loop CT FF $\Delta\Sigma$ ADC while exhibiting a flat STF. The 0-X FF MASH ADC is very robust in terms of noise cancellation thanks to the unity NTF and STF of the flash front-end and the very stable STF of the CT FF $\Delta\Sigma$ back-end. A test chip implemented in a 28 nm CMOS process achieves a thermal-noise FOM of 171.6 dB over 53 MHz signal bandwidth.

TABLE I
COMPARISON OF THIS WORK WITH RECENT CT $\Delta\Sigma$ ADCS

Publication	This Work		[3]	[4]	[5]	[6]	[7]	[8]	[10]
			JSSC 11	*ISSCC 12*	*ISSCC 12*	*JSSC 12*	*ISSCC 12*	*ISSCC 13*	*ISSCC 14*
CMOS L_{MIN}	**28nm**		45nm	90nm	90nm	65nm	45nm	28nm	130nm
Active Area	**0.9mm^2**		0.9mm^2	0.23mm^2	0.12mm^2	5.5mm^2	0.49mm^2	0.08mm^2	0.33mm^2
Supply Voltages	**0.9/1.8/–1.0V**		1.1/1.8V	1.2V	1.2V	1.2/±2.5V	1.4/1.8V	N.A.	1.2V
Sampling Rate	**3.2GHz**		4GHz	0.5GHz	3.6GHz	4.0GHz	6.0GHz	0.64GHz	0.26GHz
Power (P)	**235mW**		256mW	8.5mW	15mW	750mW	20mW	3.9mW	5mW
OSR	**35**	**30**	16	10	50	26.6	50	17.7	64
Bandwidth (BW)	**45MHz**	**53.3MHz**	125MHz	25MHz	36MHz	75MHz	60MHz	18MHz	2MHz
*Dynamic Range (DR)**	**90dB**	**88dB**	70dB	72dB	80dB*	79dB	62dB	78.1dB	82dB
SNRmax	**84.6dB**	**83.1dB**	65.5dB	69.1dB	76.4dB	N.A.	61.5dB	N.A.	80.5dB
SNDRmax	**72.6dB**	**71.4dB**	65dB	67.5dB	70.9dB	N.A.	60.6dB	73.6dB	74.4dB
$ENOB = (DR\text{-}1.76)/6.02$	**14.7**	**14.3**	11.3	11.7	13	12.5	10	12.7	13.3
$FOM1 = DR + 10\log_{10}(BW/P)$	**172.9dB**	**171.6dB**	156.9dB	166.7dB	173.8dB	158.2dB	156.8dB	174.7dB	168dB
$FOM2 = P/(2BW \cdot 2^{ENOB})$	**96.7fJ**	**107fJ**	400fJ	52.2fJ	25.5fJ	686fJ	162.8fJ	16.5fJ	124fJ

* *DR* is measured as the input signal range corresponding to 0dB SNR and peak SNR-1dB

***ENOB, FOM1 and FOM2 are calculated based on DR*

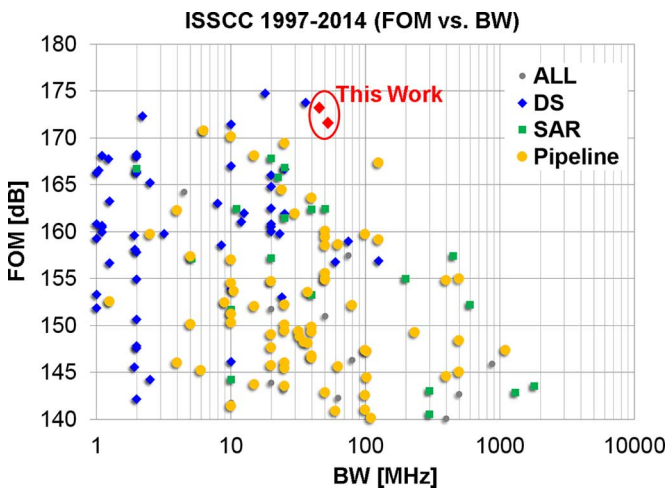

Fig. 24. Comparison of this work with ADCs published at ISSCC 1997–2004.

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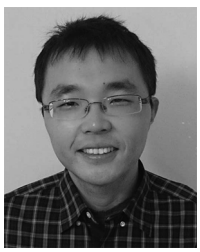

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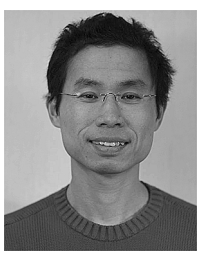

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