# A Differential-Capacitance Read Scheme for FeRAMs

Yadollah Eslami*, Ali Sheikholeslami*,
Shoichi Masui†, Toru Endo†, and Shoichiro Kawashima†
* Department of Electrical and Computer Engineering, University of Toronto, Canada
* Email: {eslamiy, ali} @eecg.utoronto.ca
† Fujitsu Laboratories Limited, Atsugi, Japan, Email: {masui, tendo, poosan}@flab.fujitsu.co.jp

**Abstract**

A differential-capacitance read scheme keeps the plateline voltage constant at ground and begins sensing the stored data immediately after a wordline is raised, hence eliminating the time spent in conventional read schemes in raising the highly capacitive plateline and in charge sharing of the bitlines with the ferroelectric capacitors. The proposed read scheme is used in a 256x128-bit testchip that features both 2T-2C and 1T-1C cells in 0.35μm technology. The read scheme achieves a 40% reduction in access time.

## Introduction

FeRAMs are replacing EEPROMS and Flash memories in applications that require fast and low-power write access. FeRAMs, however, are still behind EEPROM and Flash memories in terms of read access time. Current FeRAMs achieve a read access time of about 80ns, which is at least twice as large as those of EEPROM and Flash memories. This paper proposes a novel read scheme that reduces the read access time by 40%. The proposed read scheme explores the difference in capacitance (instead of the difference in polarization charge) of a ferroelectric capacitor in its two polarization states. We present this read scheme for both 2T-2C and 1T-1C architectures and compare their read access times with those of the conventional read scheme [1], the Non-Driven Plateline (NDP) read scheme [2], and the BitLine Driven (BLD) read scheme [3].

Fig. 1 shows the hysteresis loop of a ferroelectric capacitor along with the definition of polarization states for stored "1" and stored "0", their corresponding capacitances ($C_1$ and $C_0$), and their respective charges ($Q_1$ and $Q_0$). Present read schemes differentiate between $Q_1$ and $Q_0$ to determine the stored data. In the conventional 2T-2C read scheme, shown in Fig. 2, the plateline (PL) is raised from ground to $V_{DD}$ to transfer $Q_1$ and $Q_0$ onto the bitlines (BL and $\overline{BL}$) for sensing. This scheme spends a major portion of the access time on raising a highly capacitive PL. The NDP scheme eliminates this portion of the timing by keeping the PL constant at $V_{DD}/2$ at all times, but maintains charge sharing of the ferroelectric capacitors with the bitline capacitors. Similarly, the BLD read scheme maintains charge sharing between the ferroelectric capacitor and a bitline

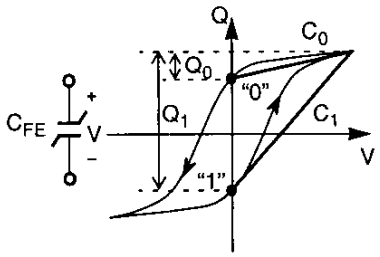


Fig. 1 Ferroelectric Capacitor Hysteresis loop defining "0", "1", $Q_0$, $Q_1$, $C_0$, and $C_1$

precharged to $V_{DD}$. In contrast, our proposed read scheme eliminates both the PL driving used in the conventional read scheme and the charge sharing required in NDP and BLD read schemes, hence substantially reducing the read access time.

## Differential-Capacitance Read Scheme (DCRS)

### A. 2T-2C Architecture

Fig. 3 illustrates the differential capacitance read scheme for a 2T-2C cell architecture. This scheme precharges both BL and $\overline{BL}$ to ground, keeps the PL at ground, raises the WL and, immediately after, turns on the sense amplifier. At the outset of sensing, the PMOS transistors of the sense amplifier act as

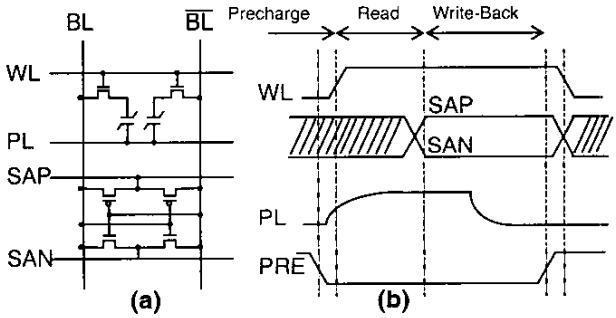


Fig. 2 (a) 2T-2C architecture, (b) conventional read timing

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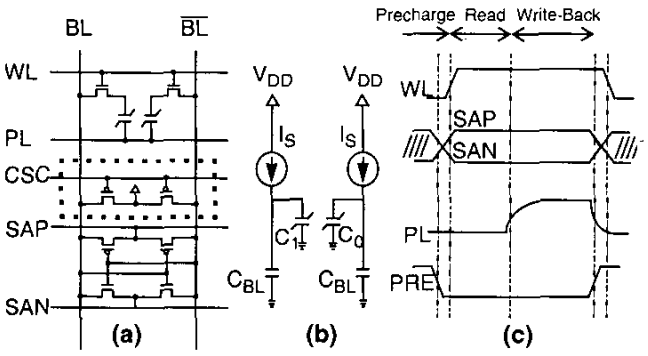


Fig. 3 (a) 2T-2C architecture with added PMOS transistors, (b) equivalent circuit for DCRS, (c) DCRS read timing

current sources, charging up the bitlines. The role of the PMOS transistors controlled by CSC in Fig. 3(a) is described later in this paper. The bitline accessing a ferroelectric capacitor storing a "0" (BL0) will experience a voltage slew rate higher than a bitline accessing a ferroelectric capacitor storing a "1" (BL1). This is due to the fact that the ferroelectric capacitor storing a "0" has a lower capacitance, as seen in Fig. 1. An equivalent circuit for the scheme is shown in Fig. 3(b). Assuming the initial saturation current of a PMOS transistor charging up the bitlines is $I_S$, the voltage slew rates of BL0 and BL1 are given by the following equations:

$$SR_0 = I_S/C_{BL0} \text{ and } SR_1 = I_S/C_{BL1} \quad (1)$$

Fig. 4 shows how the voltages $V_{BL0}$ and $V_{BL1}$ rise according to (1) if the positive feedback effect of the sense amplifier is not present. It can be seen that more than 350mV of voltage difference is developed on BL0 and BL1 to be sensed by the sense amplifier in less than 6ns. By activating SAN and SAP, as $V_{BL0}$ and $V_{BL1}$ rise above the threshold voltages of the NMOS transistors ($V_{Tn}$), the sense amplifier positive feedback effect drives BL0 and BL1 to $V_{DD}$ and ground, respectively. The simulation results of this reading scheme is shown in Fig. 5.

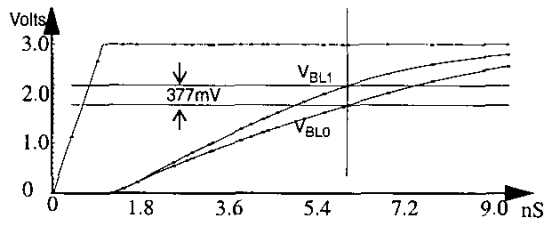


Fig. 4 $V_{BL1}$ and $V_{BL0}$ for 2T-2C architecture

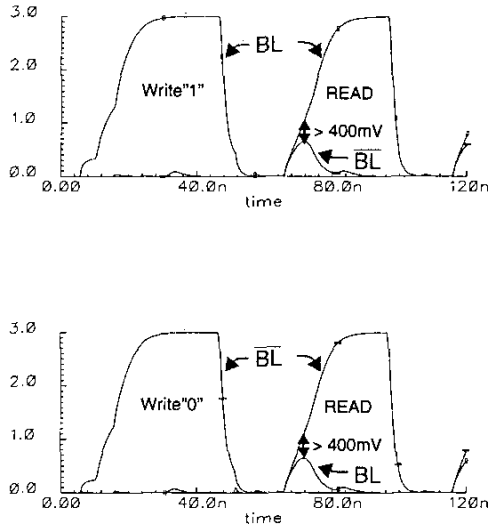


Fig. 5 Simulation results for 2T-2C FeRAM architecture: DCRS read scheme

This scheme functions properly despite potential mismatches in the threshold voltages or the saturation currents of the PMOS transistors, as long as $SR_0 > SR_1$. Assuming a $\Delta I_S$ mismatch, the requirement for correct data sensing is this scheme is:

$$\frac{C_{BL0}}{C_{BL1}} < \left(1 - \frac{\Delta I_S}{2I_S}\right) \Big/ \left(1 + \frac{\Delta I_S}{2I_S}\right) \quad (2)$$

For example, to compensate for a 10% mismatch in $I_S$, $C_{BL0}/C_{BL1}$ must be smaller than 0.9. Based on our simulation results, this condition holds for up to 512 cells per bitline using $1\mu m^2$ cell ferroelectric capacitors.

### B. *1T-1C Architecture*

In a 1T-1C folded-bitline architecture, odd bitlines (BLO) serve as reference bitlines for the even bitlines (BLE) and vice versa. In order for a reference bitline (RBL) to have a slew rate half way between $SR_0$ and $SR_1$, RBL must have a capacitance constrained by the following equation:

$$\frac{1}{2 \times C_{RBL}} = \frac{1}{C_{BL0}} + \frac{1}{C_{BL1}} \quad (3)$$

To reduce the implementation complexity of RBL, we have approximated (3) with the following constraint:

$$C_{RBL} = C_{BL} + \frac{C_0 + C_1}{2} \quad (4)$$

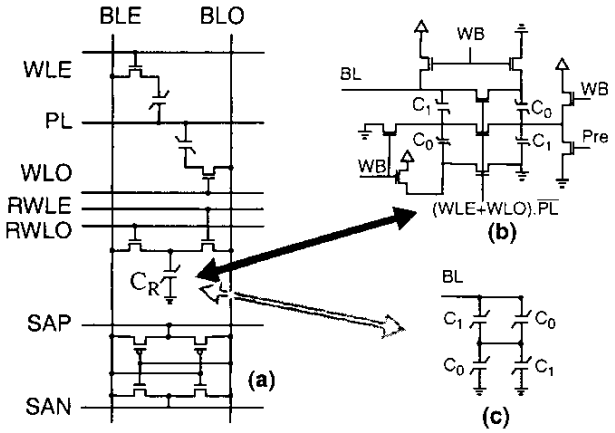


Fig. 6 (a) Folded bitline structure for 1T-1C architecture, (b)reference capacitance implementation, (c) equivalent circuit when accessed

As shown in Fig. 6(a), $C_{RBL}$ is implemented by connecting $C_R = (C_1 + C_0)/2$ to the BL. To produce $C_R$, we have used a combination of four ferroelectric capacitors, all identical in size to the cell capacitor, as shown in Fig. 6(b).

Including $C_{RBL}$, as the reference capacitor in the simulations, the voltages on BL0, BL1 and BLR, without the sense amplifier feedback, change according to the waveforms shown in Fig. 7. It can be seen that at least 170 mV of voltage difference is available to the sense amplifier after 6ns. The simulated waveforms of this architecture with sense amplifier activated, are presented in Fig. 8.

Another way of producing $C_R$ is to use a single ferroelectric capacitor in non-switching mode and larger than the cell capacitor. We have implemented both approaches in our testchip for comparison purposes.

## Simulation Results

The simulation results for 2T-2C and 1T-1C architectures are shown in Fig. 5 and Fig. 8, respectively. The circuits are simulated for four different bitline sizes: 8, 128, 256, and 512 rows per bitline. In all cases the circuit detects the stored bit correctly. The access time for a 512x128 array is 50ns, using a Pulse-based Parallel-Element Macromodel [4] in conjunction with HSPICE.

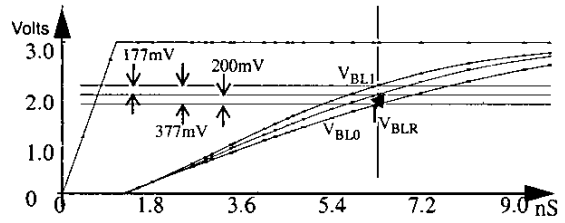


Fig. 7 $V_{BL1}$, $V_{BL0}$, and $V_{BLR}$ in 1T-1C architecture

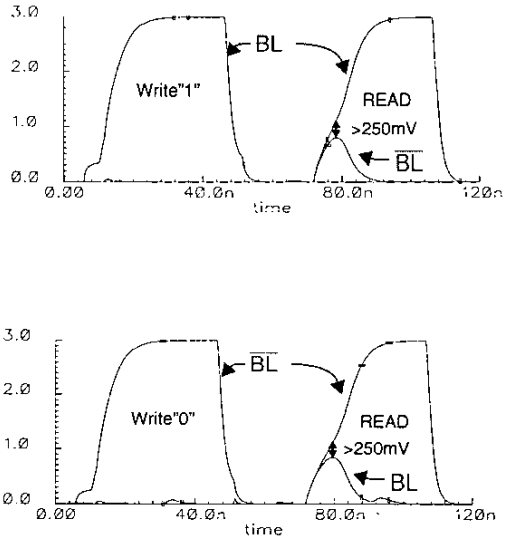


Fig. 8 Simulation results for 1T-1C FeRAM architecture: DCRS read scheme

Fig. 9, compares the access time of this scheme with the other three schemes using identical simulation models for all four schemes. Omitting the PL drive and charge sharing steps, the proposed scheme reduces the access time by more than 40% compared to the conventional scheme, and more than 20% compared to NDP and BLD schemes.

## Testchip Considerations

The proposed read scheme, as presented so far, ignores the PMOS transistors controlled by CSC in Fig. 3(a). We have included these two transistors to allow a slightly modified timing of the read scheme in the testchip. By activating CSC

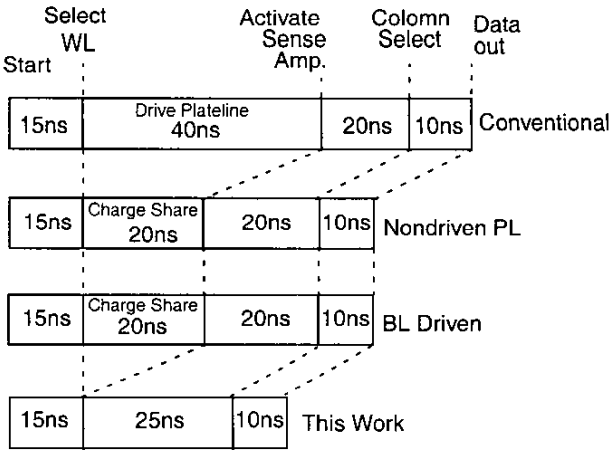


Fig. 9 read access-times among various read schemes

prior to activating SAP and SAN, we allow the voltage on the bitlines to develop without the positive feedback effect of the sense amplifier PMOS transistors. This would reduce the possible effect of $\Delta V_{Tp}$ on the sensing. Similarly, by allowing to delay activation of SAN in relation to SAP, we allow the voltage difference on the bitlines to rise above the threshold voltages of the NMOS transistors, hence avoiding the effect of $\Delta V_{Tn}$ at an early stage of the sensing. We have achieved this by including a programmable delay element in the testchip.

## Conclusions

A differential-capacitance read scheme eliminates both the time required for driving the PL, as in the conventional read scheme, and the time required for charge sharing of the ferroelectric capacitor and the BL capacitor, as in the NDP and the BLD read schemes. By relying on the capacitive imbalance of the ferroelectric capacitor in States "1" and "0", the DCRS achieves a 40% read access-time improvement over the conventional scheme. The DCRS is implemented in a 256x128 bit testchip in a 0.35um technology. The testchip's layout is shown in Fig. 10. The measurement results of this testchip will be presented during the symposium.

## Acknowledgments

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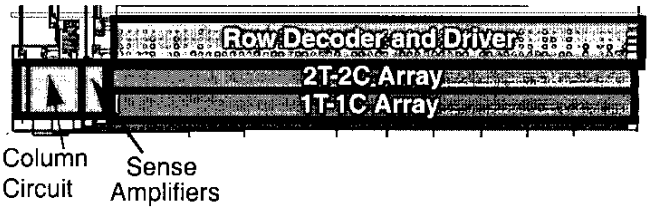


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|---|---|
| Technology | 0.35 μm, 3 Metal |
| Ferroelectric Capacitor | Planar |
| Power Supply | 3.0 V |
| Memory Array (2T-2C) | 8kBits |
| Memory Array (1T-1C) | 8kBits |
| Sense Amplifier | CCSA Sensing |
| | Bitline Monitor |

Fig. 10 Testchip layout and specifications