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A Voltage-Dependent Switching-Time (VDST) Model of Ferroelectric Capacitors for Low-Voltage FeRAM Circuits

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Abstract

The time required to switch a ferroelectric capacitor from one binary state to the other is strongly related to the magnitude of the applied voltage, especially at voltages well below the power supply. This paper presents a Verilog-A model that accurately predicts the voltage-dependent switching dynamics of various FeRAM technologies. Spectre simulations of low-voltage FeRAM circuits implemented in a 0.35μm CMOS/PZT testchip are in full agreement with our measurement results.

Introduction

As circuit innovations in ferroelectric random-access memories (FeRAM) target low voltages and low access-times, the switching time of ferroelectric (FE) capacitors becomes all the more critical. Traditionally, circuit simulation models have neglected the switching time [1] [2] in favor of the RC time constant of the circuits involved. This assumption is still valid for voltages near the power supply (V_{dd}), where switching completes in the sub-nanosecond time regime, but becomes invalid for smaller applied voltages (less than $V_{dd}/2$) where switching can take up to one second.

To demonstrate the effect of voltage-dependent switching, we apply a 1.8V step to the plateline (PL) of a 1T-1C cell that uses V_{dd} = 3V, as shown in Fig. 1. The bitline (BL) voltage rises to its final value in less than 50ns if a zero-switching time is assumed, but remains substantially below the final value if the switching time is taken into account.

Previous attempts at incorporating the switching time either target a particular technology [3] or target FE capacitors as stand-alone elements [4]. This paper presents a dynamic model that is adaptable to various technologies and applicable to FE capacitors in any circuit topology. We demonstrate the model's accuracy through the comparison of simulations and measurements obtained from a 0.35μm CMOS/PZT FeRAM testchip and successfully apply the model to the analysis of low-voltage FeRAM circuits.

Voltage-Dependent Switching Time (VDST) Model

The VDST model is composed of a dynamic and static portion as depicted in Fig. 2. The dynamic portion models the switching delay of the FE capacitor by delaying V_{in} through a set of time constants (τ_i) to produce a corresponding set of V_{eff_i}. A weighted sum of V_{eff_i} is then applied to the static portion [1] to determine the charge, $Q(V_{eff})$. Mathematically,

$$V_{eff}(t) = \mu_1 V_{eff_1}(t) + \mu_2 V_{eff_2}(t) + \ldots + \mu_n V_{eff_n}(t) \quad (1)$$

where $\mu_1 + \mu_2 + \ldots + \mu_n = 1$, and each V_{eff_i} is governed by

$$dV_{eff_i}(t)/dt = (V_{in}(t) - V_{eff_i}(t)) / \tau_i \quad (2)$$

$$\tau_i (V_{pulse_i}) = \tau_\infty exp((V_{o_i}/V_{pulse_i})^m) \quad (3)$$

$$V_{pulse_i} (V_{eff_i}) = V_{in} - c_i - k_i (V_{eff_i} - c_i)^x \quad (4)$$

where $i = \{1, 2, \ldots, n\}$, $k_i = (V_{in} - c_i)^{-(x-1)}$ and c_i is V_{eff_i} at the last change of V_{in} such that the boundary conditions $V_{pulse_i}(c_i) = V_{in} - c_i$ and $V_{pulse_i}(V_{in}) = 0$ are met. Eq. (1)-(4) are implemented in Verilog-A and integrated into Spectre [5]. The implementation using Verilog-A achieves the same accuracy as an implementation using circuit elements, but with a 20-fold reduction in simulation time.

Fig. 3 shows a depiction of (3) and (4) and the role of x in characterizing the switching behavior of various FeRAM technologies. V_{eff_i} is initially at $V_{eff_i}@t_0$, which corresponds to a small switching time constant ($\tau_i@t_0$). As V_{eff_i} increases with time and approaches V_{in}, τ_i dynamically increases to mimic the switching delay of the FE capacitor.

The parameter x controls the rate of increase of τ_i and can be calibrated to match the switching dynamics of a particular technology. For x = 1, $V_{pulse_i} = V_{in} - V_{eff_i}$, and the model degenerates to [3]. As V_{eff_i} approaches V_{in}, V_{pulse_i} decreases linearly, thus increasing τ_i exponentially. This results in a slow switching characteristic consistent with a 0.5μm PZT technology. For x = 2, V_{pulse_i} decreases at a slower rate, thus holding τ_i at a smaller value. This results in a faster switching characteristic resembling that of a 0.35μm PZT technology.

To verify this analysis, the circuit in Fig. 4(a) is used to generate the switching curves (switching charge vs. time) of a FE capacitor for applied voltage steps of 1.5V, 2V, and 3V [4]. P1 defines the initial state of the capacitor, P2 reverses the polarization for various t_2 and v_2, and P3 measures the result. Fig. 4(b) and 4(c) show the measured switching curves of a 0.5μm (V_{dd}=5V) and 0.35μm (V_{dd}=3V) PZT FE capacitor [6] and simulated results for x = 1 and x = 2, respectively. The results are in close agreement and confirm the VDST model's adaptability to various FeRAM technologies.

Fig. 5 shows the 0.35μm CMOS/PZT FeRAM testchip layout [7] used for simulation and measurement purposes, which utilizes a supply voltage of 3V. To exaggerate the effect of voltage-dependent switching, we reduce V_{dd} to 1.8V and observe the simulated BL voltage development with time for a conventional step-sensing read scheme [8]. Fig. 6 shows the expected gradual increase of V_{BL0} and V_{BL1} due to the large switching time of the FE capacitor at small applied voltages, a trend consistent with our measurement results.

Application to Low-Voltage FeRAM Circuits

FeRAM circuits experience smaller applied voltages due to supply-voltage scaling and voltage division in circuits containing FE capacitors in series. An example of the latter is the reference generation circuit proposed in [7] that uses four FE capacitors to provide an equivalent capacitance of $C_{ref} = (C_0 + C_1)/2$, where C_0 and C_1 are the nominal capacitances of a stored '0' and stored '1', respectively, as shown in Fig. 7. Due to the series combination of FE capacitors, each capacitor experiences only half of the reference BL voltage (V_{BLref}) instead of the full voltage, causing these capacitors to switch slower than the cell capacitor. Simulations using a model that neglects the switching time predict correct functionality of the reference capacitor [7]. The measurement results, however, indicate that the testchip always outputs a '1' regardless of the stored data. Simulations using the VDST model, calibrated to the 0.35μm discrete PZT sample in Fig. 4(c), successfully reproduce this behavior by showing that V_{BLref} is larger than both V_{BL0} and V_{BL1}, as shown in Fig. 8.

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Conclusion

The VDST model successfully incorporates the voltage-dependent switching of FE capacitors for circuit simulations of low-voltage FeRAM circuits. The model accurately predicts measurement results obtained from a 0.35μm CMOS/PZT FeRAM testchip.

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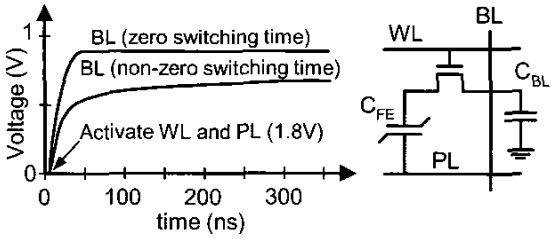

Fig. 1: Assuming zero switching time (i.e. solely relying on the RC time constant of the circuit) erroneously reveals a fast-rising bitline.

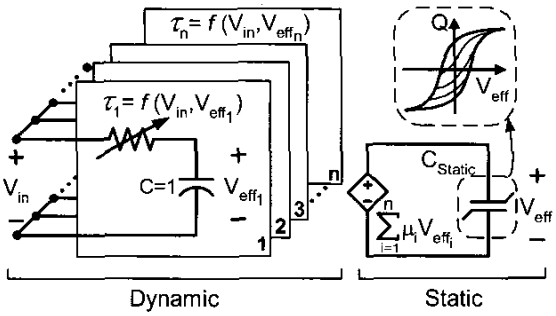

Fig. 2: V_{in} is delayed through a set of time constants (τ_i) to model the switching delay of the FE capacitor. The resulting effective voltage (V_{eff}) is applied to a static model to determine the charge.

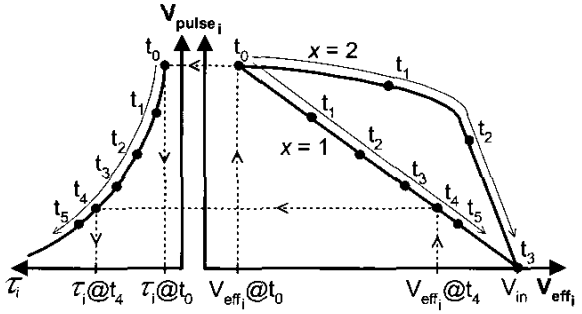

Fig. 3: Switching time (τ_i) dynamically increases with time as V_{eff_i} approaches V_{in}. The rate of increase is controlled by x in (4).

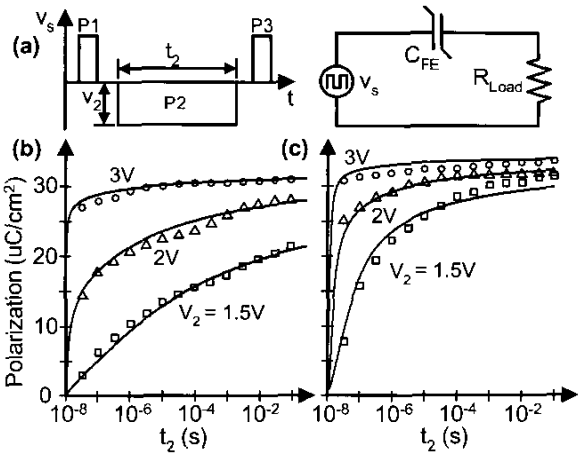

Fig. 4: **(a)** P1 sets the initial state of the capacitor, P2 switches the polarization, and P3 measures the result. Measured data points [6] vs. simulated switching curves for **(b)** 0.5μm and **(c)** 0.35μm PZT capacitors.

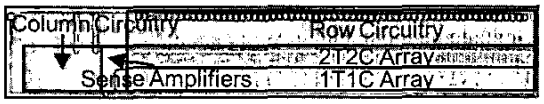

Fig. 5: Differential Capacitance Read Scheme (DCRS) testchip [7] is used to collect measurement data.

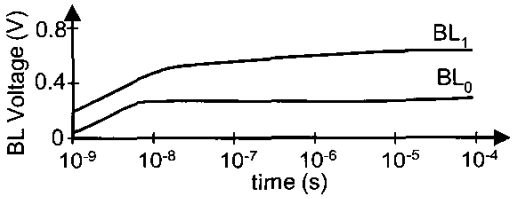

Fig. 6: Simulated bitline voltages for a step-sensing read scheme [8] at a reduced supply voltage of 1.8V.

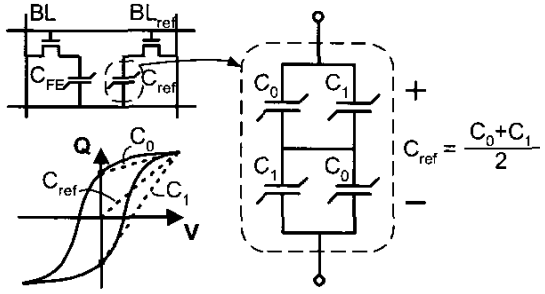

Fig. 7: Reference capacitor for DCRS (C_{ref}) [7] is theoretically the average of C_0 and C_1. However, the actual C_{ref} is much smaller. See Fig. 8.

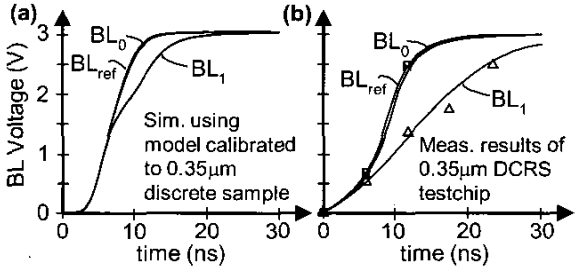

Fig. 8: **(a)** Simulation and **(b)** measurement results of DCRS circuit of Fig. 7. The VDST model accurately predicts that V_{BLref} is larger than both V_{BL0} and V_{BL1}.