On-Chip Measurement of Data Jitter with Sub-Picosecond Accuracy for 10Gb/s Multilane CDRs

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Abstract

On-chip jitter measurement is demonstrated in a 10Gb/s CDR by correlating the phase detector outputs of two adjacent CDR lanes. The RMS jitter of the received data and an estimate of the jitter's power spectral density are then extracted without using an external reference clock. Circuits implemented in 65nm CMOS measure random jitter ranging from 0.85ps to 1.89ps in PRBS31 data with no more than 100fs error compared to an 80GS/s real-time oscilloscope. Sinusoidal jitter of 0.89ps to 5.1ps is measured with a worst-case error of 580fS compared to the oscilloscope.

Introduction

As data rates increase, jitter is becoming the main bottleneck in maintaining the low bit error rate (BER) required in serial links. On-chip measurement of data jitter can help reduce its adverse effects through adaptation of circuit parameters. Previous works on jitter measurement have mostly focused on clock jitter [1-2] where either a clean reference clock is provided or only period-jitter is measured. In [3], data jitter is measured by feeding the data along with a reference clock to a time-to-voltage converter and sampling its output to produce an analog signal for measurement off-chip. This technique sends a relatively small analog voltage off-chip or would require an on-chip high-speed, high-resolution ADC to produce a digital output. In this work, we digitally correlate the outputs of two bang-bang phase detectors (PD) to estimate the autocorrelation function of the jitter. This function is available on-chip for use by other circuit blocks, or can be sent off-chip for diagnostic purposes. Post-processing of the chip output provides not only the RMS value of the jitter but also its estimated power spectral density (PSD).

Proposed Jitter Measurement System

As shown in Fig. 1, if input signal (*DATA*) with jitter Φ_{DATA} feeds two PDs driven by two clocks (*CK1* and *CK2*) with uncorrelated jitter Φ_{CK1} and Φ_{CK2}, multiplying and averaging the PD outputs using a low-pass filter (LPF) cancels uncorrelated jitter components Φ_{CK1} and Φ_{CK2} and yields an estimate of Φ_{DATA} as $E[K_{P1}\cdot K_{P2}\cdot(\Phi_{DATA})^2]$ where K_{P1} and K_{P2} are PD gains and $E[\cdot]$ denotes the expected value. In this scheme, neither clock is used as an ideal reference. Therefore the jitter of the clocks does not need to be much lower than that of the signal being tested. We apply this technique to a multilane CDR where *CK1* and *CK2* are provided by CDRs.

As shown in Fig. 2, *CK1* and *CK2* are generated by two adjacent VCO-based CDRs locked to *DATA*. In a multilane system, *CK2* could be provided by an adjacent lane, configured in a diagnostic mode using a MUX, or a global diagnostic PLL, amortizing the cost of circuits across many lanes. The CDR loops high-pass filter Φ_{DATA} to produce Φ'_{DATA1} and Φ'_{DATA2}, which enter the two PDs. Assuming Φ_{VCO1} and Φ_{VCO2} represent the uncorrelated jitter generated by the CDR circuits, the PD correlation signal *B* (see Fig. 2) then contains a high-pass filtered version of Φ_{DATA}. Since in-band jitter is suppressed by the CDR loops, this scheme characterizes the out-of-band data jitter responsible for performance degradation in the CDR. To calculate the jitter from the PD correlation, the PD gains must be known.

We use bang-bang PDs whose outputs can be correlated and averaged digitally. It is well known that the gain of a bang-bang PD is linearly proportional to the slope of the cumulative distribution function (CDF) of $\Delta\Phi$ [4], where $\Delta\Phi=(\Phi_{DATA} - \Phi_{CK})$. Accordingly, to measure the PD gain we measure the CDF of $\Delta\Phi$ using an on-chip edge-monitor with adjustable phase to sweep the edge of the data eye, counting the ratio of early to late transitions at each phase. Since we only require the slope of the CDF, the edge monitor's time resolution only needs to be fine enough to measure a few points on the CDF. This contrasts with previous work, where the measurement resolution is determined by the time resolution of circuits such as time-to-digital converters.

Dividing the correlation of the PD outputs by the product of the PD gains ($K_{P1}\cdot K_{P2}$) and taking the square root yields the estimated RMS jitter in seconds. We estimate the autocorrelation function $R[n]=E[\Phi'_{DATA1}(k)\cdot\Phi'_{DATA2}(k-n)]$ of the jitter by adjusting the time shift between the outputs of PD1 and PD2 with a FIFO. The resulting function $R[n]$ is the inverse Fourier Transform of the estimated PSD of the jitter.

System Implementation

The test chip, implemented in Fujitsu 65nm CMOS, contains two half-rate 10Gb/s CDRs and a digital core as shown in Fig. 3. In the CDR, a 5-bit CML phase interpolator (PI_E in Fig. 3) interpolates between adjacent phases of the 5GHz 4-phase VCO to adjust the phase of the edge-monitor clock *CK_EDGE* with a resolution of 25ps/31=0.8ps. Two additional PI blocks PI_I and PI_Q, having a fixed interpolation ratio of 0.5, are included to match the clock delays and ensure that *CK_EDGE* and *CK_Q* are nominally aligned. The PD outputs are demultiplexed and sent to a digital correlation block. A 17-bit edge counter counts up to 262k total data transitions while a second accumulator counts edges where the two PD outputs are equal. When the edge counter reaches its limit, both counters stop and the output of the second accumulator gives the correlation between PDs.

Experimental Results

To validate the circuits, the CDRs are driven with PRBS31 data from a Centellax TG1B1 BERT clocked by a TG1C1 clock synthesizer. Sinusoidal jitter (SJ) is injected by the clock synthesizer's internal circuits. Random jitter (RJ) is injected by a NoiseCOM noise generator driving the external jitter input of the clock synthesizer. The jitter modulation bandwidth of the synthesizer in this configuration was limited to between 20MHz and 100MHz due to equipment limits.

Fig. 4 shows a measured CDF of $\Delta\Phi$ (generated by sweeping the edge-monitor phase) and its corresponding probability density function (PDF). The PD gain is calculated from the slope of the CDF in its linear region.

Fig. 5(a) shows jitter measurement results when SJ is injected into the data at 100MHz. The upper plot compares the jitter as estimated by on-chip measurement against the

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jitter measured by an Agilent DSAX91604A 80GS/s (16GHz bandwidth) real-time scope. The scope has a 150fs jitter measurement noise floor and uses software-based clock recovery to measure jitter on the data. The estimated jitter differs from the real-time scope's measurement by no more than 580fs over the range of injected jitter amplitudes. Fig. 5(b) shows results for RJ injection, where the estimated jitter is within 100fs of the real-time scope's measurement. Even though the CDR recovered clock jitter exceeds 2ps RMS in all of these measurements, jitter as low as 0.85ps in the input data can still be estimated with this approach.

The upper plot in Fig. 6(a) shows the measured jitter autocorrelation *R[n]* when 0.05UI$_{PP}$ SJ is injected at 100MHz. Duty cycle distortion (DCD) in the half-rate CDR causes oscillations to occur between odd and even values of *R[n]*. These oscillations disappear in the lower plot, which only shows odd samples of *R[n]*. The SJ at 100MHz is visible in both plots as a sinusoid. Fig. 6(b) compares the FFT of *R[n]* to the jitter spectrum measured by the scope. Both show a large spur at 100MHz, demonstrating that individual SJ components can be identified with this approach.

Fig. 7 shows the CDR's jitter tolerance for 10Gb/s PRBS31 data. High frequency jitter tolerance is 0.19UI$_{PP}$. Each CDR consumes 62mW and occupies 0.084mm^2. The edge-monitor blocks add 11% measured power and 9% area overhead. The digital core containing test registers and additional circuits not described here occupies 0.106mm^2 and consumes 31mW. The DMUXes occupy a total of 0.013mm^2 and consume 7mW.

Acknowledgements

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References

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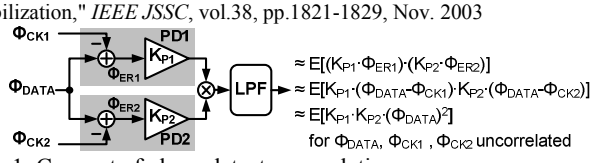
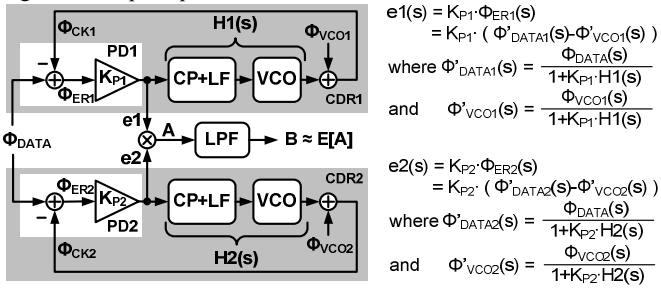


Fig. 1. Concept of phase detector correlation



If VCO jitter Φ_{VCO1} and Φ_{VCO2} are uncorrelated,

$$B \approx E[A] = E[e1(t)\cdot e2(t)] \approx K_{P1}\cdot K_{P2}\cdot E[\Phi'_{DATA1}(t)\cdot\Phi'_{DATA2}(t)]$$

If $S'_{DATA}(f)$ is the PSD of Φ_{DATA}, then B has PSD

$$S'_B(f) = \frac{S'_{DATA}(f)}{(1+K_{P1}\cdot H1(f))^*(1+K_{P2}\cdot H2(f))}$$

Fig. 2. Correlation using two CDRs

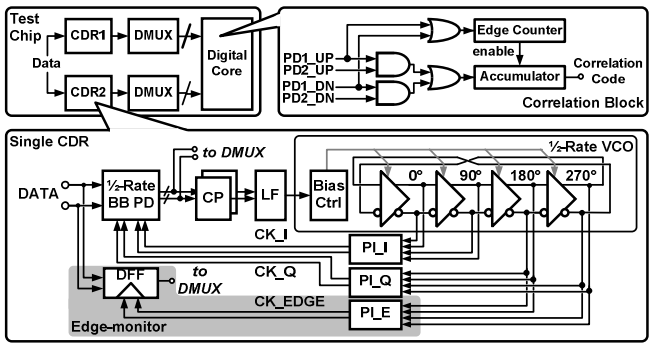


Fig. 3. Implementation of a single CDR

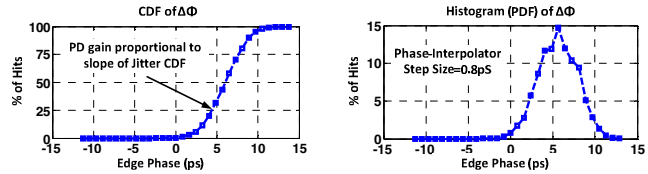
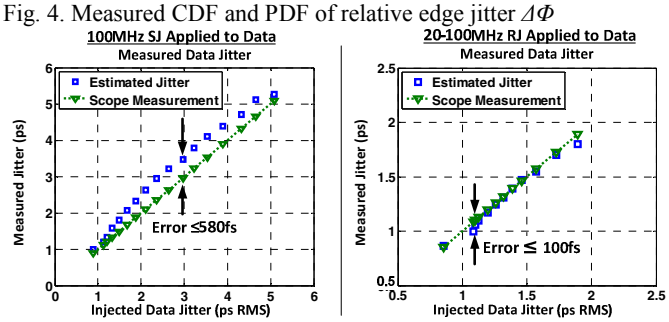
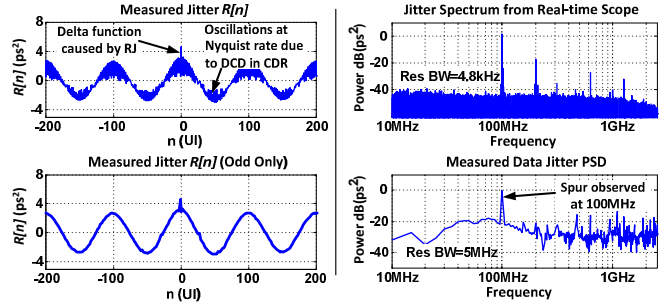


Fig. 4. Measured CDF and PDF of relative edge jitter $\Delta\Phi$



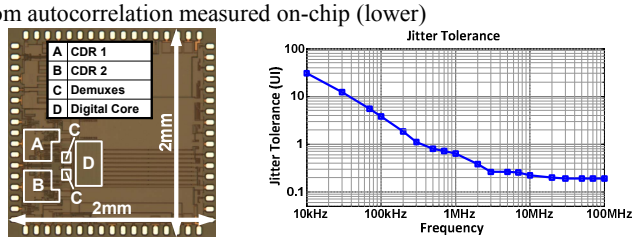
(a) (b)

Fig. 5. (a) RMS jitter measured on-chip vs. real-time scope for 100MHz SJ and (b) 20-100MHz RJ



(a) (b)

Fig. 6. (a) Jitter autocorrelation function measured on-chip with 100MHz SJ on data with all samples (upper), and odd samples only (lower) (b) Jitter spectrum measured by scope (upper) vs. jitter PSD from autocorrelation measured on-chip (lower)



(a) (b)

Fig. 7. (a) Die photo (b) Jitter tolerance for 10Gb/s PRBS31 data

Table 1. Comparison to Previous Work

Reference	Input Signal	Ext. Ref. Clock	Output Signal	Frequency /Data Rate	Information Available		Measurement Error
					Histogram	Spectrum	
[1]	Clock	Yes	Digital	1 GHz	Yes	No	101fs*
[2]	Clock	No	Digital	3.36 GHz	Yes	No	350-700fs*
[3]	PRBS	Yes	Analog	2.5 Gb/s	Yes	Yes	1.56ps†
This work	PRBS	No	Digital	10 Gb/s	Yes	Yes	≤ 580fs

* Jitter only reported for one case

† Standard deviation of measurement error