

Errata

for

Fundamentals of Digital Logic with VHDL Design

Page 59

In problem 2.31, the equation for function f_1 should be

$$f_1 \leq (x_1 \text{ AND } x_3) \text{ OR } (\text{NOT } x_1 \text{ AND NOT } x_3) \text{ OR } (x_2 \text{ AND } x_4) \text{ OR} \\ (\text{NOT } x_2 \text{ AND NOT } x_4) ;$$

Page 179

The sixth sentence from the top of the page, which reads:

“These inversions are at inputs x_1 , x_5 and x_6 , and at the output f .”

should be changed to read

“These inversions are at inputs x_1 , x_5 , x_6 , and x_7 and at the output f .”

Page 248

Near the middle of the page, the sentence that reads:

“Similarly, the expressions for G_2 , P_2 , G_3 and P_3 are”

should be changed to read

“Similarly, the expressions for c_{24} and c_{32} are”

Page 304

Near the end of Section 6.5 the equation

$$AltB = \overline{AeqB} + AltB$$

should be

$$AltB = \overline{AeqB} + AgtB$$

Page 375

In Figure 7.41 the statement:

WAIT UNTIL Clock'EVENT AND Clock = '1' ;

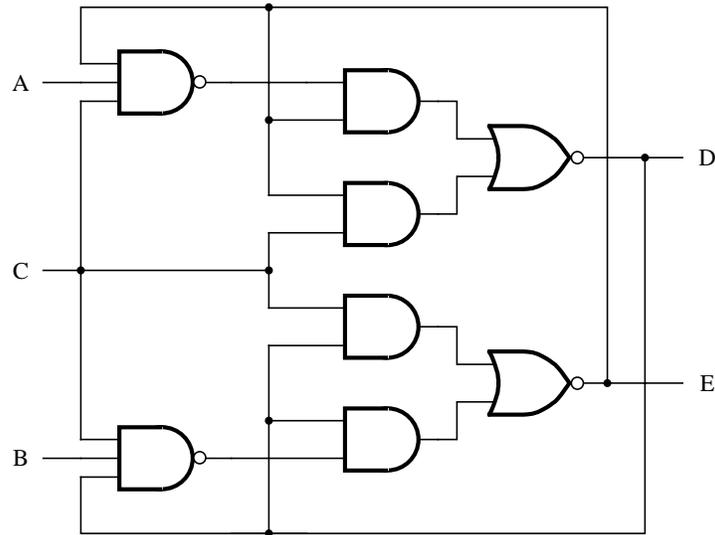
should be changed to remove the Clock'EVENT condition:

```
WAIT UNTIL Clock = '1' ;
```

Please note that this problem is also present in the sample VHDL code on the CD-ROM provided with the book.

Page 420

Figure P7.2 in problem 7.9 is incorrect. The intended figure is:



Page 521

In Figure 9.4, the caption for part (a) should be “Circuit”, not “State diagram”.

Page 530

The 14th sentence from the bottom of the page states

“; since we are assuming that y_2 changes first,”

This should be changed to

“assuming that y_1 changes first in the transition from $y_2y_1 = 01$,”

Page 535

There is an error in Example 9.6:

The circuit in Figure 9.22 is hazardous. If inputs change from $r_1=r_2=0$ to $r_1=r_2=1$, then depending on gate delays there may be glitches on g_1 and g_2 . The solution is to use a mutual exclusion device (ME) on the input side, which sequences the inputs such that the arbiter circuit never sees both inputs equal to 1.

Page 553

In the middle of the page, the sentence

“Of course, this diagram can also be derived directly from Figure 9.39.”

Should be deleted. Figure 9.41 is needed for the derivation, because it shows that D and H are not compatible.

Page 604

In Figure 10.12, the caption should refer to the “control circuit”, not the “datapath circuit”.

Page 622

In Figure 10.28, fourth line from the bottom, the statement:

$$\text{Sum} \leq \text{R} \& \text{R0} + (\text{NOT B} + 1);$$

should be changed to remove the parentheses:

$$\text{Sum} \leq \text{R} \& \text{R0} + \text{NOT B} + 1;$$

The parentheses cause the VHDL compiler to generate a wrong circuit, because the number of bits in each of the two operands of the addition are not the same. An alternative way to fix this problem is to explicitly sign-extend the *B* operand:

$$\text{Sum} \leq \text{R} \& \text{R0} + ((\text{B}(\text{N}-1) \& \text{NOT B}) + 1);$$

Please note that this problem is also present in the sample VHDL code on the CD-ROM provided with the book.