Errata

for the CD-ROM in

Fundamentals of Digital Logic with VHDL Design

1. On the CD-ROM in the VHDL source code file named:
   CDROM-drive:\VHDLcode\Chap7\Figure7.41\flipflop.vhd the statement:

   WAIT UNTIL Clock'EVENT AND Clock = '1' ;

   should be changed to remove the Clock'EVENT condition:

   WAIT UNTIL Clock = '1' ;

2. In the VHDL source code file named:
   CDROM-drive:\VHDLcode\Chap10\Figure10.28\divider.vhd the fourth statement from the bottom is:

   Sum <= R & R0 + (NOT B +1) ;

   This statement should be changed to remove the parentheses:

   Sum <= R & R0 + NOT B +1 ;

   The parentheses cause the VHDL compiler to generate a wrong circuit, because the number of bits in each of the two operands of the addition are not the same. An alternative way to fix this problem is to explicitly sign-extend the B operand:

   Sum <= R & R0 + ((B(N−1) & NOT B) +1) ;