

Highlights:

- Research focus on CAD algorithms and tools. Focus on CAD for FPGAs.
- Strong commitment to teaching. Eight years of experience as a teaching assistant at the University of Toronto. For four of these years I held a position of the Head Teaching Assistant.
- Extensive experience in Software design and HDL digital design for FPGAs.
- Received Best TA Award for Spring 2008 term.

Education:

Ph.D., Computer Engineering, University of Toronto, 2008

Focus: Physical Synthesis for FPGAs, Logic Synthesis, Power Optimization

Dissertation: Physical Synthesis Toolkit for Area and Power Optimization on FPGAs

M.A.Sc., Computer Engineering, University of Toronto, 2004

Focus: Physical Synthesis for commercial FPGAs, Synthesis of logic into carry chains

B.A.Sc., Computer Engineering, University of Toronto, Ontario, Canada, 2001

Work Experience:

Employer: Department of Electrical and Computer Engineering, University of Toronto

Period: 1999-2008

Position: Teaching Assistant and Head Teaching Assistant

Courses: Computer Fundamentals, Digital Systems, Computer Hardware, Digital and Computer Systems, Computer Organization, VLSI Systems.

Employer: Altera Corporation

Period: May 2000 - September 2000 and May 2001 - September 2001

Position: Software Engineer (Summer Internship)

Focus: Computer Aided Design Tool Development

Employer: University of Toronto

Period: May 1999 - September 1999

Position: Undergraduate Summer Research Position

Focus: Software Development for PalmOS.

Teaching Experience:

1. I held a position of a teaching assistant for eight years. Four of those years I was a Head TA. My responsibilities included management and training of over 20 teaching assistants for Digital Systems and Computer Hardware courses.
2. I gave lectures and lead laboratory exercises for digital design courses.
3. I received a consistent average rating of 6.9/7 from students for the quality of assistance and

teaching. I won an Teaching Assistant award in 2008 for excellence in teaching.

4. Completed a Teaching in Higher Education course offered by the School of Graduate Studies at the University of Toronto.

Research Skills:

Extensive knowledge of CAD algorithms and CAD tools. Focus on FPGAs.

Extensive knowledge of synthesis algorithms and digital design.

Research Interests:

I am interested in Computer Aided Design algorithms and tools, specifically in the area of logic and physical synthesis. Implementation of arithmetic circuits and efficient synthesis algorithms are a primary focus. I am also interested in projects of cross-disciplinary nature focusing on the speedup of computation using digital circuits.

Journal Publications under review (abstracts and/or full text available upon request):

1. T.S. Czajkowski and S.D. Brown, "Functionally Linear Decomposition and Synthesis of Logic Circuits and its Application to FPGAs," Submitted to the Transactions on Computer Aided Design.

Publications (accepted or in print):

1. T.S. Czajkowski and S.D. Brown, [Fast Toggle Rate Computation for FPGA Circuits](#), Accepted for publication at the 18th International Conference on Field-Programmable Logic and Applications, Heidelberg, Germany, September 8-10, 2008.
2. T.S. Czajkowski and S.D. Brown, [Functionally Linear Decomposition and Synthesis of Logic Circuits for FPGAs](#), IEEE Proceedings of the 45th Design Automation Conference, Anaheim, California, USA, June 8-13, 2008, pp. 18-23.
3. T.S. Czajkowski and S.D. Brown, [Using Negative Edge Triggered FFs to Reduce Glitching Power in FPGA Circuits](#), IEEE Proceedings of the 44th Design Automation Conference, San Diego, California, June 4-8, 2007, pp. 324-329.
4. T.S. Czajkowski and J. Rose, [A Synthesis Oriented Omniscient Manual Editor](#), Proceedings of the 12th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, Monterey, California, February 22-24, 2004, pp. 89-98.

Non-refereed reports:

1. T.S. Czajkowski, B. Fort and I. Kuon, "Quake Server Parallelization," Parallel Programming Course Project Report, December 2004.
2. F. Plavec and T. S. Czajkowski, "Distributed File Replication System based on FreePastry DHT," Distributed Systems Course Project Report, December 2004.
3. T. S. Czajkowski, C. J. Comis, and M. Kawokgy, "Fast Fourier Transform Implementation for High

Large Projects:

- 2004-Present - Physical Synthesis Toolkit software package. The package is designed to allow research and development of algorithms targeting commercial FPGA devices. It currently interfaces with Altera Quartus II software and support Altera Stratix and Stratix II devices. Approximate code size is 85000 lines of code.
- Spring 2004 - 16K point Fast Fourier Transform design for Altera Stratix device. The project was designed for use in the context of astrophysics research. The approximate size of the design was 11000 logic elements, 48 DSP blocks and 750Kbits of memory.
- Spring 2002 - Behavioural Synthesis project to convert a C description of a program into a hardware description language such as VHDL. The project was successfully completed, with source code in the range of 10000 lines of code.

References:

Available upon request.