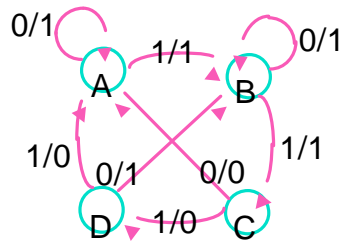
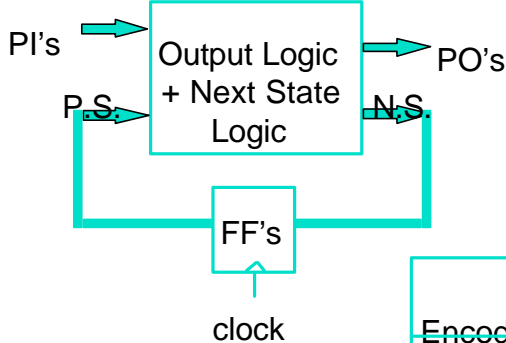


Outline

- Sequential Machines
- Initializing Sequences
- Iterative Logic Array Model
- State Justification
- Logic Values
- Simulation-Based Test Generation

Sequential Machines

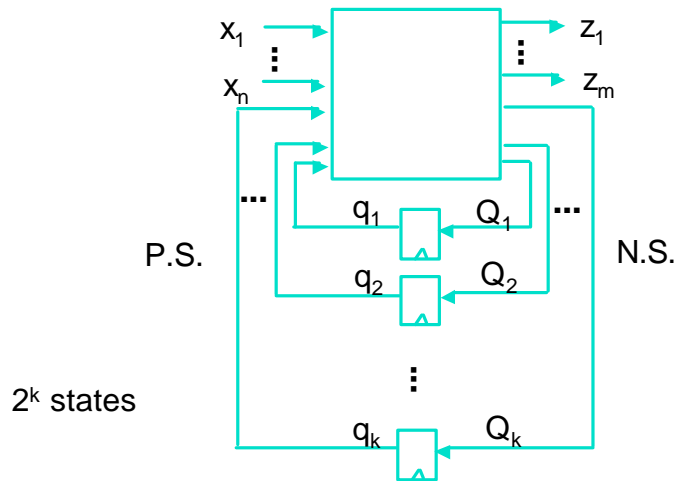
- Most commonly used form: **Mealy Machine**



Note that clock is **implicit**

Encoding	P.S.	N.S., output	
		$x_1=0$	$x_1=1$
00	A	A, 1	B, 1
01	B	B, 1	C, 1
10	C	A, 0	D, 0
11	D	B, 1	A, 0

Sequential Machines



State Table

P.S. $q_1 q_2 \dots q_k$	N.S., output				2^n columns	
	00...00	00...01	00...10	00...11	...	11...11
					...	

- Number of entries in state table = 2^{n+k}
- For $k=100$ FF's and $n=30$ inputs, 2^{130}

Initializing Sequences

- In combinational circuits, there are no unknowns (or any unknowns can be removed).
- In sequential circuits, initial state is often unknown.
- An initializing sequence, synchronizing sequence, reset sequence puts the machine in a known state.
- Except for clock or pulse generators, all practical machines must have a reset sequence.
 - ◆ **Unfortunately, the reset sequence is most often unavailable to an ATG system.**
 - ◆ **A reset sequence can get corrupted by the presence of a fault.**

Fault Detection

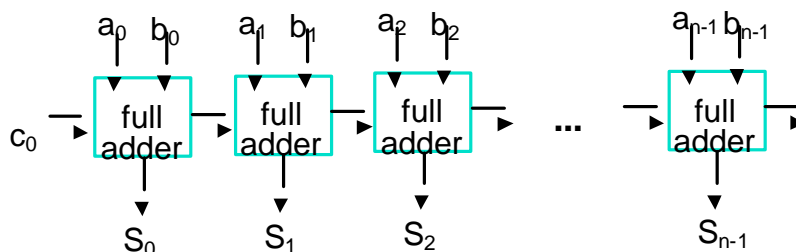
- A test sequence T **strongly detects** a fault f if the output responses (sequences) $R(q, T)$ and $R_f(q, T)$ are different for all initial states q .
- A test sequence T **detects** a fault f if the output responses to vector $t_i \in T$ are different for all initial states q , i.e., sequences $R(q, T)$ and $R_f(q, T)$ differ in a specific position i for any starting state q .

Sequential Redundancy

- A sequential redundancy is not defined in terms of fault detection.
 - ◆ A fault f is **redundant** in machine M if the good machine M and the faulty machine M_f are equivalent; i.e., prove that M and M_f are equivalent for every initial state.
- A fault in a sequential circuit is **combinationally redundant** if a test cannot be generated even if PPI's are considered to be PI's and PPO's are considered to be PO's (controllable and observable).

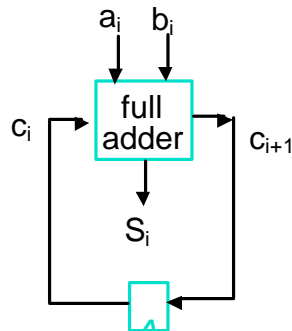
Iterative Logic Array (ILA) Model

- Classical techniques for sequential circuit test generation are based on iterative logic array (ILA) expansion.
- An ILA is a combinational circuit with identical cells.

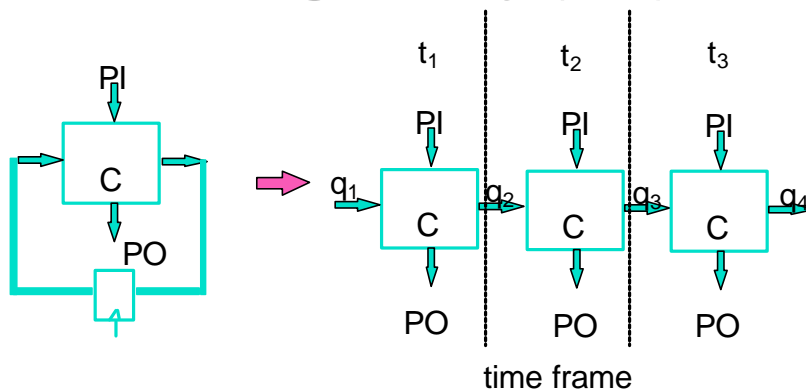


Iterative Logic Array (ILA) Model

- Bit-serial adder



Iterative Logic Array (ILA) Model



- Clock is implicit
- Also called time-frame expansion

Sequential Circuit Test Generation

- Three main components of sequential circuit test generation (not in order):
 - ◆ Excite the fault
 - ◆ Propagate the fault effects
 - ◆ Justify the state with **backward** propagation

