What is a Core?

- A pre-designed, pre-verified silicon circuit block.
  - e.g., microprocessor, video-processing unit, bus interface, BIST logic

- Soft core
  - A synthesizable HDL description

- Firm core
  - A gate-level netlist that meets timing assessment.

- Hard core
  - Includes layout and technology-dependent timing information
What is a Core?

[Zorian, Gupta, IEEE D&T, 1997]
[Crouch, Core Test Basics, 1998]

- Cost-of-Test and Time-to-Market concerns have lead to a Core-Based Design approach.
- Goal is to supply easy-to-integrate cores to the system-on-a-chip market.
- Core design and core integration are major issues.
Testing Challenges in Core-Based Design

- There is no direct access to the core cell ports from the primary inputs and primary outputs of the chip.

- Creation of peripheral access often involves an additional DFT effort.
  - Core integration

- Use of multiple cores within one design, where cores use different DFT strategies.
Test Issues in Core Design

- Making adequate, portable internal core tests.
- Providing core accessibility.
- Composing an integrated test and its control mechanism for the overall system chip.
Core Test

- Need to test Core and User-Defined Logic (UDL)
Internal Core Test

- The core integrator has little knowledge of the adopted core’s structural content.
- The core builder won’t know which test method to adopt, the type of fault, or the desired level of fault coverage.
  - Several versions of a core may be available, each using different parameters or a different DFT strategy.
- The organization responsible for testing the overall chip should define the DFT and Test strategy.
- If intellectual property (IP) is not an issue, a standard DFT approach can be used.
  - Nondisclosure agreements (NDA’s) may be adequate.
Core Access Methods

- Multiplex all core signals so that they are directly accessible from chip package pins.
  - Only possible if number of core I/O’s is small.
- Isolation ring
  - Boundary scan chain
  - Internal (parallel) scan for sequential cores
    ▲ Higher test application time.
- Partial isolation ring
  - Place some core I/O’s in a boundary scan chain.
MUX Isolation

- Core I/O’s are directly accessible from chip I/O’s.
- Need to provide observability for UDL 1 and controllability for UDL 2.
Isolation Ring

- Boundary scan chain for accessing Core I/O’s
- Internal scan chain.

Diagram: A chip with Boundary Data Latches (UDL) connected to a core through scan chains.
Partial Isolation Ring

- Not all core I/O’s placed in boundary scan chain.
- Need observability (for testing UDL 1) for core inputs omitted from boundary scan chain.
- Need controllability (for testing UDL 2) for core outputs omitted from boundary scan chain.