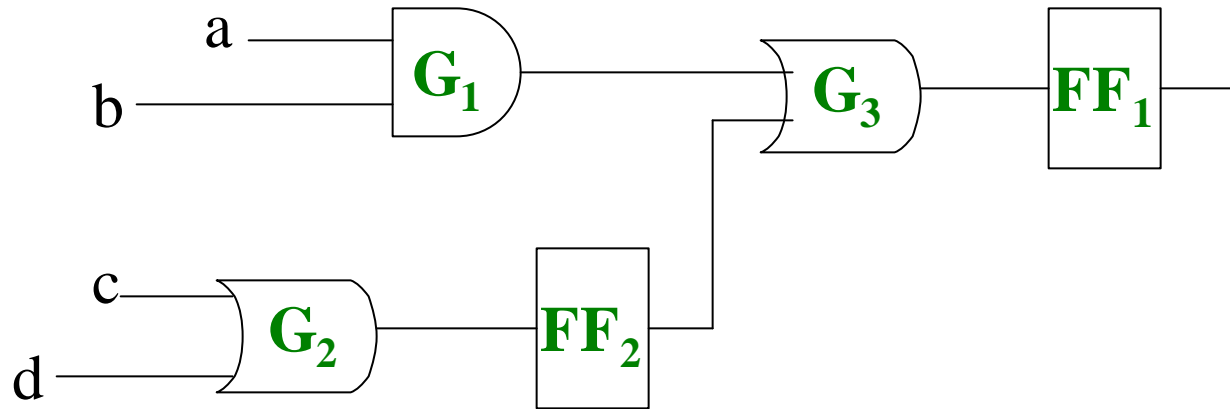


- **Step 1:** Select  $W$  faults from fault list
- **Step 2:** Copy logic values of all FF in Logic Simulator (LS) circuit to L-arrays of FFs in PFS circuit
- **Step 3:** Insert  $W$  faults. For every fault  $i$ :
  - Set  $i$ -th bit of mask for fault  $i$
  - Let  $FF_j$  be in the flip-flop list of fault  $i$  with value  $\nu_l$ .  
“Recover”  $\nu_l$  in the  $i$ -th entry of  $FF_j$ ’s L-arrays.
- **Step 4:** PFS circuit for vector  $V$
- **Step 5:** Examine the  $W$  faults you just simulated:
  - If for some PO the  $i$ -th L-array entry is different to LS  $\Rightarrow$  delete fault  $i$  from fault list and future PFS simulation cycles
  - If all entries are the same (i.e. fault not detected in this cycle) then you need to update  $i$ -th fault’s FF-list
    - **Delete old list and save all FFs with  $i$ -th L-array entry (i.e. next state) different from LS value**



**Faults (in linked list):** a s-a-1, c s-a-0, G<sub>3</sub> s-a-0, G<sub>3</sub> s-a-1

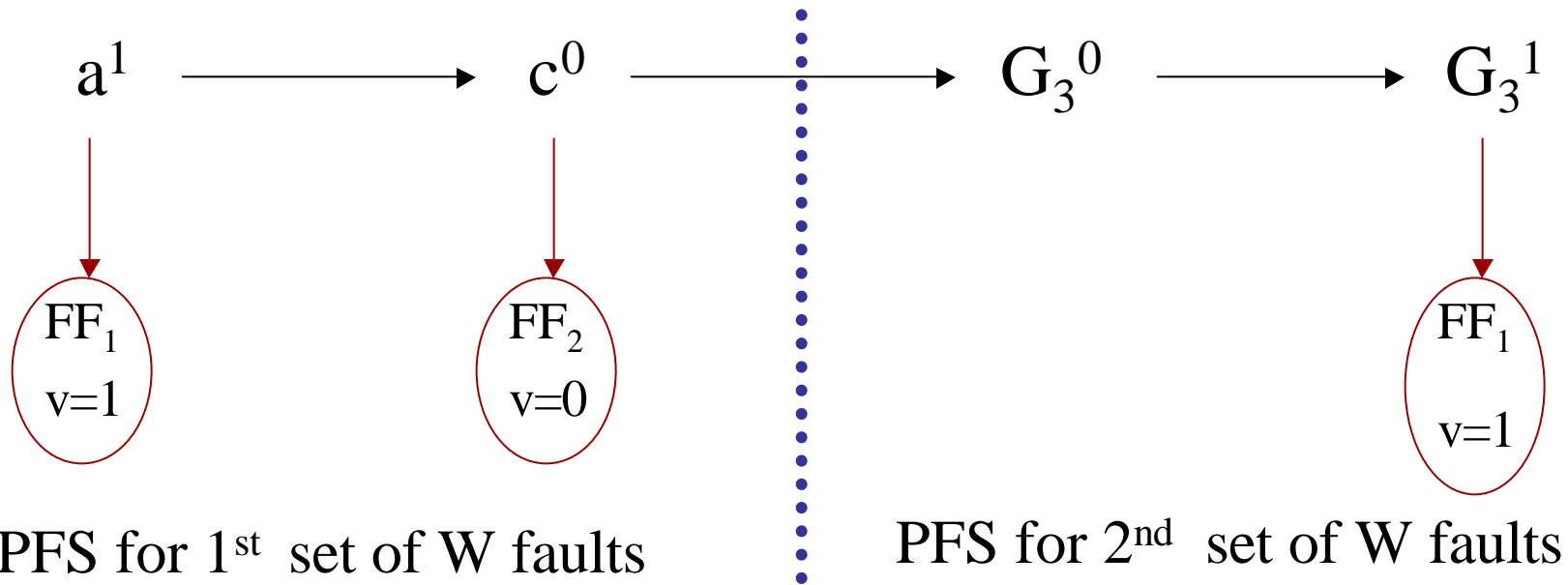
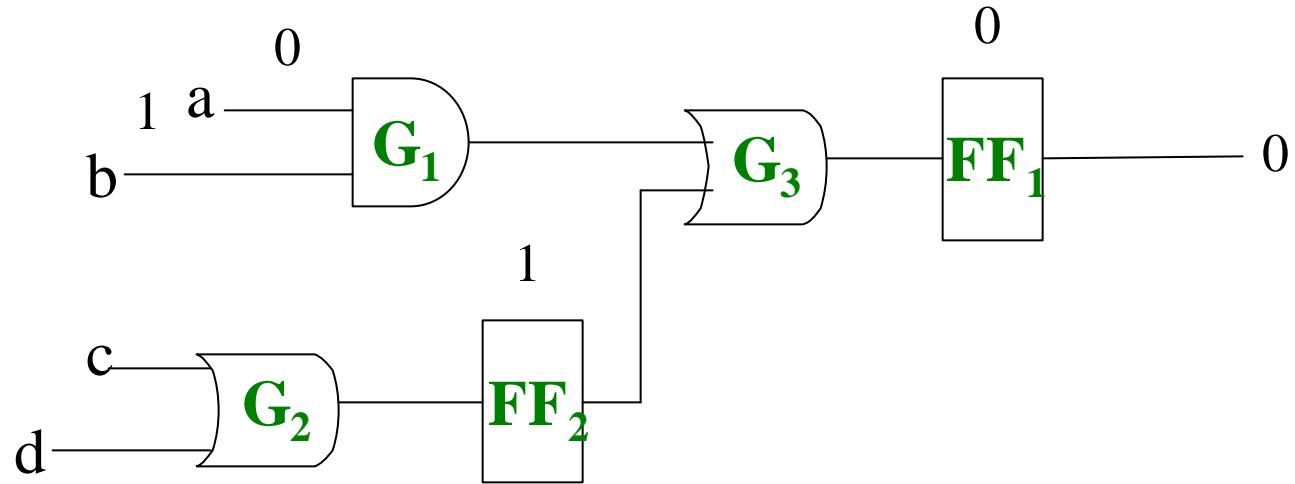
**Word length W:** 2

**Initial FF value:** 0 (reset)

**Input vectors (a, b, c, d):** (0, 1, 1, 0) and (1, 1, 1, 0)

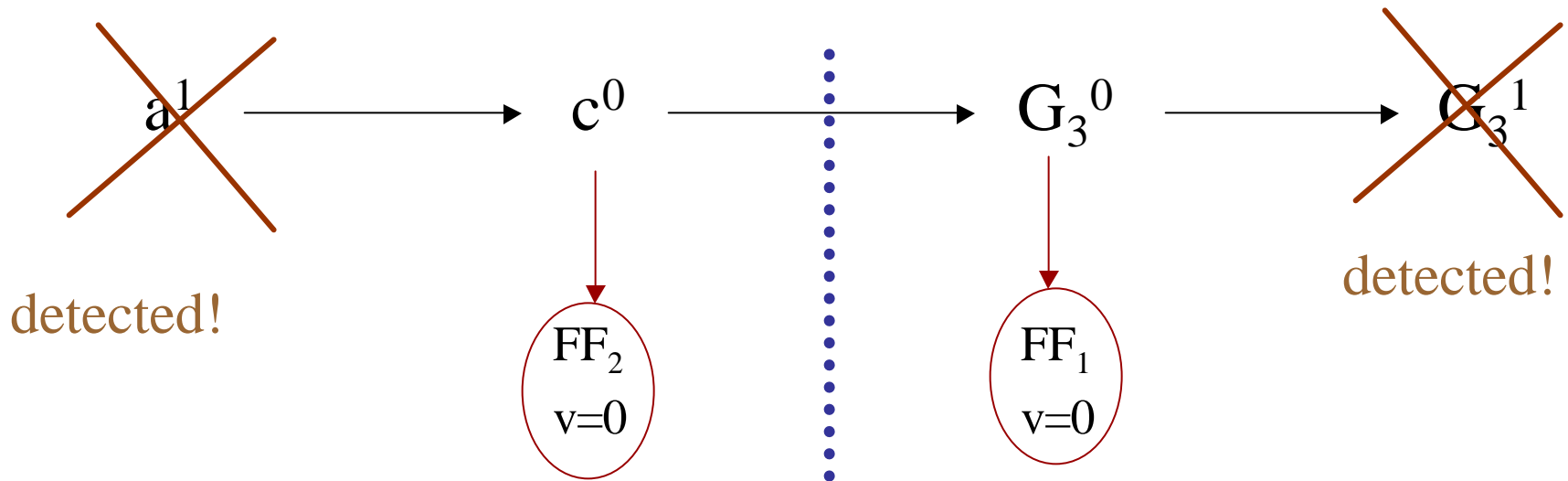
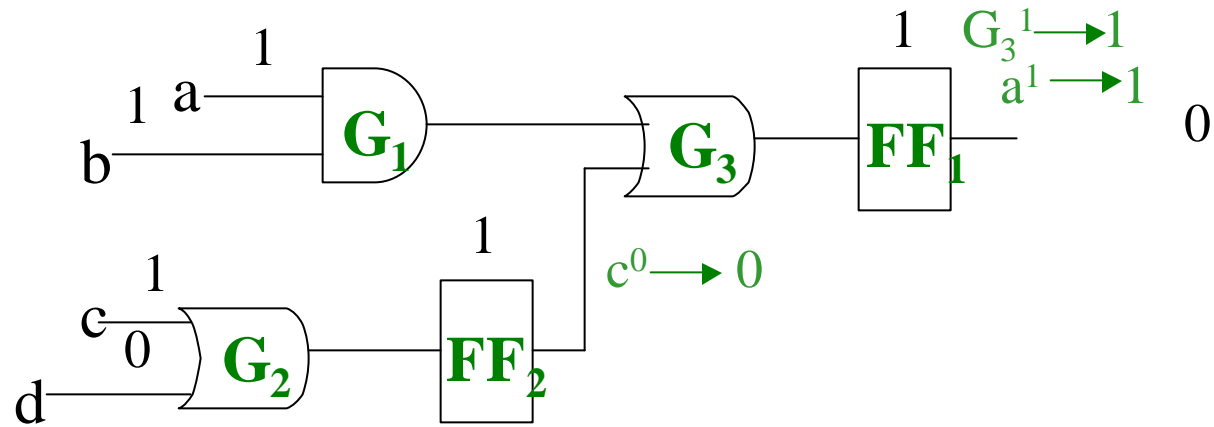
# First Simulation Cycle for vector $(a, b, c, d) = (0, 1, 1, 0)$

LS



## Second Simulation Cycle for vector (1, 1, 1, 0)

LS



PFS for 1<sup>st</sup> set of W faults

PFS for 2<sup>nd</sup> set of W faults