



Design Approaches to Field-Programmable Analog Integrated Circuits

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Abstract. The drive towards shorter design cycles for analog integrated circuits has given impetus to several developments in the area of Field-Programmable Analog Arrays (FPAAs). Various approaches have been taken in implementing structural and parametric programmability of analog circuits. Recent extensions of this work have married FPAAs to their digital counterparts (FPGAs) along with data conversion interfaces, to form Field-Programmable Mixed-Signal Arrays (FPMAs). This survey paper reviews work to date in the area of programmable analog and mixed-signal circuits. The body of work reviewed includes university and industrial research, commercial products and patents. A time-line of important achievements in the area is drawn, the status of various activities is summarized, and some directions for future research are suggested.

Key Words: FPAA, FPMA, FPGA, programmable analog, IC, analog CAD, field-programmable, mixed-signal IC

1. Introduction

The role of analog integrated circuits in modern electronic systems remains important, even though digital circuits dominate the market for VLSI solutions. Analog systems have always played an essential role in interfacing digital electronics to the real world in applications such as analog signal processing and conditioning, industrial process and motion control and biomedical measurements. In addition, analog solutions are becoming increasingly competitive with digital circuits for dense, low-power, high-speed applications in low-precision signal-processing. An important advantage of digital integrated circuits has been their relative ease of design over analog circuits. In particular, since digital circuit design is amenable to automation, several CAD-compatible digital integrated circuit design methodologies have been developed, including design-for-testability, design optimization, rapid prototyping in Field-Programmable Gate Arrays (FPGAs) and, more recently, hardware synthesis from behavioral descriptions. In the highly competitive electronics industry, the application of CAD techniques to digital integrated circuit design has led to shorter design cycles, alleviating some of the time-to-market pressures felt by developers of commercial products.

Because of the wide variety of analog functions required in electronic systems and the complexity of the signals (frequency, time, signal levels, parasitics), analog system design is very specialized and supported by a diverse set of CAD tools that are more difficult to integrate than those required for digital design. The drive towards shorter design cycles for analog integrated circuits has demanded the development of high performance analog circuits that are reconfigurable and suitable for CAD methodologies [1].

This has been the motivation for research in the area of Field-Programmable Analog Arrays (FPAAs), which seek to provide accurate, low-cost, rapid-prototyping techniques for analog and mixed analog-digital circuits—a long awaited development for circuit designers. Commercial products introduced recently, along with progress made at University research labs, indicate renewed interest and further accomplishment in achieving this goal. This paper reviews work to date in the area of Field-Programmable Analog Arrays and Field-Programmable Mixed-Signal Arrays (FPMAs). We begin with a general description of FPAAs, followed by a discussion of some of the architecture, circuit design, and implementation issues of programmability in analog circuits.

1.1. General Description of FPAAs

In its most general form, an FPAAs is a monolithic collection of analog building blocks, a user-controllable routing network used for passing signals between the building blocks and a collection of memory elements used to define both the function and structure. Alternatively, the structure may be defined by other means such as antifuse programming. Fig. 1 shows a conceptual block diagram of an FPAAs, including a set of Configurable Analog Blocks (CABs) and a routing network. Configuration memory is provided for the blocks and interconnect. Associated with this is a CAD system, as shown in Fig. 2, that takes the designer's circuit and translates it into a collection of configuration bits that, when stored in the memory elements, instantiates the circuit in the programmable array. Several approaches to realizing such a system have been attempted.

The next step in the evolution of field-programmable analog systems is undoubtedly the integration of analog and digital functions on a single chip, to create a Field-Programmable Mixed-Signal Array (FPMA). One of the characteristics a designer would

like in such a concept is to freely exchange analog and digital signals within the prototyping medium. Market research firms have forecast that mixed-signal ICs will represent 30% of the \$12.7 billion standard-cell IC market in the year 2000, up from 26% of the \$4.8 billion market in 1995 [2]. This indicates that there might be a promising market for a rapid-prototyping medium for mixed-signal ICs.

In this paper we present a detailed survey of work to date in the area of programmable analog and mixed-signal integrated circuits, with a view to introducing the reader to the field of Field-Programmable Analog and Mixed-Signal Arrays. The body of work reviewed includes approaches to making analog circuits programmable both in structure (to implement different circuit topologies) and parameters (to implement variable component values, amplifier gains, etc.). It should be noted, however, that the field of analog circuits with programmable parameters includes numerous publications in areas such as Automatic Gain Control (AGC), programmable amplifiers and filters, from which just a few examples are addressed in this survey of university and industrial research, commercial products and patents.

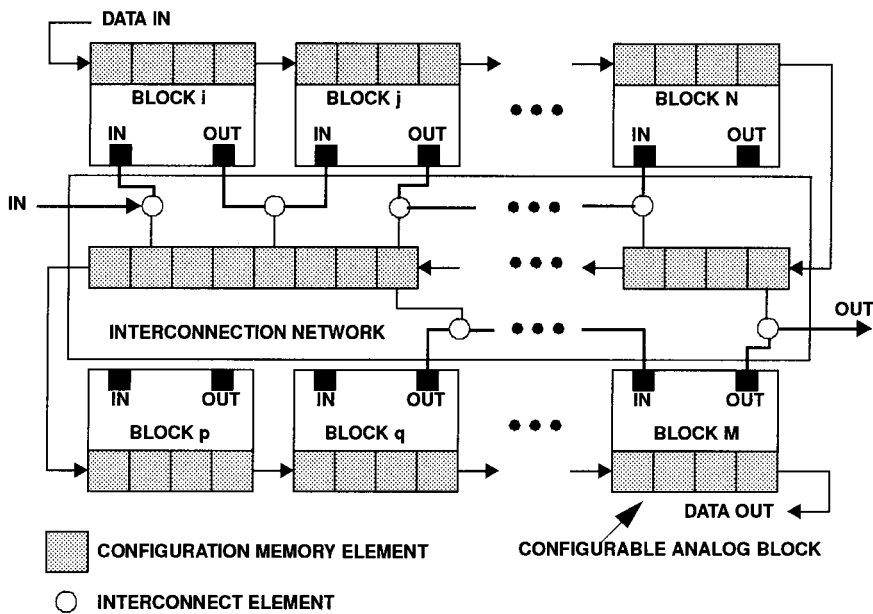


Fig. 1. FPAAs Conceptual Block Diagram.

1.2. FPAA Design Issues

In this section, programmable analog integrated circuit design issues are discussed to provide a foundation on which to base the descriptions of research and commercial work that follow.

1.2.1. Discrete-time vs. Continuous-time. A key choice in the implementation of an FPAA is whether to operate in discrete-time or continuous-time.

Discrete-time approaches, such as switched-capacitor circuit techniques, are well suited to digital control and hence do not require the use of on-chip tuning circuitry for VLSI implementations of programmable components. However, such sampled-data techniques require that input signals be bandlimited to at least one half of the sampling frequency, and hence anti-aliasing and reconstruction filters must be used. This requirement often limits the bandwidth of discrete-time FPAA circuit implementations. The integrated circuits described in the literature that operate in discrete-time employ various techniques, namely: switched-capacitor circuits [3,4], controlled duty-cycle signal chopping and reconstruction [5], analog to digital conversion followed by digital

processing and digital to analog conversion [6], or switched-current circuits [7].

Continuous-time circuit techniques [8–12] do not need bandlimited input signals, but may require more complicated implementations to have circuit components programmable over a large dynamic range. Continuous-time techniques of both subthreshold and linear circuits have been used in programmable analog circuits.

1.2.2. Voltage-mode vs. Current-mode. Another important design choice is whether to use voltage or current as the signal parameter in the FPAA implementation. Voltage signals have a high fanout, and voltage-mode circuit techniques are well-developed. Several programmable analog circuits have been developed based on voltage mode signals [3–5,8,9,13].

However, advantages such as the simpler implementations of current mode circuit operations (e.g. algebraic addition can be performed simply by wiring signals together), and the high accuracy and high bandwidth of current-mode amplifier circuits [14], have led to the choice of current as a signal parameter for some implementations of programmable analog

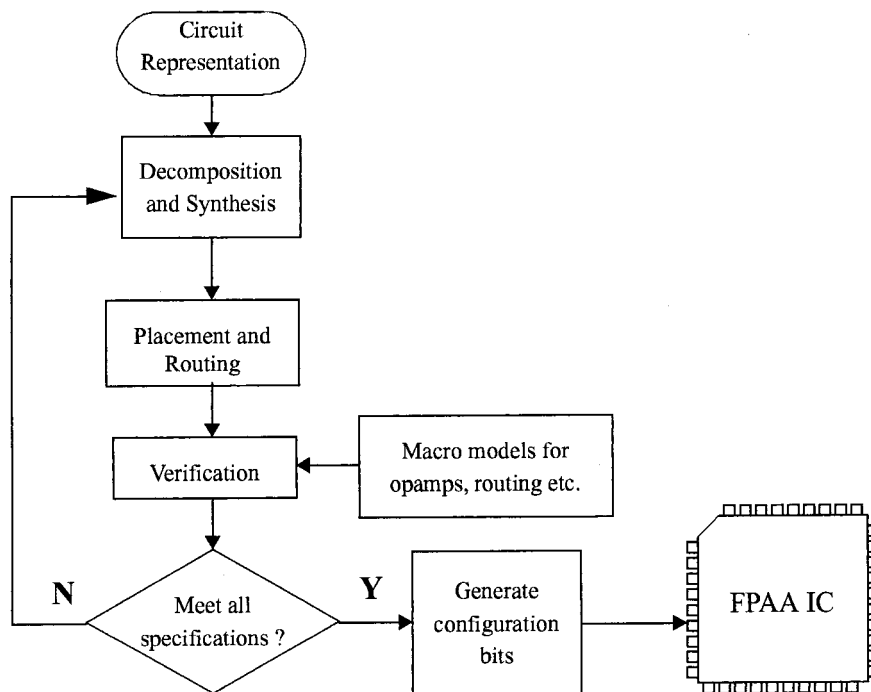


Fig. 2. The FPAA Design Process (from [18]).

circuits [7,10–12]. Recent trends towards lower power supply voltages have reduced the dynamic range available in voltage-mode circuits, making current-mode signalling more attractive [15]. In this context, the concept of “adjoint networks” [15] is interesting in that a transformation between voltage- and current-mode implementations of circuits is possible, and an adjoint realization of a circuit may lead to superior noise performance. Mixed voltage- and current-mode approaches have also been attempted [16].

While both discrete- and continuous-time methods are possible for voltage- and current-modes, discrete-time approaches have been predominantly voltage-mode. Discrete-time current-mode approaches such as switched-current circuits [17] might provide approaches for future programmable analog circuits, as demonstrated in [7].

1.2.3. CAB Design. The design of the Configurable Analog Block (CAB), the basic cell used in FPAA, is usually influenced by a number of factors, including the functionality and performance features of circuits to be prototyped, the area-efficiency of routing resources dictated by the CAB design itself and the supporting semiconductor process technology. A key issue is the level of granularity. Fine grain FPAA architectures (reconfigured at the transistor level, for example) will require more routing resources and will have more switches in the signal path than a coarser grain FPAA architecture (reconfigured at a macro-block level, e.g. integrators, S/H). However, the coarser architecture will be less versatile, i.e. it will be able to implement a narrower range of circuits than the fine architecture. Another issue is whether to make the CABs distinct for different circuit functions, or identical, but programmable to implement different functions. This choice will influence the area of the CABs and routability of circuits within the FPAA. CAB design can thus be seen to strongly influence the FPAA area, the routing requirements, the variety of circuits that can be prototyped and the performance of circuits prototyped on an FPAA. These issues were explored in a detailed study of CAB design, based on a set of application circuits for analog signal processing [18]. CABs of a few different types were designed; some of them were made reconfigurable where this could be done area-efficiently. The granularity level observed to be most area-efficient in this study was

termed “building block,” and included opamps, programmable resistors and capacitors.

1.2.4. Interconnect Architectures and Implementations. The choice of an interconnection architecture and its implementation will influence the routability of prototyped circuits and their performance. Analog circuits are far more sensitive than digital circuits to problems of fanout, noise, and the presence of switches in the signal path. Both hierarchical and full crossbar interconnection architectures have been used. Interesting work, influenced by Cellular Neural Networks, has been done in the area of cellular interconnect architectures, in which CABs are connected only to their nearest neighbors [3,10].

Pass transistors and CMOS transmission gates have been used as switches to reconfigure the topology of the circuit being implemented. Some approaches to implementing FPAA have used circuits with MOS transistors operated in the sub-threshold region. In these implementations, voltage drops due to switch on-resistance are not a problem because of the extremely small currents in the circuits [16,19]. In linear circuit implementations of FPAA, where the currents flowing through the switches are much higher, circuit techniques such as linearization of switch resistance [8] or judicious placement of transistor switches in the circuit embedding [9], have been applied to minimize the effects of the non-idealities of the switches. Other designs have made circuit structure reconfigurable without the use of extra switches in the signal path, by the use of discrete-time sampled-data techniques [3–5]. In these designs, switches used for circuit operation are also used to program the circuit structure. Alternatively, signals can be coupled from one CAB to another without reconfiguration switches in the signal path by changing the bias of an interface circuit such as a current source [10].

1.2.5. Programmable Components. Various methods have been used to implement programmable resistors. These have included the use of polysilicon resistors switched into circuits with pass transistors [20], complementary MOS transistor pairs with controlled gate voltages [21] and more complex transistor implementations of programmable resistive elements such as MOS transconductors [8]. Programmable capacitor arrays have been widely used, especially in switched-capacitor circuits [3,4], in which they can be

made to emulate programmable resistors. The literature contains several publications and products in the areas of programmable amplifiers and filters [22–25]. On-chip tuning circuits may be required to produce bias voltages or currents that set the value of programmable components. These circuits often involve the use of digital registers to store component values, and digital to analog conversion to produce the bias voltage or current.

1.2.6. Configuration Memory. Two types of configuration memory are typically found in a programmable analog integrated circuit. Digital registers are widely used to store the states of connection switches as well as the values of components such as programmable capacitor arrays. Analog memory is commonly used to store circuit parameters such as multiplication coefficients or the gate voltages of a MOS transistor in a circuit implementing a programmable resistor. Storing a voltage on a capacitor is the most common implementation of analog memory, and requires a means for refreshing the stored voltage [26,27], as well as consideration of errors due to charge injection from access transistors [28]. Error correction of the analog memory contents has been demonstrated [29], as has current-mode multivalued memory [30]. Organization of the digital memory has been done in different ways, including serially; in which all memory cells are connected together as a single shift register, serial-parallel; where a serial bit-stream is loaded into a horizontal shift register, the contents of which are then strobed into a row of configuration memory indexed by the bits in a vertical shift register, and finally random access, where address lines determine where the input configuration data goes. The latter two approaches can be used to reconfigure parts of the IC while other parts continue to operate.

It should be noted that configuration memory can occupy a significant proportion of the total die area of an FPAA integrated circuit.

1.2.7. CAD Tools. Field-programmable analog circuits to date have required configuration bit-streams ranging from several hundred to a few thousand bits to instantiate the circuits being prototyped on them. Generation of this configuration bit-stream from a definition of the circuit and downloading of the bits onto the chip needs to be handled by a CAD tool. Because of the many different circuit techniques used

to implement existing programmable analog circuits, the use of many of the present CAD tools requires detailed knowledge of circuit design using the appropriate circuit techniques, or working at a higher level of abstraction, commonly called the macro-block level, with predesigned components from a library [31]. Some CAD tools display the entire FPAA architecture on a single screen, enabling a user to configure each block and make the interconnections that instantiate the circuit being prototyped [32–34].

The area of FPAA CAD tools has a number of research issues to be addressed. Software is required that will allow design and schematic capture in terms familiar to a circuit designer, followed by technology mapping, placement and routing for the target FPAA or FPMA architecture with adequate consideration of analog IC issues such as noise and layout parasitics. Recent moves towards the standardization of Analog Hardware Description Languages [35–37] should serve to unify efforts in CAD development.

1.3. Organization

This paper is organized as follows: Section 2 describes some early approaches to the design and implementation of non-monolithic configurable analog systems, and discusses some IC design approaches related to FPAAs and FPMAs. Section 3 looks at several first-generation works in programmable analog integrated circuit research. In Section 4 we describe the present state of the art, including academic and commercial research ventures, commercial products and patent literature. Conclusions and suggestions for future work are presented in Section 5.

2. Early Configurable Analog Systems and Related IC Approaches

By way of background, this section discusses some early configurable analog systems. Parametrically configurable building blocks and flexible interconnection systems were used to build analog signal processing systems that provided signal-conditioned and pre-processed signals to digital computers for further analysis. These approaches foreshadowed in

intent later work that appears in monolithic form. We also discuss two CAD-compatible analog integrated circuit approaches that are related to FPAA's, namely metal-masked analog arrays and analog standard cells.

2.1. Analog Computers

In the 1960s analog computers were commonly used as hardware simulators in various areas of science and engineering. We describe a nuclear measurement system and a power system simulator based on systems of analog building blocks.

2.1.1. Arbel Nucleonic Computer. One of the first published attempts at identifying standard analog building blocks that could be used to build reconfigurable analog signal processing systems is presented in [38]. The application, in the field of nuclear instrumentation, was signal conditioning and pre-processing of the current-output signal from a radiation detector, before digital signal processing by a computer.

Current was chosen as the signal parameter for this system. The building blocks included linear amplifiers, discriminators, ADCs, time-to-amplitude converters, linear gates and analog memory modules. Where necessary, parametric configuration was performed by using front-panel controls. The blocks were interconnected with coaxial cables that could be used (by appropriate choice of the cable length) as signal delay elements.

2.1.2. Power System Simulators. Another early application of configurable analog circuits [39] sought to build a real-time simulator for power system studies, with a modular approach that would permit flexibility in configuring the parameters of the components and the topology of the system being modeled. To implement the simulator, circuit models of the power systems were created from differential equations in state variable form. The analog blocks used in the circuit implementation included integrators, linear amplifiers, non-linear elements, weighted summers and resistors. Power system components such as transformers, machines, transmission lines, filters and valves were modeled using this technique.

Simulation studies were performed to model HVDC transmission and inrush transients of transformers.

2.2. FPAA Related IC Approaches

In this subsection we discuss two IC implementation approaches related to FPAA's, namely metal-mask programmable analog arrays and analog standard cells.

2.2.1. Metal-mask Programmable Analog Arrays. Metal-mask programmable gate arrays are widely used for short fab cycle-time, low-cost implementations of digital integrated circuits. The circuit being implemented is instantiated in a sea-of-gates (SOG) array using a custom set of metal-masks. In our discussion of field-programmable analog and mixed-signal arrays, metal-masked arrays are interesting as a related approach that seeks to define VLSI implementations of analog building blocks that can be used to build useful circuits. Metal-masked analog arrays are also important as an extension of the FPAA design flow as a smaller-area and lower-cost means of implementing, in high volume, circuits that have been verified using FPAA's/FPMA's. Such an extension is provided for IMP's family of EPAC integrated circuits [32].

Metal-masked array technology has long been in existence for bipolar designs [40]. To provide the functions required by analog designs, these arrays tended to have small numbers of coarse granularity cells that were more complex than the fine granularity devices present in large numbers in digital arrays. Special function cells such as high power devices and voltage references were also common. Interesting in the context of mixed-signal designs is a dense array manufactured by Ferranti Interdesign [40] that packed analog cells around a digital array and in the spaces between bond pads. Another innovation in the field of bipolar arrays was pioneered by Exar [41]; which developed device layouts that could be customized as either npn or pnp transistors by the use of a metal mask. A 1991 U.S. patent [42] awarded to Plessey Overseas Ltd. describes a cell for a semi-custom array that could be instantiated as an npn or pnp transistor, a resistor or a diode by use of an appropriate metal-mask. Recent work in bipolar analog arrays has resulted in a cell-based array for wireless applications

[43] in the GHz range. The array is composed of RF and digital cells that are parameterized and interconnected using a metal mask.

Duchene et al. [44] evaluated the use of existing CMOS digital SOG arrays for implementing analog circuits, and proposed an extended CMOS array consisting of the conventional sea of gates, along with features particularly suited to mask-programmed implementations of analog circuits. An experimental study [44] found that analog circuits implemented in an SOG array with transistors built out of serial and parallel combinations of unit transistors exhibited a 10–50% degradation in performance for parameters such as gain-bandwidth product, offset voltage and phase margin when compared to full-custom IC implementations. The performance attained was found to be adequate for many applications. To further increase the performance of SOG array implementations of analog circuits, floating wells, bipolar transistors and high-precision, high-value resistors are required. An extended array proposed in [44] added to the SOG array an “analog field” containing a bank of resistors, lateral pnp transistors and matched p-channel diffpairs in isolated wells. Area-efficient mask-programmable dedicated-function blocks, in the form of high voltage (100 V) output driver transistors, a bandgap reference and a low-power oscillator, were also included because of their high frequency of usage in analog circuits.

2.2.2. Analog Standard Cells. Analog standard cell design methodologies are more challenging to implement than their digital counterparts. This is because of the wide variations in specifications, such as bandwidth and DC or AC levels of signals, for different instances of a given analog building block (e.g. an opamp) that are used in different circuits, or even within a single circuit. Analog standard cell design methodologies therefore require cells that can be reused in different applications. This requirement is similar to that of FPAA, although the number of different CABs used in an FPAA is typically much smaller than the number of cells in an analog standard cell library. A 1994 U.S. patent [45] describes a scheme for creating standard cells by connecting circuits that perform different functions through a standard interface that sets signal parameters such as DC bias and peak to peak levels.

Certain specialized classes of analog circuits have

used standard cell design approaches. A library of low voltage analog and digital cells, and high-voltage and mixed-voltage analog cells was used to implement a 60-V, 10-A intelligent power switch in a 3 μm analog CMOS process [46]. High voltage cells included charge pumps, level-shifters and protection circuits, mixed-voltage cells provided the sensing functions in the interface between the high voltage circuits and the low voltage analog and digital control circuitry.

Analog circuits for RF and microwave communication have also been implemented using a standard cell technology. Operating in the GHz frequency range, building blocks such as voltage controlled oscillators, power amplifiers and RF switches have been implemented in a 0.8 μm BiCMOS process [47]. Especially interesting in the context of reconfigurable analog integrated circuits are the RF switches, which are typically used to share components such as filters, between the transmitter and receiver sections of a radio circuit [47]. The implementation of reusable building blocks, along with integrated circuit switches to connect them together will likely influence the development of field-programmable integrated circuits for these specialized applications.

3. Previous Work

Previous work in the area of programmable analog integrated circuits is dominated by programmable neural network ICs. Another more general approach is evident in circuit implementations of the multiplication of a signal vector by a matrix of coefficients. The first field-programmable analog arrays employed continuous-time subthreshold circuit techniques, using basic building blocks interconnected by transistor switches to implement prototyped circuits. A discrete-time approach to programmable analog circuits used controlled duty cycle chopping of signals followed by signal reconstruction to implement analog coefficient multiplication in z-domain filter circuits.

3.1. Programmable Neural Networks

Programmable neural networks are an important class of programmable analog circuits. A summary of important research and commercial works in the area

of neural networks can be found in [48]. Hardware implementations of neural networks required programmable structure, adjustable gain in the neuron characteristic transfer function, and programmable interconnection weights. A block diagram of a reconfigurable neural network is shown in Fig. 3.

Programmable analog neural network research has yielded several commercial programmable neural network chips and systems [48–51], along with circuit techniques, IC implementations and experimental results for programmable analog functions and interconnect, that have been valuable to the development of more general programmable analog circuits. In particular, the storage of analog circuit coefficients on local capacitors refreshed with the results of a digital to analog conversion of the contents of digital memories [26,27], has provided means for parametric programming of analog circuits that have been used in other implementations of programmable analog circuits [52,53]. The core of the analog circuitry in one neural network processor [20] was a programmable resistor chip, containing five-bit programmable resistor networks used to implement the synapses. It is significant that the earliest monolithic implementations of programmable analog circuits, composed of basic undedicated building blocks [16,19], were designed with neural networks as important intended applications.

Cellular Neural Networks (CNN) were introduced in [54] as a new class of neural network circuits,

characterized by local-only interconnections and spatially-invariant connection weights. Since the cells of a CNN are interconnected only with cells in a specified neighborhood, this class of neural networks is fixed in structure, but programmable by a set of templates which define interconnection strengths and bias constants for the cells. Research into locally-connected CNNs has led to the identification of other classes of analog circuits [10] that can be implemented on FPAAAs with local-only interconnect architectures, and some FPAAAs [3,10] have been designed with architectures that employ local interconnections to achieve programmable structure without the use of connection switches in the signal path. Programmable current-scaling circuits such as those used in [55,56] will allow the development of current-mode interconnect architectures. As analog circuits address problems in real-time image processing, where the density of “a computer at each pixel” might be required [1], programmable neural network research will likely continue to influence the development of configurable analog circuits. Research in the area of CNNs is progressing in an interesting direction [57], one that seeks to develop high level control of analog computing with the use of CNN based analog and logical computing units. VLSI implementations of these mixed-signal “analogic” processors will give further impetus to the development of programmable analog and mixed-signal integrated circuits.

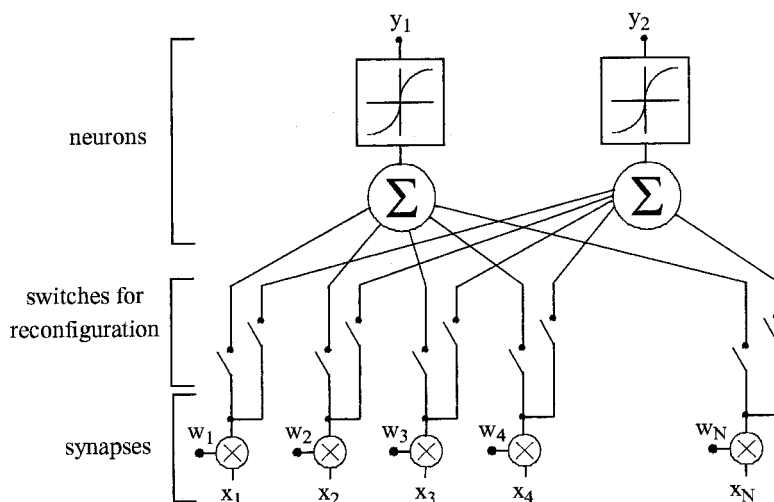


Fig. 3. A Reconfigurable Neural Network (from [28]).

3.2. Programmable Analog Vector-Matrix Multipliers

In [27], Kub et al. studied the vector-matrix multiplication operation

$$V_{Yi} = \sum_j W_{ij} V_{Xj}$$

where V_{Xj} is an input vector element, W_{ij} is a matrix of weights and V_{Yi} is the output of the multiplication operation. This operation finds application in many neural-network and signal processing algorithms. Fig. 4 shows a possible circuit implementation of this operation. An analog implementation of this operation offers the benefits of lower power consumption, higher density and faster performance than a digital implementation. A 32×32 programmable vector-matrix multiplier IC has been described in the literature [27], comprising an array of analog multipliers with weight coefficients in the analog memory periodically refreshed from the contents of digital registers. An architecture was described for implementing a multilayer neural-network from cascaded vector-matrix multipliers.

A 1991 U.S. patent [58] describes the design of a resistive network for the purpose of calculating, in real-time, a complex signal transformation of an input signal. The invention is targeted at complex signal transformations such as the Discrete Fourier Transform (DFT), which can be expressed as a sum of products, and hence as a matrix-vector multiplication operation. Time-domain samples of the voltage-mode input signal are created by passing it through a series of delay elements. These voltage

samples are converted to currents by resistors in the network. The currents are then summed at network nodes, creating the output terms in the sum of products expression of the complex signal transformation being performed. The coefficients of the multiplication are thus inversely proportional to the resistance values.

3.3. Sivilotti Proto-chip

A field-reconfigurable IC called the Proto-chip, intended primarily for synthesis and test of analog neural-network architectures, is described by Sivilotti [19]. CMOS transmission gates were used as the active switch elements that connected basic resources such as differential pairs and current mirrors in a hierarchical routing network. A conceptual view of the Proto-chip depicting the circuit embedding of a transconductance amplifier is shown in Fig. 5.

While the on-resistance of connection switches was not an issue in implementing the low-current subthreshold circuits for which the Proto-chip was intended, parasitic capacitance of the wiring and switches in the interconnection network did present a problem. To minimize capacitance effects, transistor scaling and ‘‘ring transistor’’ layouts [19] were used to maintain a constant ratio of current drive to capacitive load for the transistors in the leaf cells. On board memory (SRAM) was used to store the state of each switch element, but no memory was provided for storing circuit coefficients.

Partial test results were published, including a ring-oscillator test of the performance of the interconnect

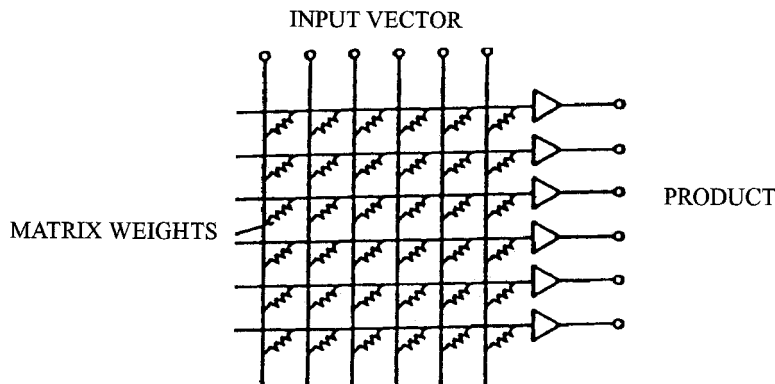


Fig. 4. Block diagram of a circuit implementation of matrix-vector multiplication (from [27]).

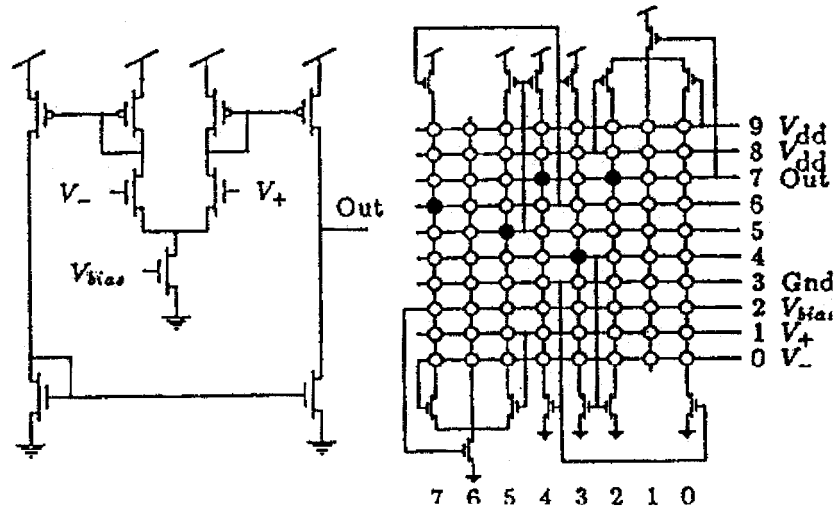


Fig. 5. Sivilotti Proto-chip showing circuit embedding of a transconductance amplifier (from [19]).

and measurements of the resistive and capacitive parasitics of the interconnect. A companion CAD tool to this FPAA system was a “metacompiler,” which created a description of a Proto-chip given parameters for the interconnect and a leaf-cell layout which met some layout dimension constraints.

3.4. Lee-Gulak Sub-Threshold FPAA

In later work, Lee and Gulak [16,52,59] developed a low-power FPAA based on MOS sub-threshold circuit techniques. This IC employed both voltage- and current-mode circuits and was designed to implement structurally and parametrically reconfigurable neural-networks. Pass transistor switch networks controlled by SRAM-based memory elements were used as the active switch elements that connected basic resources such as differential pairs, current mirrors and transistors. Multi-valued memories were used to store circuit coefficients. The interconnect architecture of the FPAA was hierarchical. A circuit diagram of the CAB for this FPAA is shown in Fig. 6.

A prototype FPAA, comprising a sub-tree which included two Configurable Analog Blocks (CABs) and a switch-block, was fabricated. Experimental results verified the functionality of the FPAA and characterized the performance of the CABs in various circuit configurations. Die-to-die variations in subthreshold

model parameters provided challenges to circuit operation in some applications. A further contribution of this work was the development of macro-models of the CABs to be used for the design and simulation of neural networks implemented on the FPAA.

3.5. Timing-Controlled ASP

Seeking to achieve the programmability associated with digital signal processing, without the need for complex circuit structures such as ADCs, DACs and microprocessors, an analog emulation of z-domain filters was proposed by Vallancourt and Tsividis [5,60]. For this class of filters, transfer functions are determined for a given filter topology by the signal gain in each network branch.

The implementation of these Analog Signal Processors (ASP) avoided the use of programmable resistor and capacitor arrays by chopping the input signal with a transmission gate switched at a digitally controlled duty cycle, followed by signal reconstruction to effect the analog multiplication that determines network branch gain. This technique, described in [5], uses a periodically reset integrator to reconstruct sampled signals and a Low Pass Filter (LPF) to reconstruct non-sampled signals, enabling all coefficients of the filter transfer function to be individually programmable using duty cycle control alone.

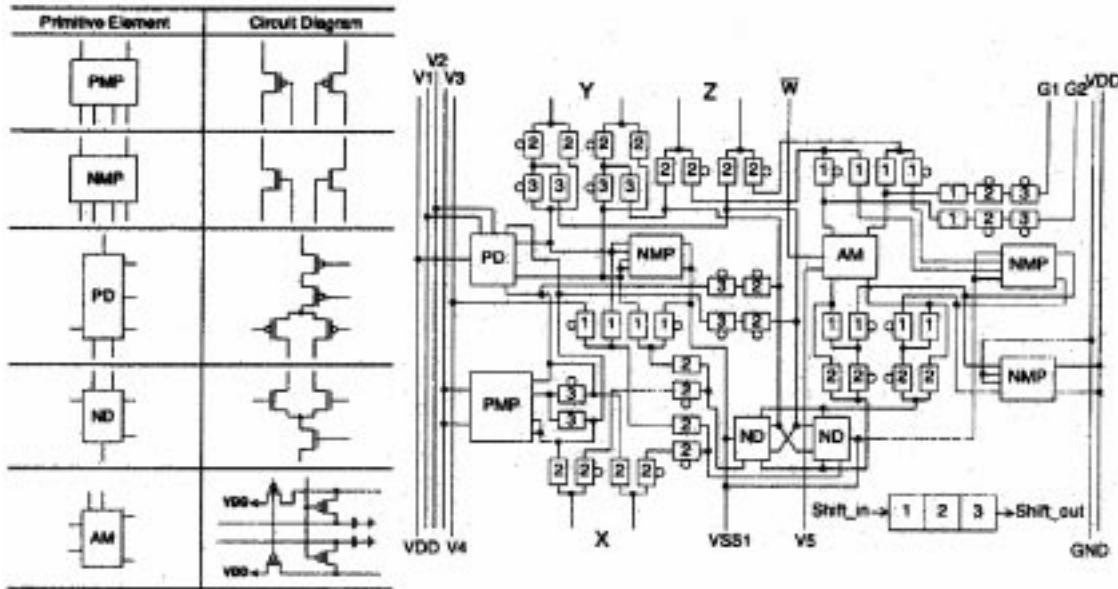


Fig. 6. CAB design for the Lee-Gulak sub-threshold FPAA (from [59]).

Weighted summation of signals could also be implemented by using this technique with appropriately sequenced chopping signals [60]. Programming of circuit structure was also demonstrated, with switch selection determining the filter topology, addressing the problem of interconnection network parasitics by using connection switches as circuit components. The timing-controlled technique has the added advantage of the capability to trade signal bandwidth for resolution in coefficient programming after fabrication, by varying the system clock and chopping signals. It should be noted that whether operating on sampled or non-sampled signals, the timing-controlled technique requires that input signals be bandlimited to at least one-half the chopping frequency.

Experimental results were published [5] for a sampled signal, fully-programmable biquad filter with a sampling rate of 16 kHz. A single second order section was used to implement an automatically reprogrammed, time-interleaved, fourth order low-pass transfer function. In addition to being a possible candidate for FPAA architectures, this technique represents a CAD-compatible analog design method appropriate for circuit implementation on FPMAs, in which the digital circuitry would generate the timing signals, and the analog circuitry would implement the switches and LPFs used in the ASP.

4. Present State of the Art

In this section we describe various field-programmable analog and mixed signal integrated circuits that have resulted from research at academic and commercial laboratories, as well as commercially available programmable analog components and integrated circuits. This is followed by a discussion on the status of intellectual property ownership in this field. A status table and a time-line of major achievements in the fields of FPAA and FPMA integrated circuits are presented at the end of the section.

4.1. Field-Programmable Analog Arrays

The body of present work consists of several field-programmable analog array integrated circuits that have resulted from research in the academic and commercial sectors.

4.1.1. PMeL-Motorola FPAA. Pilkington Micro-Electronics (PMeL), has published details [3,61,62] of an FPAA based on switched-capacitor circuit techniques. This IC consists of a 4×5 array of programmable analog cells each containing an operational amplifier, a programmable capacitor

array and a set of CMOS transmission gate switches. Local RAM within each cell holds digital configuration data that is decoded by a configuration manager to set the connectivity and switch phasing of the switches in the cells, implementing the desired function. Fig. 7 shows a conceptual view of a cell implementing a switched-capacitor integrator. Each cell is locally interconnected with nine neighboring cells, with each cell selecting at its input the signals required to implement the programmed function. Global interconnections are facilitated by a pair of routing tracks in each horizontal and vertical channel in between cells, with an array of switches at the intersections of tracks to make cross connections. Parasitic-insensitive circuit techniques were used in the design of the switched-capacitor cells to minimize the effects of signal degradation in the FPAA routing. The cells can be configured to implement several analog subcircuits including operational amplifiers, comparators, gain stages, first-order filter sections, integrators and differentiators [31]. Switches can be

dynamically controlled by signals internal to the array, allowing the implementation of designs such as switched-capacitor full-wave rectifiers. A circuit embedding for a PCM CODEC using several analog cells was described in [3]. To date, experimental results have been published for a test of the analog cell as a variable gain amplifier. Commercial products based on this research are expected to be released in 1997 following Motorola's recent acquisition of PMeL [63].

4.1.2. Lee-Gulak Transconductor based FPAA. A MOS-Transconductor based FPAA has recently been described in the literature [8,53]. It consists of operational amplifiers and programmable capacitors linked by a transconductor based interconnection array. The innovation in this design is that the switches in the interconnection network are in fact programmable linear resistors in the circuit being prototyped. Fig. 8 shows the circuit embedding of a filter biquad section in this FPAA. Programmable

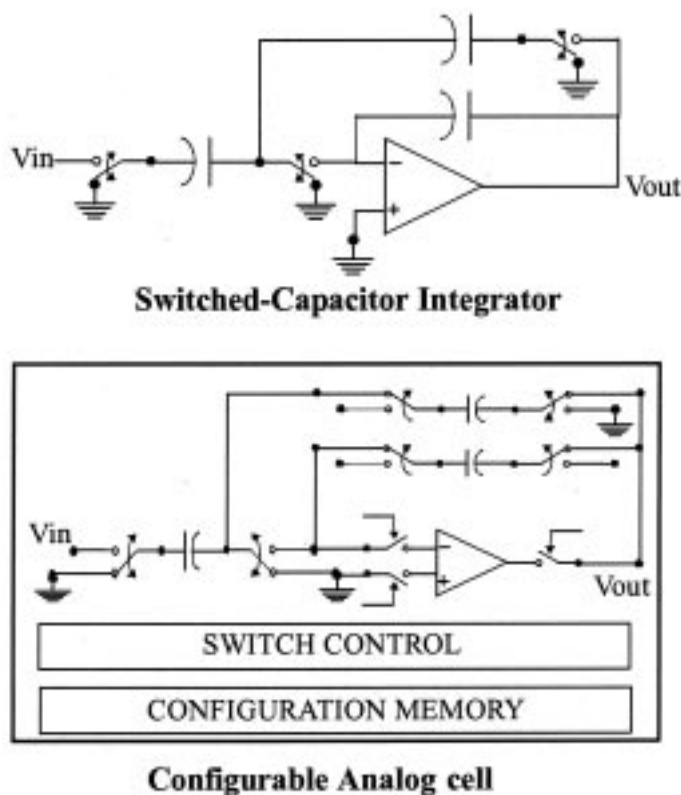


Fig. 7. Conceptual view of the PMeL-Motorola switched-capacitor FPAA cell showing embedding of an integrator.

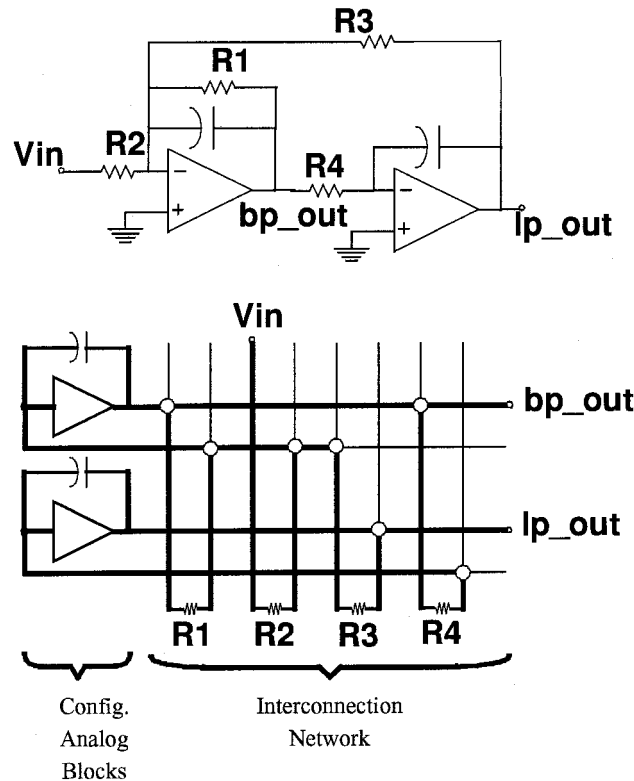


Fig. 8. Lee-Gulak FPAA showing circuit embedding of a filter biquad.

resistors are implemented as four-transistor MOS transconductors [64], a circuit arrangement that uses four matched MOS transistors operated in the linear region, cross-coupled such that the non-linear components in the drain currents are cancelled for fully-differential voltage inputs and current outputs. This results in a circuit that can be used as a programmable linear resistor, a signal controlled resistor, a signal multiplier or a polarity change switch. A modification [18] of the basic transconductor circuit, shown in Fig. 9, splits each transistor into three serially connected transistors, with the transistors in the centre implementing a high resistance value set by the voltage contents of an analog memory periodically refreshed from on-chip 10-bit digital registers, and the transistors on the ends implementing lower-resistance termination parts that switch the resistor into the circuit being implemented by the FPAA.

This FPAA was designed to implement applications in the area of analog signal processing. An analysis [18] was carried out for FPAA implementa-

tions of a set of benchmark circuits in this field, with functional blocks reconfigured at five different granularity levels, from the transistor level (NMOS, PMOS) to the sub-system level (S/H, ADC, DAC). Parameters studied included the versatility of the blocks at each level (a measure inversely proportional to the number of distinct blocks required to implement a benchmark circuit), the ratio of usage between components (how many resistors were present in the benchmark circuits for each instance of an opamp), and the routing resources required for each granularity level. The building-block level (e.g. opamp, MOS transconductor, capacitor, diode) emerged as a good candidate for FPAA granularity because of the high versatility of the blocks, the area efficiency and moderate routing resource requirements when compared to other granularity levels for implementations of the benchmark circuits.

A fully functional prototype, fabricated in a $1.2\ \mu\text{m}$ CMOS process, was reported in [53]. Functionality and programmability were verified for the configurable analog blocks and interconnect, and several

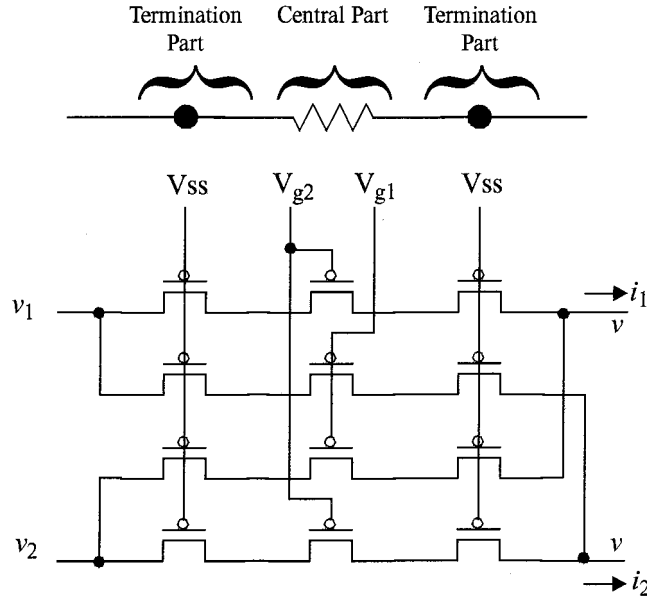


Fig. 9. Modified MOS Transconductor (from [53]).

application circuits operating in the audio-frequency range were implemented and tested. A PC-based CAD tool [33,34] was used for schematic capture, configuration bit-stream generation and device programming.

4.1.3. Analogix bipolar current-mode FPAA. A current-mode bipolar FPAA intended to operate at hundreds of MHz is presented by Analogix Corp./Portland State University in [10,65]. Inspired by the success of locally-connected architectures of Cellular Neural Networks, an analysis of analog circuits showed that certain classes of circuits, notably multistage amplifiers, biquad filters and ladder filters, are readily implemented on an FPAA with a local interconnect architecture. The resulting FPAA comprises an array of homogenous analog cells, each locally interconnected with four neighboring cells without the use of switches in the signal path.

The cells use fully-differential current-mode circuit techniques to implement a set of mathematical functions. The general form of the functions is

$$Y = k \cdot \left[\sum_{w_i \in W_1} w_i X_i \right] \cdot \left[\sum_{w_j \in W_2} w_j X_j \right]$$

where X is the set of inputs to the cell, W_1 and W_2 are independent sets of programmable weights and k is a

programmable gain factor. Special cases of this form implement the operations of summation and multiplication. The result Y can then be integrated with a programmable loss-factor, and passed through a programmable non-linear thresholding and clipping circuit. A block diagram illustrating the programmable cell functions is shown in Fig. 10. Each cell contains a control block which stores cell configuration data, and provides programming signals to the circuits in the cell to control its operation. The control block is capable of configuring the function of the cell depending on signals internal to the FPAA, allowing it to implement such functions as minimum/maximum signal tracking. An additional level of global interconnect was provided to increase the flexibility of the FPAA, however, its use is intended to be minimized because it adds switches to the signal path. Circuit embeddings have been demonstrated for an eighth-order elliptic bandpass filter, a circuit which tracks the solution of a system of linear equations, multi-valued logic applications and a fuzzy-logic controller.

4.1.4. Multi-Function Signal Detection Block.

Chang et al. [9] describe an approach to the construction of an FPAA based on a collection of “Multi-function Blocks,” each of which implements

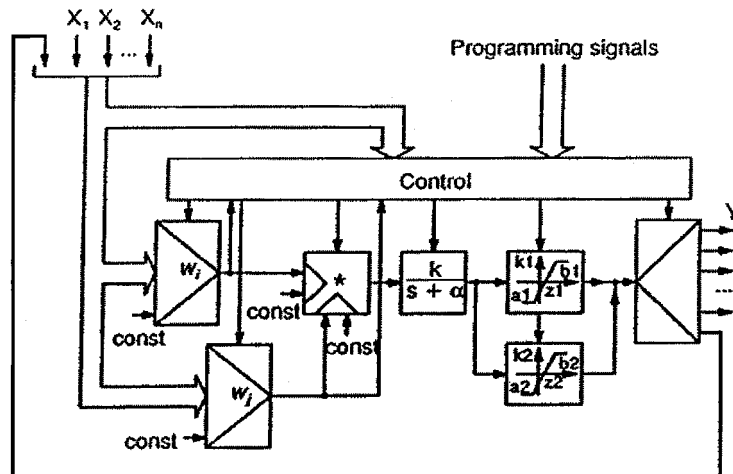


Fig. 10. Block diagram of a cell in the Analogix FPAA (from [65]).

a set of the various analog functions required by the class of analog circuits being prototyped. The function of each block is determined by the state of a number of switches within the block which make the circuit reconfigurable. A “Multi-function Signal Detect Block,” or MFSDB, containing an opamp, a diode, a capacitor and a set of CMOS transmission gates, can be configured as a voltage follower, a peak detector, a half-wave rectifier and a comparator with variable (or no) hysteresis. The block is designed so that, as much as possible in the implementation of the above circuits, the resistance of the non-ideal switches appears either in low-current paths such as those leading to the high-impedance inputs of the opamp, or in series with the opamp output, inside the feedback loop. In the former case, the voltage drop across the switch will be kept small, in the latter the effect of the increase in the opamp output resistance due to the switch can be eliminated by following the MFSDB with a buffer stage. A characterization cell was fabricated in a $2.4\ \mu\text{m}$ CMOS process. Switches and interconnect were reported to occupy a significant percentage (65%) of the layout. Experimental results verified operation of the cell in its various modes, for signals up to 1.2 MHz for the voltage follower, and 11.2 kHz (opamp slew-rate limited) for the half wave rectifier. The sampling time of the sample-and hold circuit was $1.6\ \mu\text{s}$, response time for the comparator was on the order of $3\ \mu\text{s}$. The effects of interconnect on the performance of an FPAA based on this cell were not addressed. Future work was to focus on

building more “Multi-function Blocks,” for functions such as filtering and input/output.

4.1.5. Kutuk & Kang Switched-Capacitor FPAA. A recent publication [4] describes the design of an FPAA based on switched-capacitor techniques, designed to operate at frequencies up to 125 kHz. Each CAB in the design contained a lossless integrator and a lossy integrator, implemented using stray-insensitive switched-capacitor techniques and connected in a loop using switched capacitor connections as shown in Fig. 11. The CAB could be configured using three schemes. By interchanging switch phases, inverting or non inverting integration could be achieved. Switches could be used to connect or disconnect CAB elements from the circuit. Finally, capacitor values could be programmed to one of four capacitance values. The interconnection network between CABs in the FPAA was also composed of switched capacitors configurable in the same ways as in the circuits within the CAB, allowing the use of switched capacitor interconnections to implement signal summation at a node and the use of unswitched capacitor interconnections to realize finite transmission zeros. An Algorithmic State Machine execution unit was designed to configure the array from configuration bits stored in an EPROM. Eight-bit control words were decoded by the control circuit to produce the appropriate control signals for the CAB and interconnection network. The frequency of the clock for the switched-capacitor circuits was pro-

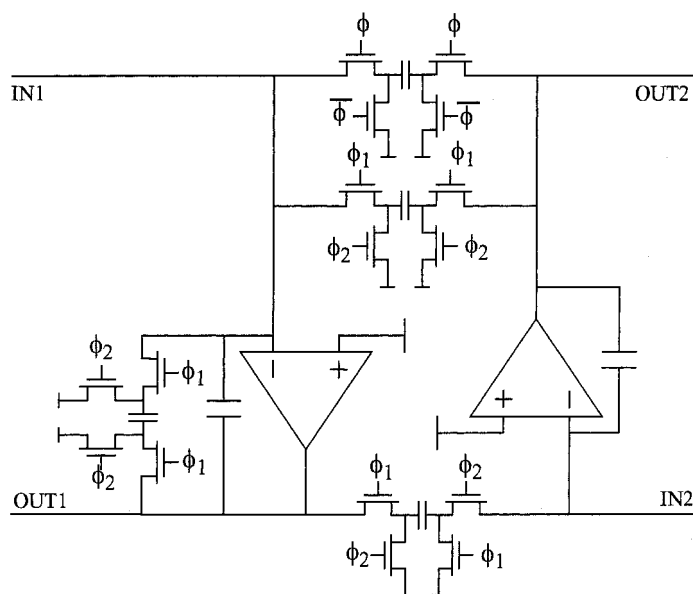


Fig. 11. Switched-Capacitor CAB (from [4]).

grammable in multiples of two between 2 kHz and 256 kHz. Simulation results were given for circuit embeddings of a third-order low-pass elliptic filter, a fourth-order bandpass filter, a balanced modulator and a quadrature sinusoidal generator.

4.1.6. Recent Current Mode Approaches. FPAAs based on current mode approaches have been described in the literature recently. Premont et al. [11] designed an FPAA with CABs consisting of two current conveyors, along with tunable resistors and capacitors. A discrete-time current mode approach was used in the design of a switched current FPAA by Chang et al. [7]. Embabi et al. [12] describe an FPAA based on a folded cascode integrator circuit, which can be configured to function as an integrator, an amplifier or an attenuator. Undoubtedly we will see many more innovative ideas in this area.

4.2. Field-Programmable Mixed-Signal Arrays

To date, field-programmable mixed analog-digital integrated circuit designs have been based on the union of previously designed analog and digital arrays, along with some provision for the exchange of signals between the two domains. Two options,

illustrated in Fig. 12, exist in this respect; dedicated data converters (Fig. 12a) can be implemented to perform the analog to digital and digital to analog conversion of signals, or the converters can be built out of analog and digital resources available in the arrays (Fig. 12b). The works discussed in this section include examples of both options.

4.2.1. U. Toronto MADAR FPMA. A continuous-time FPMA prototype IC called MADAR was described in [66]. It allowed on-chip exchange of signals between the analog and digital domains. This array was built from a previously designed digital FPGA based on four-input lookup tables [67] and the continuous-time FPAA from [53]. Dedicated data converters were designed for the interface between the FPAA and FPGA with a view to improving area efficiency and performance over an interface constructed out of resources within the analog and digital arrays. Several mixed-signal circuits with applications in data conversion and signal processing were studied, to determine the sizes of the analog and digital arrays and the characteristics of the interface in between them necessary to design a prototype chip. The results indicated that the number of interconnections between the analog and digital domains was small compared to the number of connections within each domain, so the

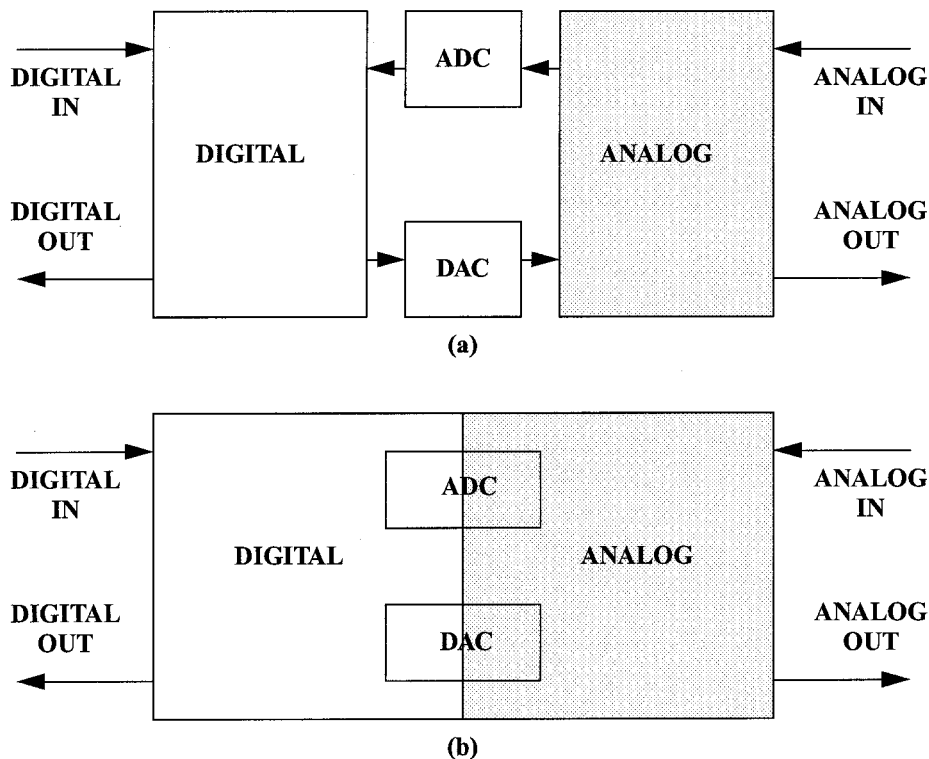


Fig. 12. FPMA Conceptual block diagrams (from [66]).

data converters in the interface were directly connected to the routing networks of the FPGA and FPAA.

Configurability was designed into the converters as a digitally programmable trade-off between converter resolution and the number of converters. The digital to analog converters were based on a MOS current division technique [68], and made programmable with a single configuration bit to split a 4-bit DAC into two independent 2-bit DACs. The analog to digital converter design exploited the fact that multi-step converters are built out of multiple lower-resolution converters. A single configuration bit was used to enable two 2-bit converters to be used independently, or to form a single 4-bit, two-step ADC. The interface included direct connections between the analog to the digital domain, extending the interface to permit analog comparator outputs to tie into the digital routing network, and to allow digital signals to control analog switches in the analog array. A circuit embedding and simulation results were given for a dual-slope analog to digital converter.

4.2.2. PMeL-Motorola FPMA. PMeL has published details of an FPMA [31,69,70] resulting from the integration of their switched-capacitor FPAA [3] with a previously-existing digital FPGA layout, to which the FPAA layout was pitch-matched. Limited details were given concerning the interface between the analog and digital domains, but the design criteria given for the interface describe the exchange of data between the domains via data converters constructed from the analog and digital programmable resources, and dynamic control by FPGA circuits of cell-configuration, component values and reference voltages in the FPAA section. Mixed-signal applications were targeted in the areas of digitally tunable filters, phase-locked loops, A/D and D/A converters. Experimental results were not published. Design of circuits for the PMeL arrays is performed on a CAD tool which supports design at the macro-cell and switched-capacitor circuit levels.

4.2.3. Faura et al. FIPSOC. The design of a Field-Programmable System On Chip (FIPSOC) is des-

cribed by Faura et al. in [71]. The proposed IC is to contain a coarse-grained lookup-table based FPGA, reconfigurable analog blocks and an 8051 microprocessor core. The device is targeted at reducing the design time for systems comprising digital, analog and software components. The analog blocks on the chip each contain four channels with programmable settings for gain, filtering and comparison. A data-conversion block contains Analog to Digital and Digital to Analog converters with reconfigurable resolution. A routing network was provided for the analog systems. The interface between analog and digital systems allows outputs from the ADC blocks and comparators to tie into the digital routing networks, and the outputs of the FPGA can drive the inputs of the DAC blocks. In addition to these interactions, signals within the analog block can be read by the microprocessor through the ADC. This design features a second set of circuit configuration memory which can be used to instantaneously reconfigure all or part of the device by issuing a command to the microprocessor.

4.3. Commercial ICs

Several commercial ICs are of interest in our discussion of FPAA building blocks. They include a

simple set of analog building blocks and flexible interconnect on a single chip, simple programmable analog components such as digital potentiometers, programmable amplifiers and filters, and more highly integrated systems for multi-channel analog control, signal conditioning, and data acquisition applications. We begin by discussing the GAP-01, followed by programmable analog components, leading up to the first modern programmable analog integrated circuits available commercially.

4.3.1. GAP-01. The GAP-01 [72] shown in Fig. 13, released in the early 1980s by Precision Monolithics Inc., was an early attempt by industry to monolithically implement a set of analog building blocks that could be structurally and parametrically configured to implement different applications. The building blocks available on this IC included two transconductance amplifiers, the outputs of which could be selectively connected, in a patented arrangement [73], to a single output buffer by means of a pair of on-chip, digitally-controlled low-glitch current-mode switches. The integration of digitally-controllable interconnect and the use of special circuit techniques to compensate for switch non-idealities mark important achievements in the evolution of field-programmable analog ICs. An uncommitted com-

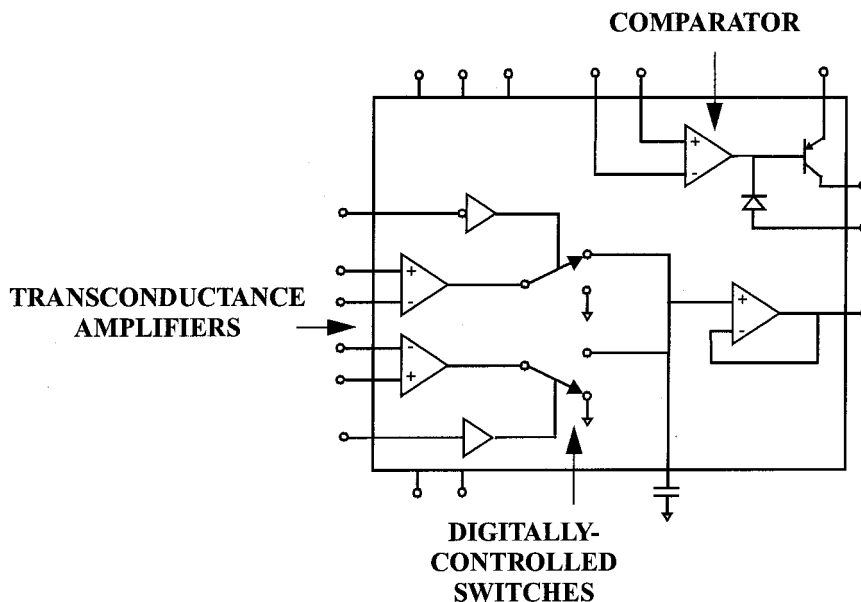


Fig. 13. The GAP-01 General Analog Processor (from [72]).

parator was also available, with its high-level output voltage parametrically set by the use of external resistors. The GAP-01 datasheet cites applications such as a two-channel sample-and-hold amplifier, an absolute value amplifier and a successive-approximation analog-to-digital converter.

4.3.2. Digital Potentiometers. Also relevant to our discussion of programmable analog circuits are digital potentiometers (Fig. 14). Xicor [74] introduced this type of ICs in 1990. Intended to replace manual potentiometers in circuits that require trimming, these ICs come in $1\text{ k}\Omega$ and $10\text{ k}\Omega$ sizes, with the wiper position controlled by a digital UP/DOWN counter which, in turn, is controlled by a human-push-button interface. Wiper positions can be changed in linear or logarithmic steps. Non-volatile EEPROM storage is available to retain the wiper position.

Analog Devices family of digital potentiometers [75] are designed for control by digital circuitry. A 3-pin serial interface loads an 8-bit number to set the wiper position of $10\text{ k}\Omega$, $50\text{ k}\Omega$ or $100\text{ k}\Omega$ potentiometers. These devices have a bandwidth of 600 kHz , and can be used to implement programmable filters and time constants as well as in circuit trimming applications.

Efforts in the development of such integrated circuits will bring commercial products that add digital programmability to analog circuits at the board level, and will result in improved integrated circuit implementations of analog circuit components, programmable over a large dynamic range, that will be essential for the design of future FPAA and FPMA ICs.

4.3.3. Programmable Gain Amplifiers. Burr Brown makes a digitally-programmable instrumentation amplifier [23], using two configuration bits to vary the gain in decade (1, 10, 100, 1000) or binary (1, 8, 64, 512) steps for applications in data acquisition and instrumentation. The gain is set by a resistor network with resistors selected by switches placed in series with the high-impedance amplifier inputs, minimizing gain errors due to the switch ON resistance. To minimize gain errors due to resistance variations with temperature, the resistor network is fabricated on a separate substrate from the amplifiers. The 3 dB bandwidth of the instrumentation amplifier varies inversely with the gain setting, between 2.4 kHz and 500 kHz .

Analog Devices manufactures a high-bandwidth

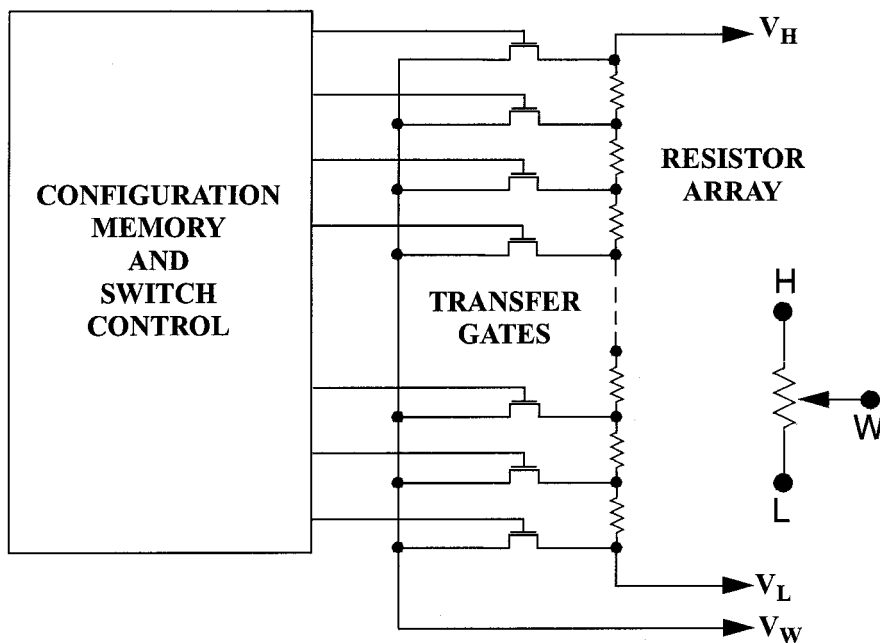


Fig. 14. Block diagram of a digital potentiometer (from [74]).

variable gain amplifier [22], for RF/IF and video automatic gain control and measurement applications. This device consists of a variable-attenuator input stage implemented as a seven-stage R-2R resistor ladder, followed by a fixed gain negative feedback amplifier. The attenuation between tap-points on the R-2R ladder is 6 dB; a proprietary circuit technique is used to interpolate continuously between tap-points based on a control voltage input.

4.3.4. Programmable Filters. To demonstrate some of the work in this area, we present two commercial approaches to programmable filter design from the numerous relevant publications, products and patents in the area.

The Universal Active Filter [24], manufactured by Burr-Brown consists of a biquad section built out of opamps and on-chip resistors and capacitors. A few off-chip resistors are required to use this device to implement Butterworth, Chebyshev and Bessel all-pole filters. An uncommitted opamp on the chip allows implementation of other filter topologies such as the Inverse-Chebyshev. A CAD tool solves filter design equations to calculate the values of the external components and display filter performance specifications. Continuous-time filters with up to 100 kHz bandwidth can be implemented using this chip.

A versatile continuous-time programmable filter manufactured by IMP for applications in the read channel circuits of magnetic tapes and disk drives is described in [25]. The filter architecture was composed of four independently programmable cascaded sections. Two were first order sections and the other two were second order sections. The RC time constants of the opamp integrators in the filter sections were implemented using oxide capacitors and triode-region MOSFETs. An automatic tuning circuit used a phase locked loop and an external frequency reference signal to set the frequency of an internal oscillator. The voltage thus developed on the gate of a triode-region MOSFET in the oscillator was then used to bias the MOSFET in the filter so that the filter cutoff frequency was set to a digitally-programmable fraction of the input reference frequency. A set of 8-bit R-2R ladder DACs allowed further control of the filter transfer function. A three-wire serial interface was provided to load the 18 eight-bit digital configuration registers that program the filter. The cutoff frequency of each section was programmable from 100 kHz to 4 MHz.

4.3.5. Texas Instruments Analog Interface Chip. TI offers a reconfigurable Analog Interface Chip (AIC) in the TLC3203X/4X [76]. The IC functions as the analog front/back end interface to a DSP in applications such as modems, speech processing, industrial process control and biomedical applications. A continuous-time anti-aliasing filter precedes the switched capacitor analog circuitry. The gain of the analog pre-amplifiers can be varied by changing the bit pattern in a control register, effecting software controlled signal conditioning. Digitally controlled analog multiplexers handle multi-channel operation of the device. Reconfigurable analog circuitry is also used to add testability to the chip; a loopback feature connects the analog output to the analog input. Under the control of a DSP, digital words can then be loaded into a register, converted to an analog signal by the on-chip DAC, then reconverted to digital form by the ADC for comparison to the original words to verify operation of the converters.

4.3.6. IMP Switched-Capacitor FPAA. In 1994, IMP Inc. introduced the 50E10 Programmable Analog Signal Conditioning Circuit (Fig. 15), the first IC in their series of Electrically Programmable Analog Circuit (EPAC) devices [13,32,77]. Aimed at multi-channel analog signal conditioning applications that require channel-dependent signal scaling and offsets, the 50E10 has an analog multiplexer front end, variable offset and gain modules, a summing amplifier and output blocks that can be configured as comparators, amplifiers or sample and hold circuits. Virtually all the analog blocks on the IC employ switched-capacitor circuits and on-chip anti-aliasing input filters and output filters are included in input and output blocks. An uncommitted opamp is provided for wiring into the circuits using external connections. On-chip EEPROM is available to store user-programmable circuit configurations. In-system reprogramming of the chip is also supported.

Possible applications of this device are sensor signal conditioning, process control, data logging, DSP front ends and test equipment. At unity gain, the chip's opamps support a stable, large-signal bandwidth of 15 kHz with the internal antialiasing filters turned on. The design goal for the EPAC was to sacrifice circuit configuration flexibility in favor of performance and ease-of-use of the device within the targeted application area. In particular, the design seeks to insulate users from analog integrated circuit

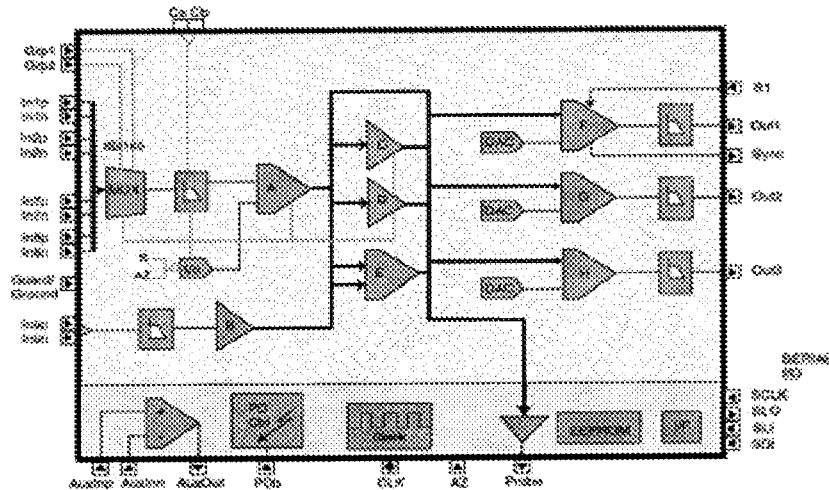


Fig. 15. Block diagram of the IMP EPAC 50E10 (from [32]).

design issues of temperature matching, offset-cancellation, parasitic coupling, loading effects, gain-bandwidth trade-offs, stability and power management. Limiting the range of circuit topologies that could be implemented in the device allowed optimization of building block and interconnect characteristics to achieve the above goals. A PC-based CAD tool is used for schematic entry, configuration bit generation and programming of the EPAC.

Follow-on products to the 50E10, with added functionality, announced recently by IMP [32] continue to target signal conditioning applications. The 50E20 Programmable Gain and Function Amplifier will add serial-output, 8-bit analog to digital conversion capability to a signal path similar to that of the 50E10, using a successive-approximation ADC. The 50E30 Programmable Monitoring and Diagnostic Data Acquisition IC will build on its predecessor with the implementation of programmable monitoring of multiple channels for threshold or window specifications, and can be set up to interrupt a microcontroller when a channel registers an error, provide a serial-output status word indicating the error channel and type, and be reprogrammed by the microcontroller to output an 8-bit measurement of the channel on which the error was detected.

4.3.7. Adaptive Logic Fuzzy Logic Controller PAIC. Adaptive Logic [6] produces the AL220 advertised as an analog microcontroller featuring a

programmable analog IC (PAIC) capability. The device operates on a set of four analog input signals, which are processed according to a set of fuzzy control rules to produce four analog outputs. The analog inputs are converted to 8-bit digital values by on-chip analog to digital converters, then processed by a digital core programmed by a 256×8 EEPROM. The 8-bit digital outputs from the core are converted to analog outputs by a digital to analog converter followed by a sample and hold circuit. Fig. 16 shows a block diagram of signal flow in the PAIC. The maximum processing speed of the digital core is limited by data sampling and processing operations to 10 kHz, at the maximum clock frequency of 10 MHz. A CAD software tool is used to convert the fuzzy control rules to a bit stream which configures the device. Applications in fuzzy logic control are demonstrated for this IC in [6].

4.3.8. Zetex TRAC. The first commercial continuous-time FPAA was announced by Zetex in 1996 [62,78]. The Totally Reconfigurable Analog Circuit (TRAC) consists of 20 cascaded analog cells, each of which can be configured to implement one of six functions, namely Add, Negate, Pass, Log, Antilog, Rectify. In addition, a cell can be turned off or programmed to be a standalone op-amp for use with external components. On-chip interconnections are local only, with the output of each cell connected to the input of the next. The inputs and outputs of all cells are brought off-chip to enable global routing

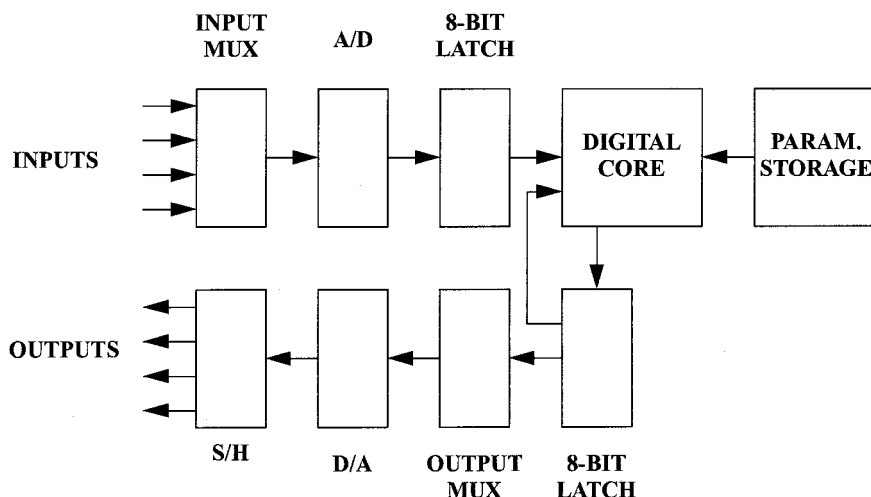


Fig. 16. Block diagram of signal flow in the Adaptive Logic PAIC (from [6]).

using external connections and/or components. A shift register provides volatile storage of circuit configuration data.

4.4. Intellectual Property Status

A review of U.S. patent literature in the area of programmable analog and mixed signal circuits reveals several patents, indicating significant commercial potential in this area. As early as 1977, a patent was granted for a digitally controlled variable conductance [79], composed of a fixed resistor in parallel with a series combination of another fixed resistor and a MOS transistor with its gate voltage controlled by a digitally controlled variable duty cycle generator. The low-glitch current-mode switch employed in the Precision Monolithics GAP-01 [72], was patented in 1981 [73]. In 1987, Czarnul was granted a patent [80], for the MOS Transconductor, a field-programmable conductance element used in [53] and in other applications such as programmable filters. In an arrangement which might be applied to FPAA's, analog standard cell methodologies or analog metal-masked arrays, Kabushiki Kaisha Toshiba's 1994 patent [45] describes a scheme for constructing standard cells from existing analog integrated sub-circuits and standard input-output interfaces which allow different analog subcircuits to be interconnected with standard DC bias and signal peak-to-peak levels.

Pilkington Micro-Electronics' 1993 patent [21] describes the design of an FPAA consisting of an array of operational amplifiers, programmable resistors constructed from multiple pairs of complementary MOS transistors and programmable capacitors with their range extended, at the expense of Q-factor, by an impedance-multiplication technique. The architecture described in this patent, along with switched-capacitor circuit techniques described in a 1994 UK patent [61], forms the basis of the PMeL-Motorola FPAA and FPMA designs. Kawasaki Steel describes, in a 1994 patent [81], an FPAA design consisting of operational amplifiers, passive resistor and capacitor elements interconnected with pass transistors. The intellectual property in this field continues to grow. Analogix [10], has a patent application pending for their bipolar FPAA design, as does Xicor, for their non-volatile digital potentiometer [74].

One of the first steps towards the evolution of an FPMA can be found in a 1992 Actel patent [82], that describes a user-programmable integrated circuit with configurable analog and digital circuit modules and interconnection networks and programmable ADC and DAC interface blocks. Patents granted to AMD in 1992 and 1993 [83,84], describe two types of PLAs in which an analog front-end or a back-end is married with a programmable logic array. A programmable mixed analog-digital, multi-channel signal-conditioning integrated circuit is patented by Hewlett-Packard [85], for applications in biomedical measurement.

4.5. FPAA/FPMA Status

The status of major research and commercial works in the area of FPAAs and FPMAs is summarized in Table 1. A timeline depicting the sequence of important achievements in the area of programmable analog circuits is shown in Fig. 17.

5. Conclusions and Future Work

The evolution of user-discretionary analog systems has shown notable progress in the last five years. While it is still relatively young compared to the

digital FPGA industry, a survey of the area of programmable analog integrated circuits from historical and current perspectives has shown it to be active and diverse. Several indicators point to continued progress and development, namely the emergence of special sessions on FPAAs in conferences on programmable devices, the existing portfolios and continued assembly of intellectual property in the area by several corporations, the packaging of analog design software with an associated FPAA IC in the recent IMP and Zetex products, an FPGA industry with an expanding financial base searching for product differentiation, the trend in the IC industry towards complete systems on a chip, and increasing

Table 1. Status of Field-Programmable Analog and Mixed-Signal Integrated Circuits.

Group	Circuit Technology	CAB Verified	Intercon. Verified	Applic. Verified	CAD Tool	Patent Issued	Product Available	FPMA Extension
Vallancourt & Tsividis 1987 [5] (Columbia)	Sampled-signal z-domain filters	✓	✓	✓				
Sivilotti 1988 [19] (Caltech)	Subthreshold		✓					
Lee & Gulak 1990 [16] (Toronto)	Subthreshold	✓	✓	✓				
Lee & Gulak 1992 [8] (Toronto)	Linear	✓	✓	✓	✓			✓ [66]
Pierzchala & Perkowski 1994 [10] (Portland State)	Linear	✓						
Chang et al. 1994 [9] (Nottingham)	Linear	✓						
Chang et al. 1996 [7] (Nottingham)	Switched-current	✓						
Premont et al. 1996 [11] (Cimirly Lyon)	Current conveyor	✓	✓	✓				✓
Embabi et al. 1996 [12] (Texas A&M)	Current integrator	✓	✓	✓				
Pilkington–Motorola 1993 [21]	Switched-capacitor	✓			✓	✓		✓
Kawasaki Steel 1994 [81]	Linear					✓		
IMP 1994 [77]	Switched-capacitor	✓	✓	✓	✓		✓	
Zetex 1996 [78]	Linear	✓	✓	✓	✓		✓	

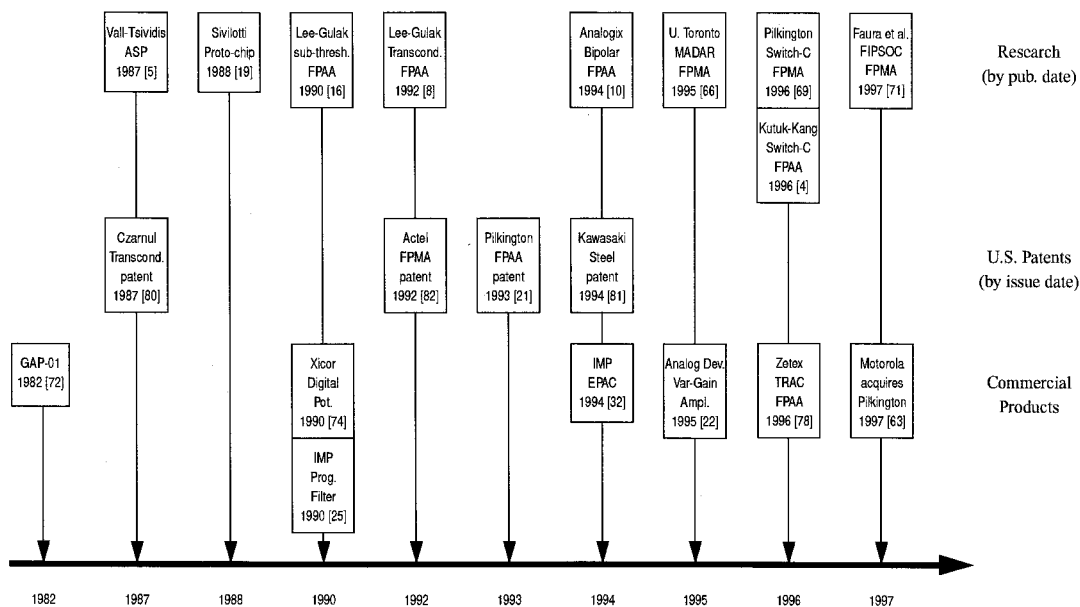


Fig. 17. Timeline marking important milestones in the field of FPAA/FPMA.

time-to-market pressures now universally exerted on product developers. The acquisition of PMeL by Motorola, and its announcement of plans to release FPAA and FPMA IC products further indicates the commercial potential of this field.

Several developments can be expected in the future. Present switched-capacitor techniques show good promise for applications below 1 MHz; this and other sampled data techniques can be expected to yield programmable analog and mixed-signal applications in lower bandwidth applications such as measurement, monitoring and control. In the longer term, it is conceivable that switched-capacitor techniques might support applications up to 10 MHz. The use of stochastic signal processing techniques on a Pulse Density Modulated (PDM) representation of analog signals might lead to some interesting implementations for low-frequency applications in measurement and monitoring. As demonstrated in [86], a PDM bit-stream produced using Sigma-Delta modulation analog to digital conversion can be processed using stochastic or deterministic methods that require simple digital hardware, and reconfigurability can be achieved using a digital FPGA.

For higher frequency applications, for example processing of video bandwidth signals, existing continuous-time techniques will need to be improved

by the development of high-performance reconfigurable analog circuit designs, like the reconfigurable opamp/differential difference amplifier in [87]. Improved architectures and implementations of FPAA interconnect will be especially important in this respect.

Future developments in both analog and digital integrated circuit memory will improve the density and performance of FPAA. Circuit configuration and component parameter storage occupies a significant percentage of FPAA area, and the accuracy of circuit component values requires analog memory or precision sample and hold amplifiers with accuracies greater than ten bits. The area of ferroelectric memory shows promise for non-volatile memory at densities competitive with DRAM, and requires simpler IC processing steps and programming techniques than flash memory. Current research in the area [88] is addressing multiple valued ferroelectric memory.

A tighter coupling of FPAA to digital structures is already evident in the evolution of the IMP EPAC devices [32]. This can be expected to continue to address interfacing of these devices to microcontrollers and monitoring systems, as well as for providing Built In Self Test (BIST) and calibration features to analog circuits. Adaptive operation, whereby a device reconfigures itself on the fly as

different functions are required, might also be attempted as has been done with digital FPGAs [89,90]. Field-programmable mixed-signal systems might also be implemented by coupling FPGA and FPAA ICs at the Multi-Chip Module or Printed Circuit Board levels. Research is necessary in the area of mixed-signal arrays, to determine circuit resources for FPMAs, particularly for the interface between analog and digital converters. Reconfigurable data converters [66,91] will be important in this respect.

Specifications for current FPAA designs have been mostly in the form of the publication of performance numbers for CABs or programmable circuit elements. Some works have addressed the issue of interconnect by looking at parasitic effects, but as yet no standards have emerged for succinct methods of describing pin-to-pin performance. An exception to this has been restricted architecture programmable circuits such as the IMP EPAC devices [32], where all possible circuit configurations can be predicted and worst case specifications determined. A useful design aid would be a software program that understands the parameters and interactions of CABs and interconnect, and can predict performance for the embedding of a circuit on a target FPAA from the configuration data.

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