

## 8.4 A 13.3Mb/s 0.35 $\mu$ m CMOS Analog Turbo Decoder IC with a Configurable Interleaver

Vincent C. Gaudet<sup>1</sup>, P. Glenn Gulak

University of Toronto, Toronto, Canada

<sup>1</sup>now with University of Alberta, Edmonton, Canada

Due to their impressive error correcting capabilities at low signal-to-noise ratios (SNR), turbo codes [1] are being introduced into several new data communications standards (3GPP, DVB-RCS, DVB-RCT). However, digital turbo decoders [1-3] potentially suffer from long latencies and high power consumption. This paper demonstrates for the first time the feasibility of an all-analog turbo decoder that includes constituent interleavers, as a method for reducing receiver power consumption.

Analog decoders eliminate the need for high-speed A/D converters (ADC) in a receiver; instead, they use analog input signals, and produce digital output signals by using comparators which operate at the information symbol rate as opposed to the coded symbol rate required by ADCs. A recent all-analog soft decoder IC [4] implements an entire 2-state tailbiting maximum a posteriori (MAP) trellis in silicon. This work extends the notion of analog decoding to a full turbo decoder constructed using two 4-state MAP decoders and a fully programmable analog interleaver/deinterleaver. A system block diagram in Fig. 8.4.1, show the interconnections between the two MAP decoders, the interleaver (II), and deinterleaver (II<sup>-1</sup>).

Each analog log-domain MAP decoder is constructed using the two circuit building blocks depicted in Fig. 8.4.2. The first, in Fig. 8.4.2a, realizes the  $\text{MAX}^*(x, y) = \ln(e^x + e^y)$  state metric function, when M3 and M4 are in weak inversion; in moderate inversion, the function is slightly distorted incurring a penalty of around 0.1dB, but with better device matching properties. Branch metrics are generated using differential pair transconductors, depicted in Fig. 8.4.2b, which use differential channel input voltages to produce differential output currents. These are summed onto the  $\text{MAX}^*$  pull-up transistors M1 and M2 operating deep in the triode region. The differential pairs from Figure 8.4.2b are also used to propagate state metric outputs from the  $\text{MAX}^*$  circuits to subsequent trellis stages. Figure 8.4.3 shows a trellis stage for one direction of recursion for a (7,5) recursive systematic convolutional (RSC) code constructed using the  $\text{MAX}^*$  and differential circuits. A total of 104 MOS transistors are used for the stage, occupying 120x70 $\mu\text{m}^2$  in a 0.35 $\mu\text{m}$  1P3M CMOS process.

An analog interleaver spatially permutes soft outputs from one MAP decoder for input to the other MAP decoder. A configurable interleaver, where a desired permutation is programmed at power-up to accommodate different standards, is built using a network of crossbars. Figure 8.4.4 illustrates such an interleaver of size 16 constructed with twelve 4-input crossbars, each programmed using a serial shift register. Two differential signals are routed for every bit position, thus combining the interleaver and deinterleaver into one unit. The interleaver does not present a performance barrier for current turbo decoding applications. Since the pass transistors implement a passive routing network, only minimal power is consumed by the interleaver.

An input demultiplexer sample-and-hold unit stores a serial input stream of noisy channel values represented as voltages onto a bank of capacitors. Each capacitor is directly connected to a branch metric transconductor. Decoding is performed in three steps. First, an entire codeword is stored using the demultiplexer,

taking time  $t_{\text{STO}}$ ; then, the turbo decoder feedback loop is opened for a short period of time  $t_{\text{RST}}$  to reset the second MAP's soft information to zero. Lastly, a continuous-time iterative decoding step is performed by closing the feedback loop for time  $t_{\text{ITER}}$  and allowing the network to settle to its final output values. Hard decisions are made on soft output values using a bank of output comparators.

A block diagram of an analog turbo decoder for a rate 1/3 code with 16 information symbols and (7,5) RSC encoders and a configurable interleaver/deinterleaver is shown in Fig. 8.4.5. Trellises are left unterminated. A die microphotograph of a 0.35 $\mu\text{m}$  CMOS implementation of the decoder is shown in Fig. 8.4.6. The pad-limited IC occupies 2691x2681 $\mu\text{m}^2$ , whereas, the core occupies 1131x1258 $\mu\text{m}^2$ . Each MAP decoder occupies 1131x483 $\mu\text{m}^2$  and the interleaver/deinterleaver occupies 525x265 $\mu\text{m}^2$ .

Testing is performed using an HP75000 tester, which presents channel test vectors to a bank of six D/A converters connected to the IC's inputs. Test vectors are generated in software with a precomputed noise component calibrated to specific SNRs. Test chip outputs are recorded and compared to noiseless reference values in software in order to generate measured bit error rate (BER) curves.

The IC is tested at a bit rate of 13.3Mb/s, with  $t_{\text{STO}} = 800\text{ns}$ ,  $t_{\text{RST}} = 150\text{ns}$ , and  $t_{\text{ITER}} = 250\text{ns}$ , and 16b codewords. The decoding latency is 1.2 $\mu\text{s}$ . With a 3.3V supply, the decoder has a power consumption of 185mW, resulting in an energy consumption per decoded bit of 13.9nJ. Figure 8.4.7 shows an oscilloscope capture of the hard output of bit position 15, and of the reset signal, which opens the turbo feedback loop before each codeword is decoded. Figure 8.4.8 presents the BER curves for the measured output of a single MAP decoder and of the turbo decoder, contrasted to a simulated floating-point digital decoder. The 1.1dB loss from ideal turbo decoding is explained by less than perfect open-loop operation during the first decoding phase  $t_{\text{RST}}$ , where old soft values are injected into the feedback loop. The programmable analog interleaver is verified by testing BERs using several different reference permutations. Decoding speed can be increased to 40Mb/s at a similar power consumption by expanding the input demultiplexer to include a swinging buffer, thus reducing the energy per decoded bit by two-thirds.

With this technique, it is expected that decoding latency will remain relatively constant with increased block size, resulting in both a near-linear increase in throughput versus block length and relatively constant energy per decoded bit. Mismatch simulations indicate near-ideal performance for cases where local matching is good and global matching is poor; however, the degradation worsens as block length increases. Future research to extend practical block sizes beyond several hundred information bits is anticipated.

### Acknowledgments

Funding is acknowledged from the Natural Sciences and Engineering Research Council of Canada and from the Canadian Microelectronics Corporation.

### References

- [1] C. Berrou et al., "An IC for Turbo-Codes Encoding and Decoding," ISSCC Digest of Technical Papers, pp. 90-91, Feb. 1995.
- [2] M. Bekooij et al., "Power-Efficient Application-Specific VLIW Processor for Turbo Decoding," ISSCC Digest of Technical Papers, pp. 180-181, Feb. 2001.
- [3] M. Bickerstaff et al., "A Unified Turbo / Viterbi Channel Decoder for 3GPP Mobile Wireless in 0.18 $\mu\text{m}$  CMOS," ISSCC Digest of Technical Papers, pp. 90-91, Feb. 2002.
- [4] M. Moerz et al., "An Analog 0.25 $\mu\text{m}$  BiCMOS Tailbiting MAP Decoder," ISSCC Digest of Technical Papers, pp. 356-357, Feb. 2000.

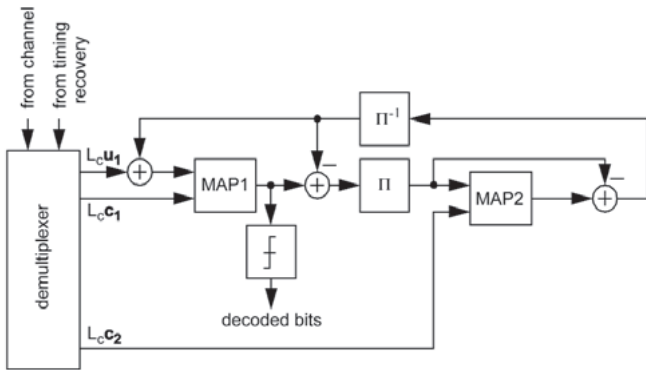


Figure 8.4.1: Turbo decoder system block diagram.

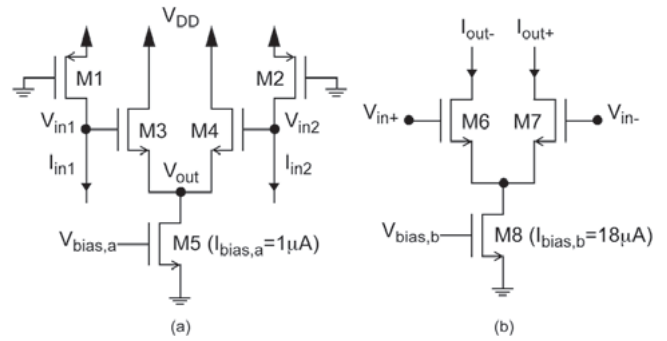


Figure 8.4.2: (a) MAX\* circuit (b) Transconductor.

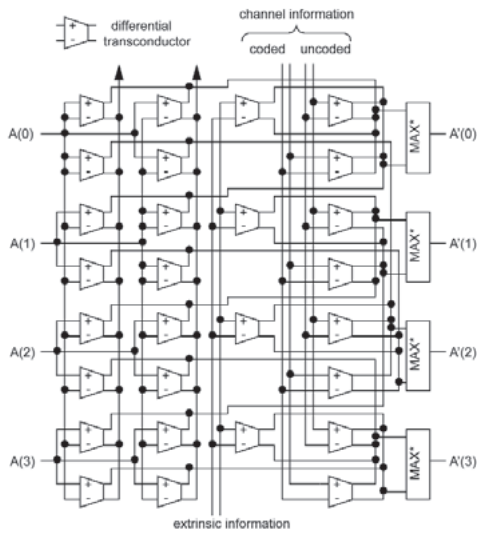


Figure 8.4.3: Trellis stage.

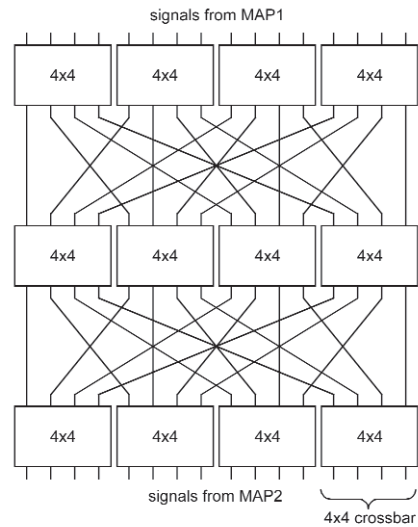


Figure 8.4.4: Size 16 interleaver.

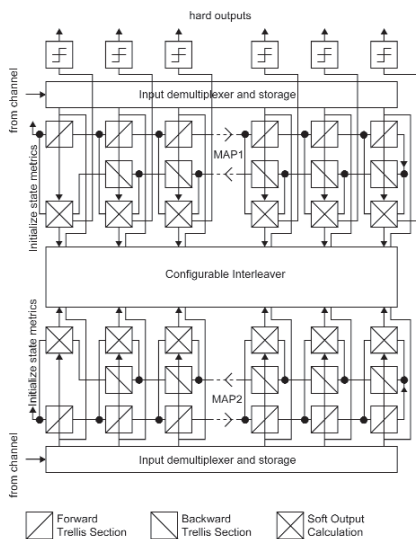


Figure 8.4.5: Block diagram of analog turbo decoder.

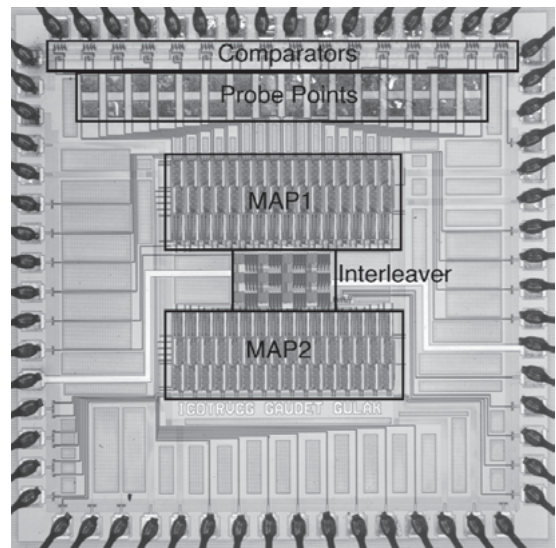


Figure 8.4.6: Die micrograph and floorplan.

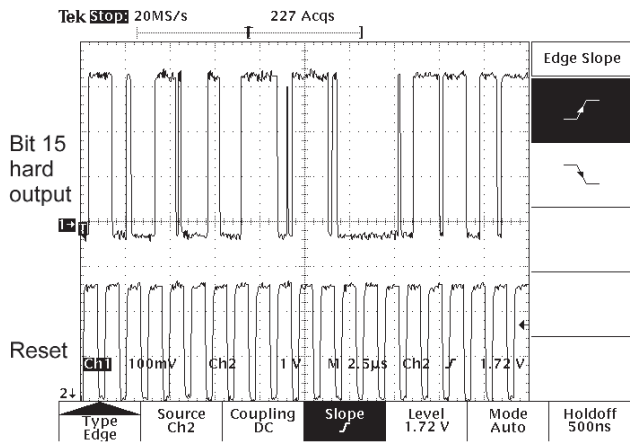


Figure 8.4.7: Measured Bit 15 (top), Reset (bottom).

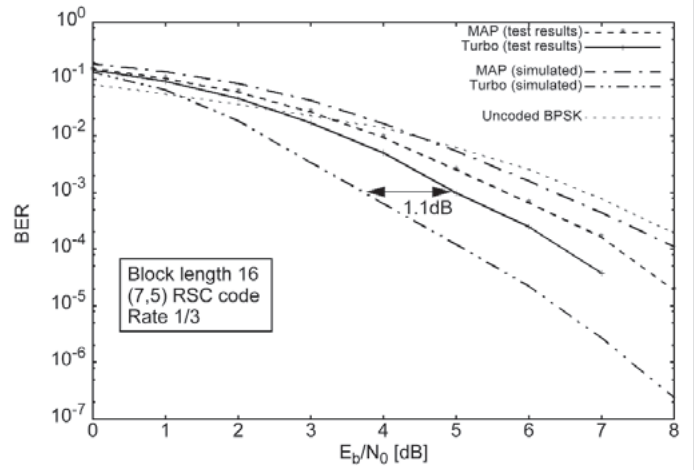


Figure 8.4.8: Measured BER for analog turbo decoder.

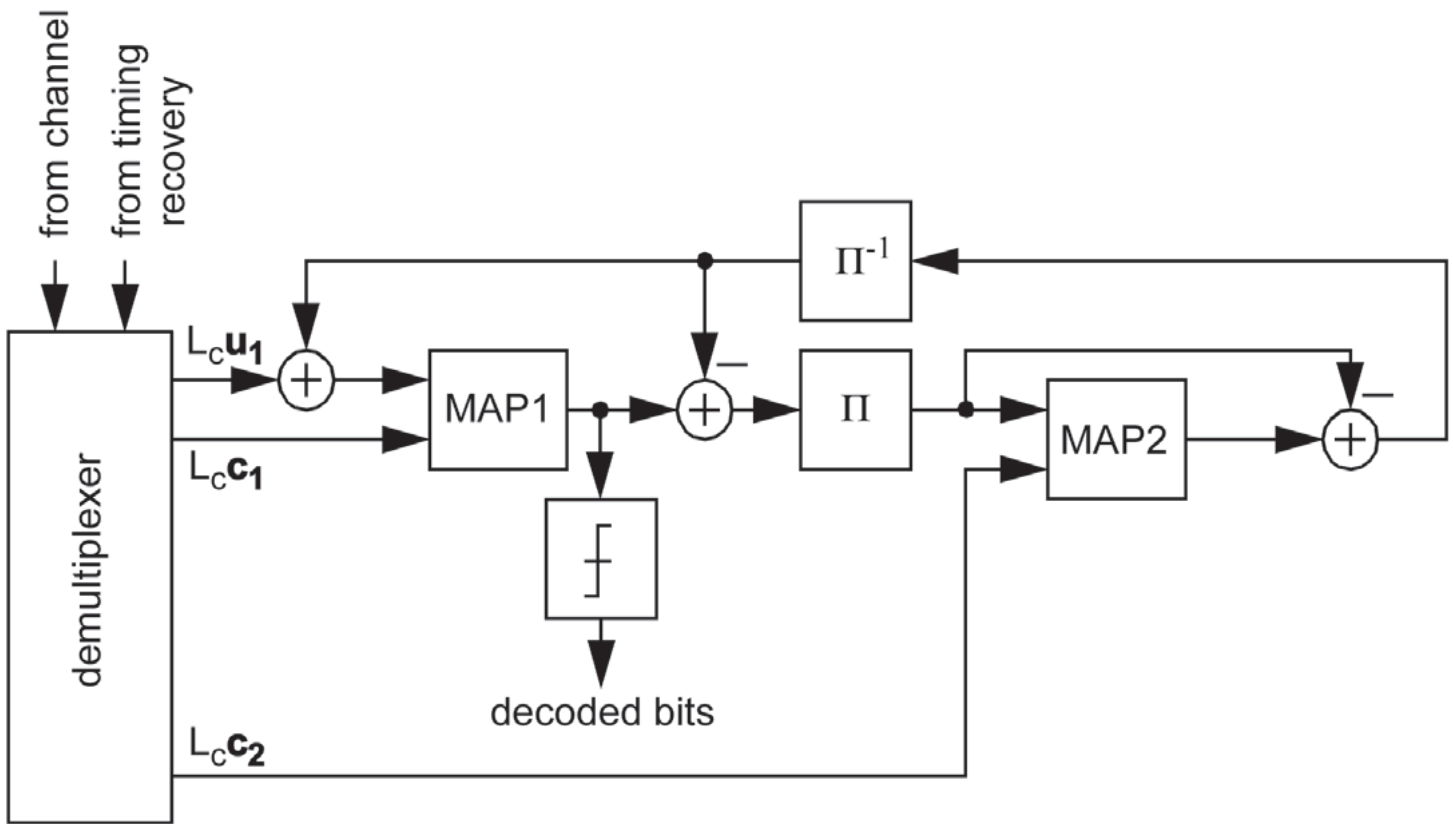
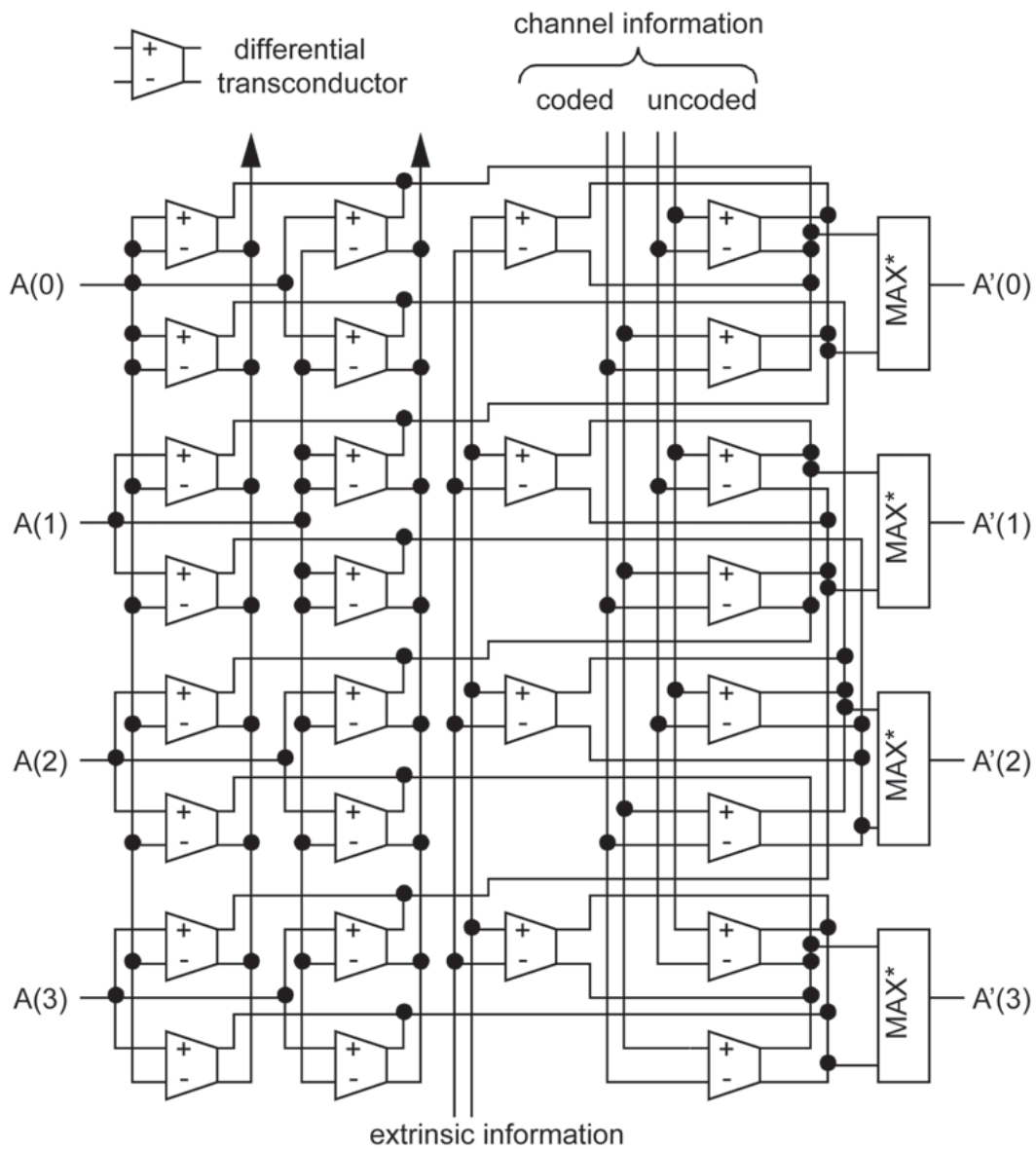
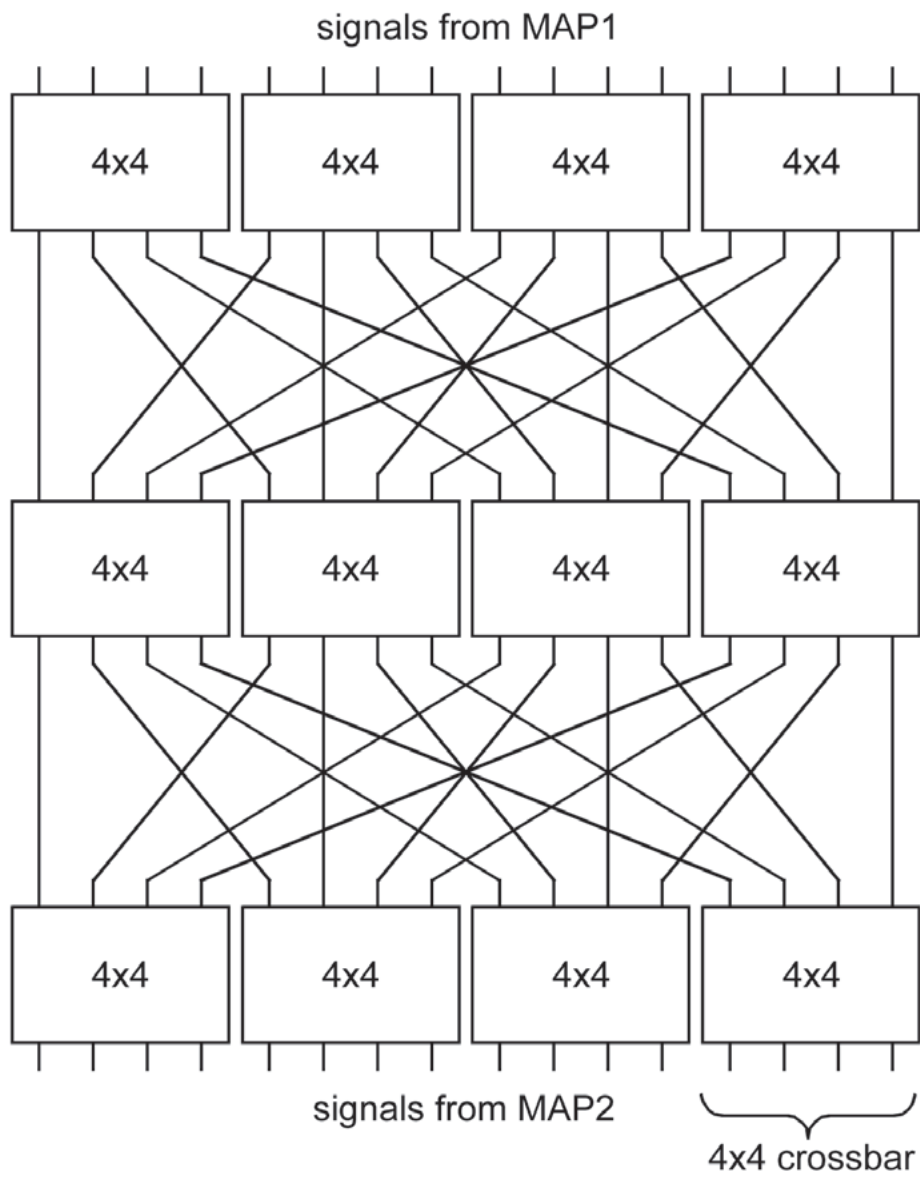


Figure 8.4.1: Turbo decoder system block diagram.

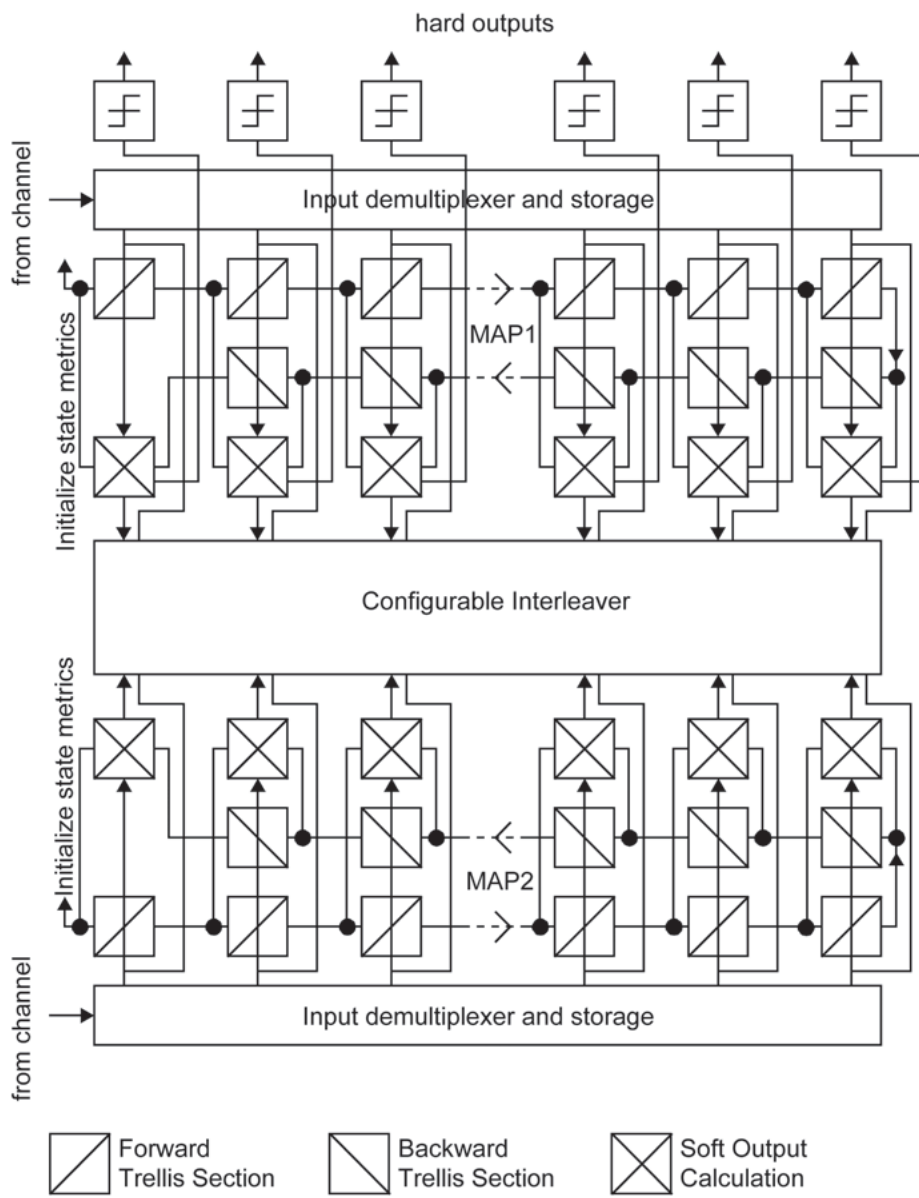




**Figure 8.4.3: Trellis stage.**



**Figure 8.4.4: Size 16 interleaver.**



**Figure 8.4.5: Block diagram of analog turbo decoder.**

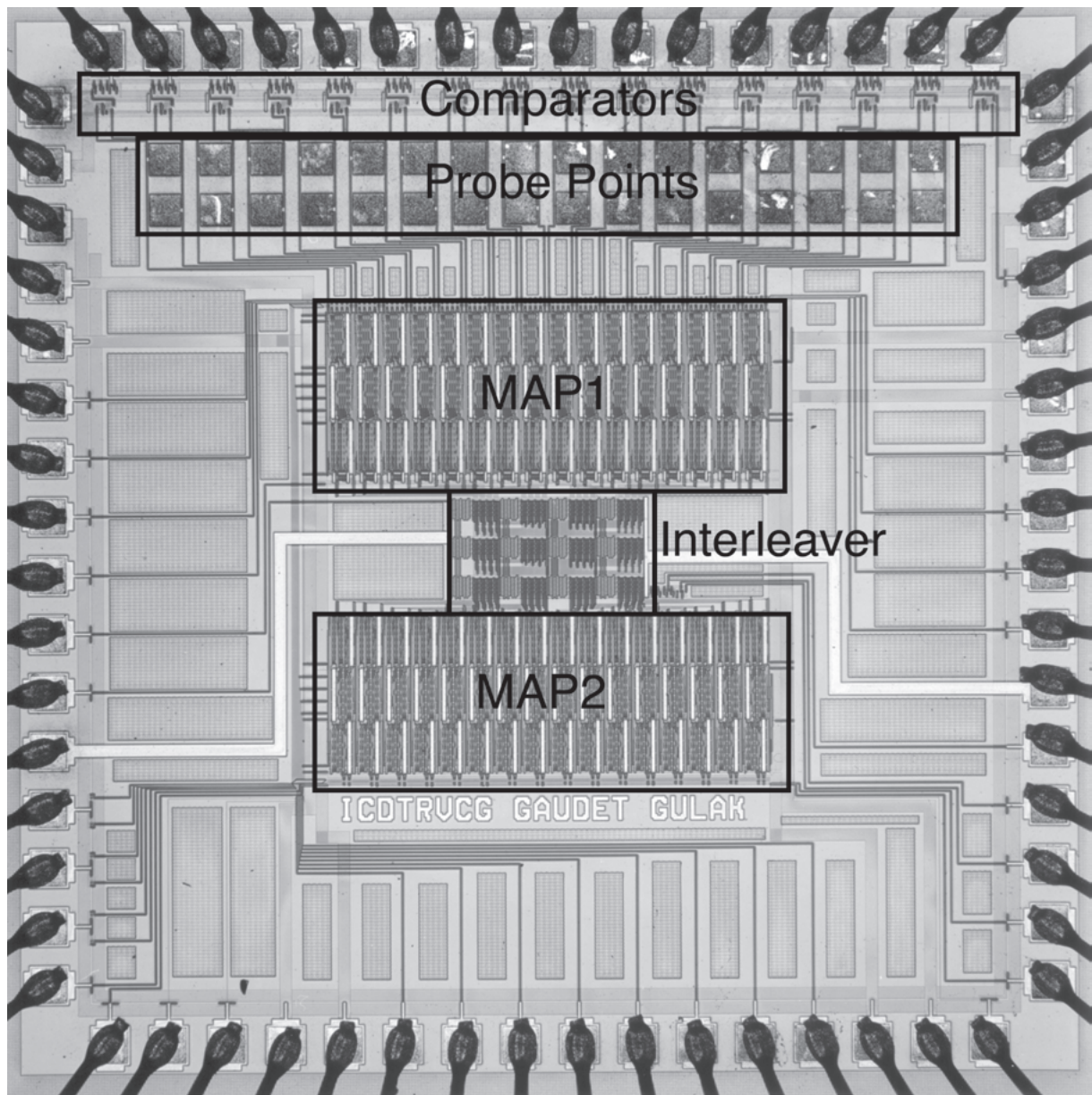


Figure 8.4.6: Die micrograph and floorplan.

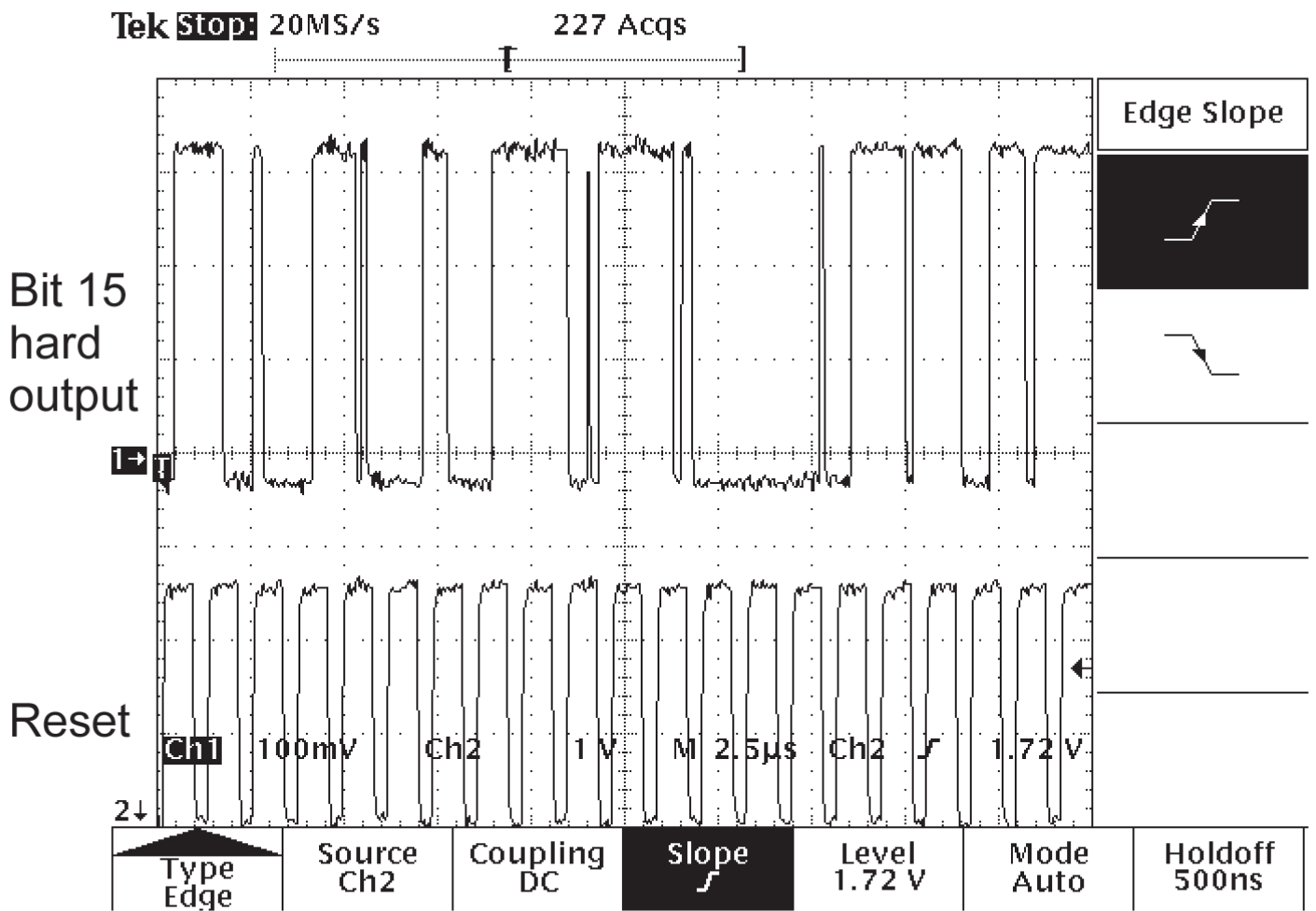


Figure 8.4.7: Measured Bit 15 (top), Reset (bottom).

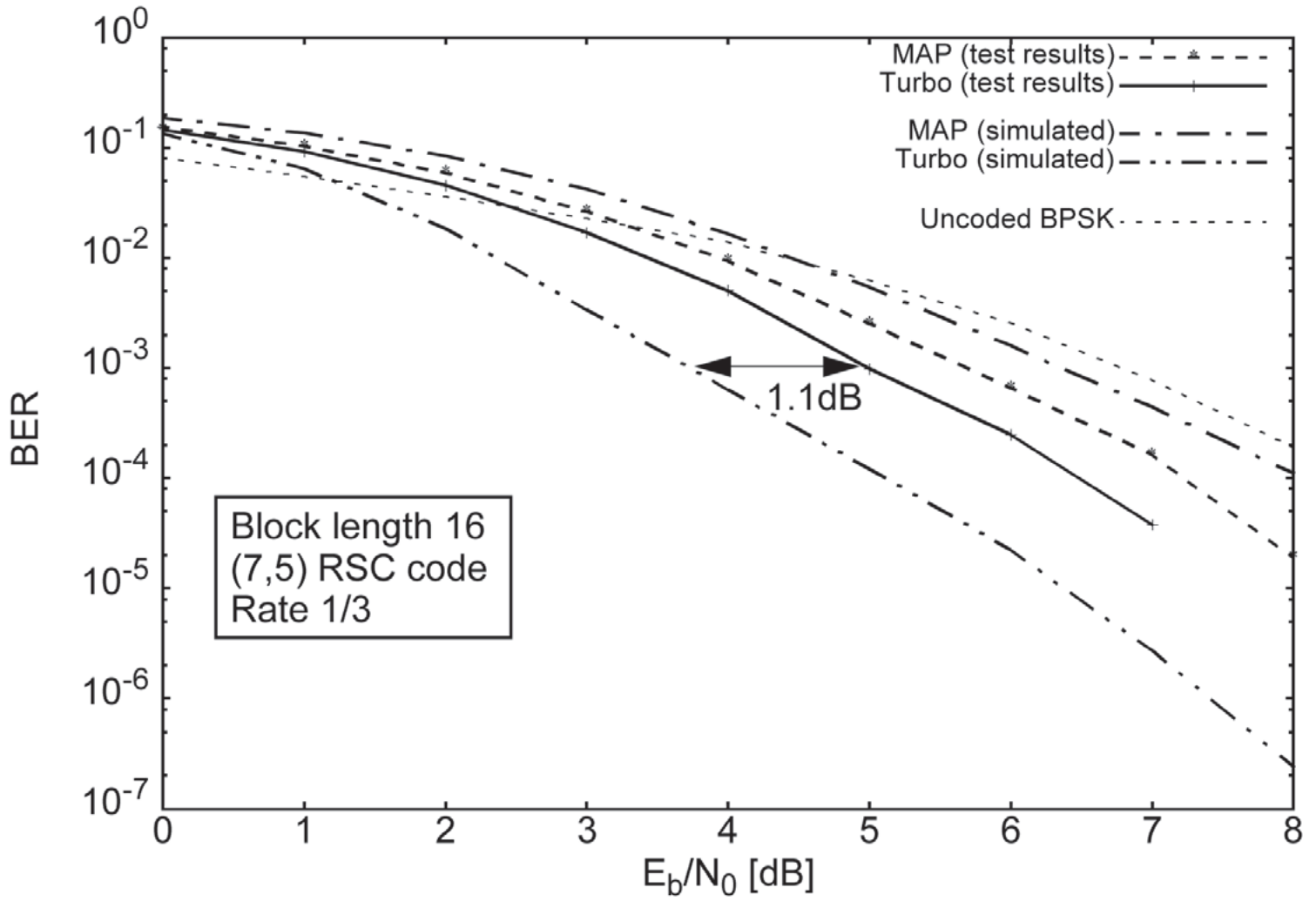


Figure 8.4.8: Measured BER for analog turbo decoder.