

# A Review of Multiple-Valued Memory Technology

(invited Paper)

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## Abstract

*This paper provides a brief overview of semiconductor memory design from the perspective of the impact multiple-valued circuit techniques are making on modern day implementations. The focus is primarily on CMOS-related technologies.*

## 1. Introduction

It has been estimated that more than  $10^{17}$  CMOS transistors are fabricated worldwide each year and 50% of these transistors are utilized in some type of memory structure. As an example, it is not uncommon for modern-day workstations to contain 128MBytes (i.e.,  $10^9$  bits!) of semiconductor memory. In addition, more than half of the transistors in today's high-performance microprocessor ICs are devoted to cache memories. Obviously, dense, high performance memory circuits are of primary concern to today's semiconductor design engineers.

The basic differences in function found in semiconductor memories have come about as a result of the specific systems requirements in which they are used. Functional characteristics of interest include data access restrictions, read/write speed, memory density, power dissipation, and volatility (i.e., whether data is maintained in the memory array when the power supply is turned off). There are several major types of semiconductor memories that can be classified according to their differing characteristics, relative to the above parameters, as illustrated in Table 1 below.

Application areas that consume large amounts of memory include microprocessors and computer main memory systems as mentioned above. In addition, other high volume application areas are video processing and graphics subsystems, HDTV frame buffers, smart cards, automotive electronics, and test equipment, to name just a few. As semiconductor technology proceeds toward system-on-a-chip capability, we can expect ASIC memory blocks to become an increasingly important part of the

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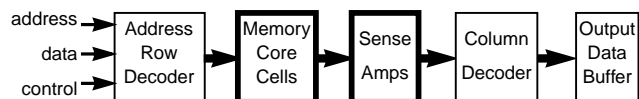
Non-Volatile		Volatile	
Write Once	Multiple-Write	General Purpose	Specialty
ROM (mask)*	EPROM	SRAM	FIFO (shift register)
PROM (fuse)	E <sup>2</sup> PROM	DRAM *	LIFO (stack)
	Flash*		SIPO/PISO
	Ferroelectric*		CAM*

\* MVL circuits and systems proven

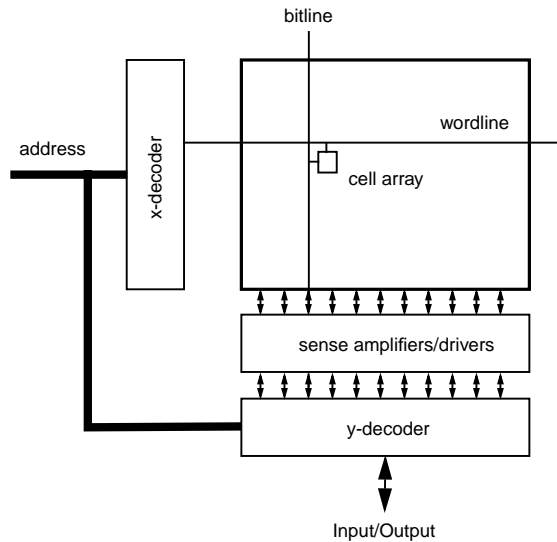
**Table 1: Semiconductor Memory Classification**

overall monolithic implementation.

Despite the varied types and applications, all semiconductor memories today are conceptually organized in very similar ways. All memories have a set of Address lines, Data lines and Control lines connected to the memory array. The control lines indicate the function to be performed or the status of the memory system. The address and data lines provide a mechanism for moving data and address information into or out of the memory array. Typically, the address lines would be connected to an address row decoder which would select a row of cells from an array of memory cells. The signal provided by the subset of cells is usually very weak and needs to be amplified and examined in some way to determine which one of the discrete values were stored in each of the selected cells. Often only one or a few of the subset of cells read from the array are selected by the column decoder and delivered to the data output buffer to application circuits outside the memory system. A summary of the internal address-path and data-path one would find in almost all memory systems today is presented in Figure 1. With respect to this figure, multiple-valued circuits have been successfully integrated



**Figure 1. Internal Address and Data Path of a Memory System**



**Figure 2. A Generic Semiconductor Memory Architecture**

into the Memory Core Cells and Sense Amplifier sections of several commercial memory designs, as we shall see in the sections that follow.

In order to understand the detailed operation of multiple valued memory circuits, it is instructive to stand back and consider a more detailed view of how semiconductor memories are constructed. Semiconductor fabrication technology today, and in particular CMOS technology, is a two-dimensional planar technology that allows for the placement and interconnection of transistors and wires in very dense structures with perhaps up to six metal layers for interconnection. The geometrical restrictions imposed by fabrication naturally influence the internal organization of the transistors and wire used to construct a semiconductor memory. The internal architecture of a semiconductor memory is illustrated in Figure 2. All of the essential components specified earlier in Figure 1 are present in Figure 2 but they are now arranged with the view to optimizing performance parameters such as area and speed.

A typical random access memory (RAM) architecture consists of an array or matrix of storage cells arranged in an array of  $2^N$  columns (bitlines) and  $2^M$  rows (wordlines). The rectangular arrangement allows one to adjust the length and hence the parasitic capacitance of the wordlines and the bitlines. Due to performance and packaging considerations, it is unusual to encounter aspect ratios of the memory array larger than 4:1. To read the data stored in the array, a row address is presented to the row decoder which in turn selects one wordline. All the cells along this wordline are activated and the contents of each of these cells is deposited onto each of their respective bitlines running vertically through the

array. The storage cells have traditionally only stored one bit of information and hence the term *bitlines* for the wires that carry the output values from these cells. Recently, schemes for storing more than one bit per storage cell have been developed with the result that sometimes more than one bit of information is present on a bitline despite the continued use of the term *bitline*.

The signal available on the bitlines is directed to a parallel collection of sense amplifiers. The sense amplifiers act as a buffer and decision device that provides an accurate estimate of the original contents or state of the selected memory cells. The column address is used to select a subset of sense amplifier outputs (possibly as few as one) and routes this to an output buffer that drives the result out of the memory system.

In what follows, we will review the highlights of advances in CMOS circuits for multiple-valued memories. We begin with the simplest type of memory known as a ROM and successively review more sophisticated memory designs such as Flash, DRAM, Ferroelectric and Content-Addressable memory systems that have all enjoyed the advantages of practical multiple-valued circuits.

## 2. Read Only Memory (ROM)

Read Only Memories or ROMs consist of an array of core cells whose contents or state is preprogrammed in hardware during the wafer fabrication process. The contents of the memory are therefore maintained indefinitely regardless of the previous history of the device and/or the previous state of the power supply. Semiconductor ROMs first appeared in the early 1970s as storage devices for microprogrammed code and for dot-matrix character generators used in computer CRT and television displays.

### 2.1 Core Cells

A binary core cell stores binary information through the presence or lack of a single transistor at the intersection of the wordline and bitline. ROM core cells can be connected in two possible ways: a parallel NOR array of cells or a series NAND array of cells each requiring one transistor per storage cell. The ROM cell in this case is programmed by either connecting or disconnecting the drain connection from the bitline. The NOR array is larger as there is potentially one drain contact per transistor (or per cell) made to each bitline. Potentially the NOR array is faster as there are no series connected transistors as in the NAND array approach. However, the NAND array is much more compact as no contacts are required within the array itself, however, the series connected pull-down transistors that comprise the bitline is potentially very slow.

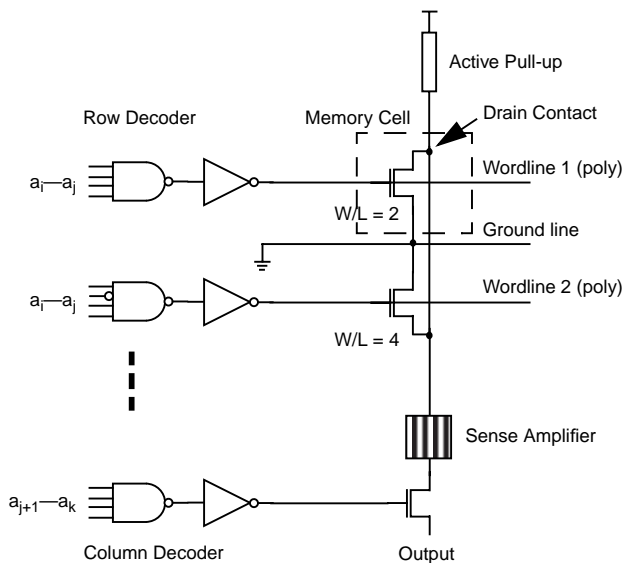
Encoding multiple-valued data in the memory array involves a one-to-one mapping of logic value to transistor

characteristics at each memory location and can be implemented in two ways: (i) adjust the width-to-length (W/L) ratios of the transistors in the core cells of the memory array or (ii) adjust the threshold voltage of the transistors in the core cells of the memory array [1].

The first technique works on the principle that W/L ratio of a transistor determines the amount of current that can flow through the device (i.e., the transconductance) and this current can be measured to determine the size of the device at the selected location and hence the logic value stored at this location. In order to store 2 bits per cell one would use one of four discrete transistor sizes. This technique was used by Intel in the early 1980's to implement high density look-up tables in its i8087 math co-processor [2]. Motorola [3] also introduced a four-state ROM cell with an unusual transistor geometry that had variable W/L devices. The conceptual electrical schematic of the memory cell along with the surrounding peripheral circuitry is shown in Figure 3.

### 2.2 Peripheral Circuitry

The four states in a two-bit per cell ROM are four distinct current levels. To determine which of the four possible current levels are generated by an addressed cell two primary techniques are possible. One technique compares the current generated by a selected memory cell against three reference cells using three separate sense amplifiers. The reference cells are transistors with W/L ratios that fall in between the four possible standard transistor sizes found in the memory array. This is illustrated in Figure 4 below.



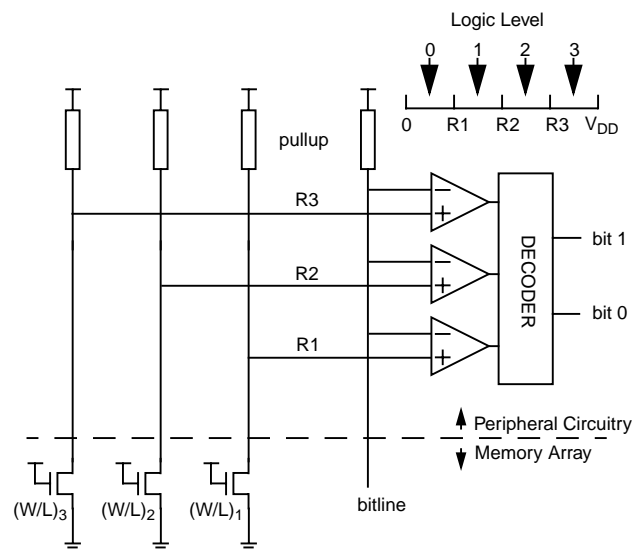
**Figure 3. Geometry-Variable Multiple-Valued NOR ROM**

The approach is essentially a 2-bit flash Analog-to-Digital (A2D) converter. An alternate method for reading a 2-bit per cell device is to compute the time it takes for a linearly rising voltage to match the output voltage of the cell. This time interval can be then mapped to the equivalent 2-bit binary code corresponding the memory contents. Other approaches can be found in [4][5].

### 2.3 Architecture

Constructing large ROMs with fast access times requires the memory array to be divided into smaller memory banks. This gives rise to the concept of divided wordlines and divided bitlines that reduces the capacitance of these structures allowing for faster signal dynamics. Typically, memory blocks would be no larger than 256 rows by 256 columns. In order to quantitatively compare the area advantage of the multiple valued approach, one can calculate the area per bit of a two-bit per cell ROM divided by the area per bit of a one-bit per cell ROM. Ideally, one would expect this ratio to be 0.5. In the case of a practical 2-bit per cell ROM [6], the ratio is 0.6 since the cell is larger than a regular ROM cell in order to accommodate any one of the four possible size transistors. ROM density in the Mb size range is in general very comparable to that of DRAM density despite the differences in fabrication technology.

In user-programmable or field-programmable ROMs, the customer can program the contents of the memory array by blowing selected fuses (i.e. physically altering them) on the silicon substrate. This allows for a “one-time” customization after the ICs have been fabricated. The quest for a memory that is non-volatile and electrically alterable has led to the development of EPROMs, EEPROMs and



**Figure 4. ROM Sense Amplifier**

Flash memories.

### 3. Flash Memory

Flash memories were originally developed [7] by Toshiba in 1984. Unlike traditional EEPROMs, “flash EEPROMs” cannot be erased at the level of granularity of bytes but rather only in large blocks (i.e., flash erase and hence the name flash EEPROM or simply flash memory). To compensate for the limitation on the granularity of memory that can be erased, the cell size and write endurance are improved relative to EEPROMs.

#### 3.1 Memory Cell

Single transistor flash cells are only slightly larger than EPROM cells and rely on the use of a floating polysilicon-gate transistor. The charge on the memory cell’s floating gate changes the threshold voltage of the floating gate transistor which can subsequently be exploited. Charge deposition/removal on the floating gate relies on the combination of hot-electron injection for programming and electron tunneling for erase operations. Many innovations in cell structure and geometry have occurred over the years, some of which are chronicled in [8]. State-of-the-art 128Mb flash memories are now being developed that store two bits of data per cell in a cell size measuring  $1.1 \mu\text{m}^2$  in  $0.4 \mu\text{m}$  CMOS technology [9].

#### 3.2 Peripheral Circuitry

A 32Mb Flash Memory has been recently developed [10] that stores two bits of data per cell using a total of 16M flash memory cells. The two bits per cell are achieved by using four distinct threshold voltages, one for each state. Three reference cells are used to define three reference voltages ( $R_1$ ,  $R_2$ , and  $R_3$ ) that are placed to lie between each of the four state reference voltages.

With respect to Figure 5, during a read operation the read reference cells are used in a binary search sensing scheme such that the addressed array cell is compared, using a comparator, to the reference cell  $R_2$ . This reference cell contains the midpoint reference voltage and defines the MSB of the stored two-bit per cell contents  $D_0$ . With the MSB defined by the output of SA1, the reference cell voltage  $R_1$  (below  $R_2$ ) or the reference voltage  $R_3$  (above  $R_2$ ) is selected and compared using SA2 to the addressed array cell to define the LSB of the two-bit per cell contents  $D_1$ . This conversion technique is essentially that of the well-known two-step A2D converter.

#### 3.3 Architecture

Flash memory array core cells can be arranged in NOR, NAND, or *virtual-ground* configurations; In very high density flash memories, NAND configurations containing 8 to 16 series transistors per bitline are used as the reduced

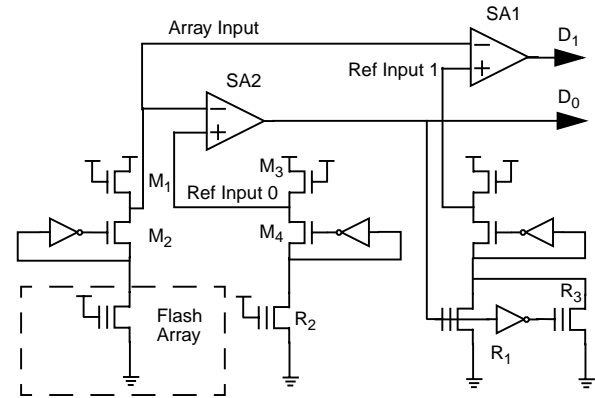


Figure 5. Binary Search Sensing [10]

number of contacts offer a significant size reduction in a NAND configuration relative to a NOR arrangement. Virtual ground configurations are an active area of research and development.

### 4. Dynamic RAM (DRAM)

The densest semiconductor chip that has ever been reported is a DRAM chip, and it is multiple-valued [11]. More than 2 billion memory cells have been integrated on a single chip, each memory cell storing a 4-valued data to create a 4Gb DRAM. This breakthrough came to life only two years after the first 1Gbit binary DRAM [12] was reported in 1995. If an advanced fabrication technology made the first 1Gbit DRAM a reality, it is the multiple-valued nature of the 4Gbit DRAM that pushed this density up by a factor of 4. In this section, we discuss in detail binary and multiple-valued DRAM cells and their associated peripheral circuitry.

#### 4.1 Memory Cell

A DRAM cell (Figure 6) consists of a single capacitor and a single transistor. The capacitor stores a quantity of charge that corresponds to the logical value of the signal, and the transistor acts as a switch to transfer charge between the cell and the bitline when the cell is accessed. A DRAM cell is identical for both binary and multiple-valued storage except for the size of the storage capacitor that is larger in multiple-valued DRAMs.

In a binary DRAM, the voltage levels of the storage are 0 and  $V_{DD}$ , and the reference voltage is  $V_{DD}/2$ . This leaves  $C_s V_{DD}/2$  as the charge stored on the capacitor for each logic signal (0 or 1).

In a quaternary DRAM, the voltage levels of the storage are 0,  $1/3V_{DD}$ ,  $2/3V_{DD}$ , and  $V_{DD}$ . Assuming a midpoint reference voltage scheme, i.e. the reference voltages to be at

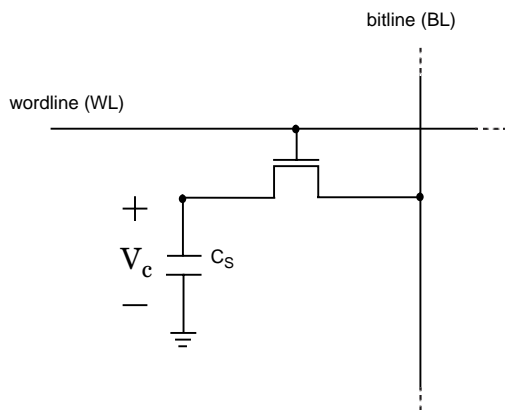


Figure 6. A DRAM Cell

$1/6V_{DD}$ ,  $3/6V_{DD}$  and  $5/6V_{DD}$ , the amount of charge corresponding to each level is only  $1/6C_sV_{DD}$ . Therefore, the  $C_s$  for a quarternary storage must be chosen 3 times as large as the  $C_s$  for a binary case in order to have identical charge per signal level. This could obviously mean a larger cell size for the quarternary storage approach. However, Murotani et al. [11] have shown that by using a high-dielectric-constant material, like BST, the cell size can be reduced to that of a binary cell. A 4-level, 4Gb DRAM that was presented by NEC at the ISSCC97 [11] employs BST to achieve the first quarternary DRAM of this size.

Experimental 16-level storage and beyond have been implemented successfully as reported in the literature [13][14]. A reliable sense and restore (read/writeback) places a limit on the maximum number of voltage levels that can be stored in a cell. This limit can be pushed up by adding error-correction technique to the sense circuitry [15].

#### 4.2 Peripheral Circuitry

A binary sense amplifier (Figure 7) is a fully-differential amplifier that consists of two back-to-back inverters connecting two adjacent bitlines, BL and  $\overline{BL}$ . This structure, also known as *the folded-bitline architecture*, works by having  $\overline{BL}$  serve as a voltage reference when a memory cell connected to BL is being accessed. Before sensing, both inverters are detached from the power supply and precharged on both ends to  $V_{DD}/2$ . In this mode, the inverters do not perform the inversion. A read begins by raising a wordline to  $V_{DD}$  (or boosted  $V_{DD}$ ), allowing the stored charge to be shared with the bitline. This charge sharing creates an imbalance between the voltage levels of BL and  $\overline{BL}$ . The sense amplifier detects this imbalance and amplifies it to recreate the original data and to restore it back to the cell.

In a multiple-valued DRAM, the sense circuitry is in

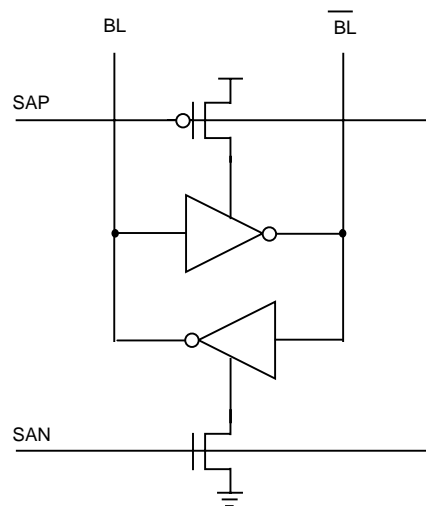


Figure 7. A Binary Sense Amplifier

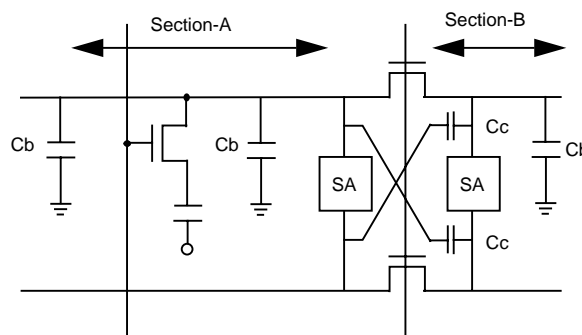


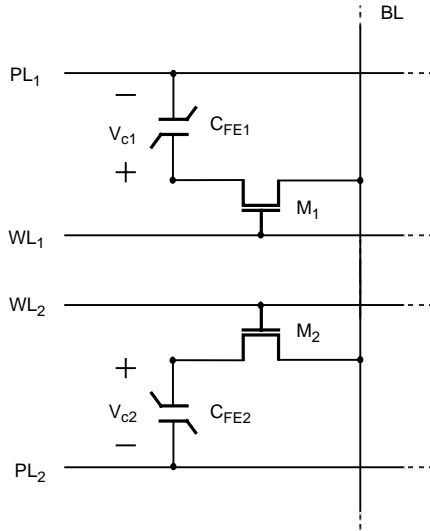
Figure 8. Sense Circuitry for the 4-level 4Gb DRAM [11]

effect an Analog to Digital (A2D) converter that generates  $\log_2(n)$  binary levels from 1-out-of- $n$  stored levels.

Figure 8 illustrates the sense circuitry used in the 4-level 4Gb DRAM [11]. Each bitline is divided into two sections, where Section A has twice the capacitance of Section B, and two binary sense amplifiers are used per bitline pair. The sense circuitry is a two-step pipelined A2D in which sections A and B detect the MSB and the LSB of the 4-valued data, respectively.

Figure 9 illustrates another sensing scheme that is based on a single-slope A2D converter principle [13]. In order to write into a cell, a descending staircase voltage is applied to the wordline, while the bitline pairs are kept at ground level. If a bitline is raised to  $V_{DD}$  at the  $i$ -th level of the staircase, then  $f(i) - V_T$  is stored in the cell, where  $f(i)$  is the voltage level of the staircase at the  $i$ -th interval and  $V_T$  is the



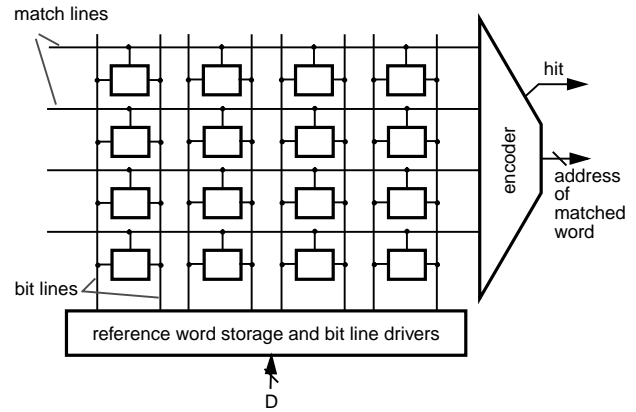


**Figure 12. A 2-bit Binary F.RAM Cell**

capacitor and one access transistor (hence called 1T-1F memory cell). The cell is activated through the word-line (WL), and written or read through the bit-line (BL) and plate-line (PL). In writing a binary digit 0 to the cell, a positive voltage (normally the full power supply,  $V_{DD}$ ) is applied to BL while PL is grounded and WL is asserted. In writing a binary digit 1, a positive voltage is applied to PL while BL is grounded and WL is asserted.

Reading the stored data consists of a sequence of precharging BL, asserting WL, pulsing PL, and sensing the voltage developed on BL by a sense amplifier. Since the reading procedure is destructive, like DRAM, the sensed data must be written back to the memory cell. This will be automatically done after the data is latched in the sense amplifier by restoring PL back to ground level.

Multilevel storage of data in a single FE capacitor faces some difficulties, as the present FE materials and technologies do not support a reliable storage of multilevel polarizations. However, it is possible to store multibit information using more than one capacitor in each cell. One example of such a strategy is shown in Figure 12, where two FE capacitors are used to store 2 bits of information. The area of  $C_{FE2}$  is twice the area of  $C_{FE1}$ . Therefore, four voltage levels can be distinguished on BL if both access transistors  $M_1$  and  $M_2$  are turned ON, and  $PL_1$  and  $PL_2$  are pulsed high simultaneously. The lowest and highest voltage levels are sensed on BL when both  $C_{FE1}$  and  $C_{FE2}$  are holding a digital state 0 or 1, respectively. The second lowest voltage level corresponds to a 1 on  $C_{FE1}$  and a 0 on  $C_{FE2}$ , and the second highest voltage level corresponds to a 0 on  $C_{FE1}$  and a 1 on  $C_{FE2}$ .



**Figure 13. Internal Address and Data Path of a CAM**

The voltage on BL can be sensed using any of the techniques described earlier for DRAM.

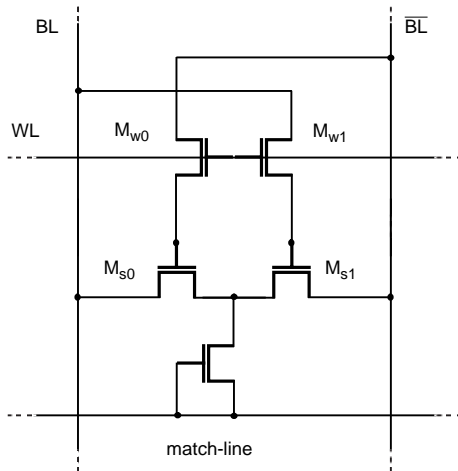
## 6. Content-Addressable Memory (CAM)

A CAM searches for data by content rather than by address. This is the main difference between a CAM and conventional address-based RAMs discussed in previous sections. One application of CAMs is in an electronic spelling checker, where it is merely searched to locate a word with a specific spelling. If there is at least one word with the same spelling as the input word, the search has been successful.

Figure 13 shows a block diagram of a simplified 4 by 4 CAM [20]. Each row of the CAM contains one word (4 bits, in this case). A CAM search begins with applying a reference word (also 4 bits) to the bitlines. Each bit of the reference word is compared against its corresponding bit of every word. A total of 16 bit-comparisons is required to decide which stored word matches the reference word. There is a match if all 4 bits of a stored word are identical to their corresponding bits of the reference word. In this case, the corresponding match line is pulled low. An encoder recognizes this match line and generates a hit signal to indicate a successful match. It also provides the address of the matched word to the next stage.

### 6.1 CAM Architecture

There are several architectures for data access and comparison in a CAM [20]. In a word-serial, bit-parallel architecture, the words are compared, one by one, against the reference word. On the other hand, a bit-serial, word-parallel architecture compares one-bit of each word in a CAM against the corresponding bit of the reference word. Assuming a CAM with  $w$   $n$ -bit words, a search operation using word-serial, bit-parallel architecture requires  $w$  clock



**Figure 14. A Conventional Binary Dynamic CAM Cell [23]**

cycles while a bit-serial, word-parallel architecture requires  $n$  clock cycles. If  $n \ll w$ , a bit-serial, word-parallel architecture is advantageous in terms of search speed.

Searching a CAM for a word that is Greater Than (GT), Not Greater Than (NGT), Less Than (LT), or Not Less Than (NLT) a reference word is also common and has numerous applications [21]. In particular, the intersection of the two sets of words that satisfy both NGT and NLT searches is a set of words that are identical to the reference word. Therefore, the two NGT and NLT searches can be combined to perform an equality search.

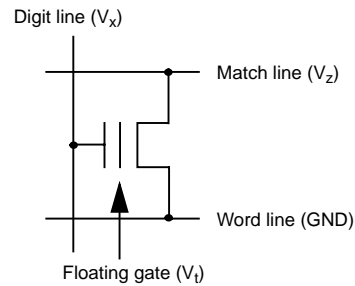
### 6.2 CAM Core Cell

A comprehensive survey of binary CAM cells have been presented in [22]. Among binary CAM cells, we only discuss the conventional dynamic CAM cell. Then we present two multiple-valued, nonvolatile CAM cells. Those are an EEPROM-based cell and a ferro-based cell.

### 6.3 A Binary Dynamic CAM cell

A binary CAM cell, referred to as a conventional dynamic-type CAM cell, is shown in Figure 14 [23]. The binary data is stored on the gates of two storage transistors  $M_{s0}$  and  $M_{s1}$  via two access transistors  $M_{w0}$  and  $M_{w1}$ , respectively. Due to substrate leakage, the stored data must be refreshed on a regular basis (and hence the word dynamic-type). If WL is disabled, the digital state of the match-line will be determined by the exclusive-nor of the stored data and the reference data (BL data). Therefore, a mismatch pulls down the match-line to ground level while a match will leave the match-line in its precharged high level.

Several cells can be laid out in a row with a common



**Figure 15. An EEPROM-Based Cell [24]**

match-line to implement a word. The match-line, in this case, is pulled low if any stored bit does not match its corresponding reference bit.

### 6.4 EEPROM-Based Cell

A single transistor with a floating gate forms the core cell of a novel multiple-valued CAM by Hanyu et al. [24]. The core cell, shown in Figure 15, stores a multiple-valued charge on its floating gate, and performs a threshold operation by comparing the voltage on the digit line ( $V_x$ ) with the stored voltage. As a result of this operation the transistor turns ON or OFF, indicating a match or a mismatch, respectively.

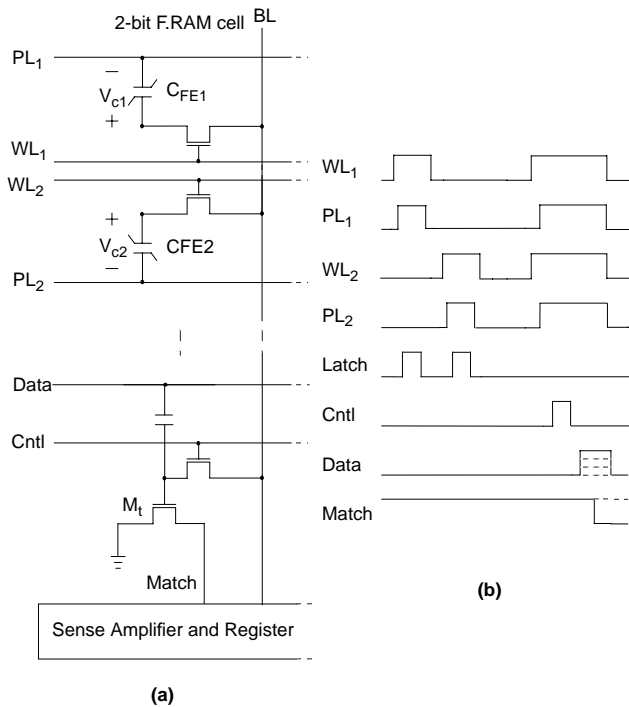
A single threshold operation suffices for an inequality search (like GT or LT search). Two threshold operations are required to complete an equality search. This can be accomplished by successive use of a single floating-gate transistor or a concurrent use of two floating-gate transistors.

The read/write operation of the CAM cell is similar to that of a conventional EEPROM. A write access time is larger than the read access time and requires a higher-voltage power supply.

### 6.5 Ferro-Based Cell

A 4-valued ferroelectric memory cell combined with a threshold-operation circuit form the basis of a 4-valued, nonvolatile, Ferroelectric CAM (FCAM for short) [16]. The read and write operations of the cell is described earlier in this paper. Figure 16 shows a 2-bit F.RAM cell along with the threshold-operation circuitry. A simultaneous access of the two binary cells creates a 4-valued voltage increment on the bitline. This voltage is then added to the converted reference data (also 4-valued) provided on Data line [21]. The final voltage is compared against the threshold voltage of  $M_t$ , causing the match line to be pulled low or stay high depending on the match result.

The threshold-operation circuitry in this design is shared



**Figure 16. (a) A sequential-access structure for a multiple-valued FCAM, (b) The timing diagram for a multiple-valued threshold operation [16].**

among a column of memory cells. Hence, it is different than the EEPROM-based cell in which the threshold-operation circuitry is integrated with the cell. The 4-valued ferro-based cell is suitable for a bit-serial inequality search. Also, the cell can be accessed twice, or two such cells can be accessed simultaneously, to provide an equality search.

An FCAM operates with a single-voltage power supply. Also, the equally-fast read and write access capability makes the device programmable in real time.

## 7. Conclusions

Advances in multiple-valued CMOS memory technology have spanned a wide variety of volatile and non-volatile memory types. The focus of this review has been on CMOS memory technology as this is the de facto mass market vehicle for cost effective products. Many commercial memory products now (or will in the near future) sport memory arrays capable of storing two or more bits per cell. This has provided a double benefit, larger storage capacities for a given silicon area and improved access time per bit for only an incremental cost associated with peripheral circuitry and sometimes marginally larger cell size. What makes all of this truly exciting is the fact that these concepts are manufacturable and yield well in high volume using well-established commercial fabrication

techniques.

A major challenge to continued utilization of multiple-valued circuits in memories is how to design high-performance circuits that work well with low supply voltages. Despite this challenge, in the near future, semiconductor memory trendlines will continue to follow Moore's law, partly due to advances in materials and fabrication technology and partly due to advances in the application of multiple-valued circuits and systems.

## 8. Acknowledgements

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