

### TP 11.7: A Transconductor-Based Field-Programmable Analog Array\*

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Field-programmable gate arrays for prototyping digital circuits are a widely endorsed approach for reducing time-to-market. Offering similar advantages, a field-programmable analog array (FPAA) for prototyping continuous-time linear analog circuits is reported here. Conceptually, a FPAA consists of configurable analog blocks (CABs) and interconnect. The function of each CAB and the connections among CABs are determined by the contents of an on-chip shift register. Different circuits can be instantiated using a FPAA by loading indifferent configuration bits. This IC strategy offers simplified analog circuit design with the advantages of instant prototyping, programmable topology, programmable parameters, CAD compatibility, and testability.

In an earlier approach, a subthreshold-based FPAA utilized current-mode techniques and pass transistors as interconnect [1]. Such an approach, however, is difficult to apply to a wide variety of analog circuits due to the parasitic effects of the pass transistors. This transconductor-based FPAA minimizes the parasitic effects, achieves high linearity, noise immunity and area efficiency.

Though an ideal zero impedance switch in MOS remains elusive, it is possible to linearize the switches by replacing each pass transistor with a four-transistor transconductor [2]. Since each switch has linear resistance, each connection cell in the interconnect can serve not only as an on/off switch but also as a polarity change switch and a variable resistor by applying different control voltages that are either stored in multi-valued memories (MVM) or controlled by internal/external signals. In designing a FPAA, the transconductor can be used as a connection cell in a crossbar network for interconnecting CABs that consist of opamps with feedback capacitors that can be connected into the circuit with switches controlled by registers. Since the transconductor is insensitive to distributed parasitic capacitance the FPAA will also be parasitic insensitive [2].

The transconductance of the transconductors, can be changed by adjusting the control voltages, and has a tuning range limited to approximately one decade only (without introducing excess noise). In addition, an architecture based solely on four-transistor transconductors consumes large area especially for low frequency applications due to the use of long transistors and a MVM in each connection cell [3].

Most circuits usually require 1.5 - 2.5 resistors (or connections) and 1 - 2 switches per opamp [3]. Therefore, a full crossbar network may often be highly under-utilized in light of the previous remarks. To efficiently exploit these observations, a modified MOS transconductor shown in Figure 1 is proposed. Theoretical analysis and HSPICE simulations show that it has harmonic distortion and frequency response comparable with the original four-transistor transconductor. The FPAA shown in Figure 2 is based on this transconductor. The central part of the transconductor is located at the bottom of each column in the variable resistor interconnection network (VRIN). The interconnection network contains the termination parts of the transconductors as connection cells. Different connections between CABs are achieved by turning on the corresponding termination parts as indicated by the shaded cells. Since the resistance is the sum of the linear resistance of each part, the termination parts can have minimum-size transis-

tors and the central part can have long transistors without significantly increasing the overall area for low-frequency applications. Furthermore, two sets of different-sized transistors and a precise S/H (similar to the design in Reference 4) for the MVM can be used in each central part to increase the tuning range and the accuracy of the resistance, respectively. Each transconductance value is set by loading a 10b register that is multiplexed to an on-chip DAC and converted to an analog voltage for refreshing the S/H periodically. Note that one column only realizes one transconductor and, hence, the number of resistors is limited by the number of columns. To further increase the tuning range of the RC time constants, two sets of feedback capacitors with different sizes are used in each CAB. The compensation of the opamp inside each CAB can also be disabled to allow the opamp to act as a fast comparator. In the signal-controlled interconnection network (SCIN), the control voltages for the central part of the transconductors are controlled by either the CAB outputs or external inputs via connection cells (indicated by squares). The central parts in the SCIN also consist of voltage level shifters at the control inputs that can be turned on or off. The FPAA also provides connection columns for three 6b binary-weighted programmable capacitor arrays (PCAs).

The FPAA, in 1.2 $\mu$ m CMOS, consists of 4CABs, 8 VRIN columns, 6 SCIN columns and 3 columns for connecting PCAs. The active area is about 2.5x2.5mm<sup>2</sup>. The die micrograph is shown in Figure 7. The FPAA dissipates less than 80 mW. The opamp in each CAB has an  $f_{-3dB}$  of 3 MHz and >60dBdc gain.

Upon being powered up the FPAA requires 353 configuration bits to a particular circuit. Many different circuits including a programmable-gain amplifier, first-to fourth-order continuous-time analog filters, a VCO, a precision full-wave rectifier and a four-quadrant multiplier tested successfully on the FPAA. Figure 3 shows a filter biquad with its embedding into the FPAA shown in Figure 2. The CABs are configured with the feedback capacitors connected. Figure 4 presents the experimental results with different transconductance and capacitance values by shifting in different configuration bits. The THD is less than -57dB at 1kHz for a 1.6V peak-to-peak output swing. Figure 5 shows the results of the full-wave rectifier that uses a comparator to detect the zero crossing of the input signal that in turn is used by the input transconductor to change the polarity of the input signal to the opamp. The opamp is connected in an inverting configuration using two transconductors. The input transconductor is embedded in the SCIN with the control terminals connected to the comparator output. Figure 6 presents the results of the four-quadrant multiplier. Since the input sinusoidal signal is multiplied by itself, a square circuit (in this case a frequency doubler) is realized. The multiplier is configured by connecting an opamp with two transconductors in inverting configuration with the two multiplier inputs being input terminals and control terminals of the input transconductor.

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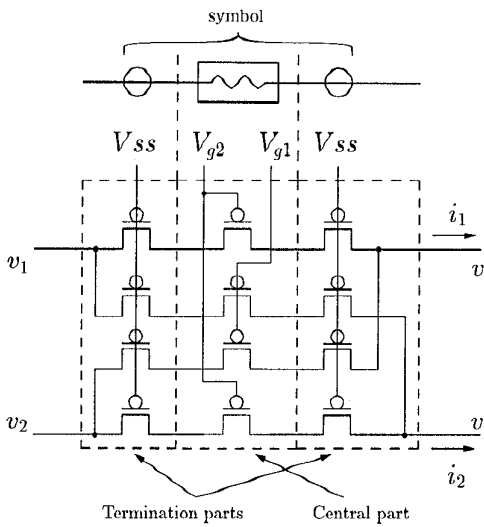


Figure 1: Modified MOS transistor.

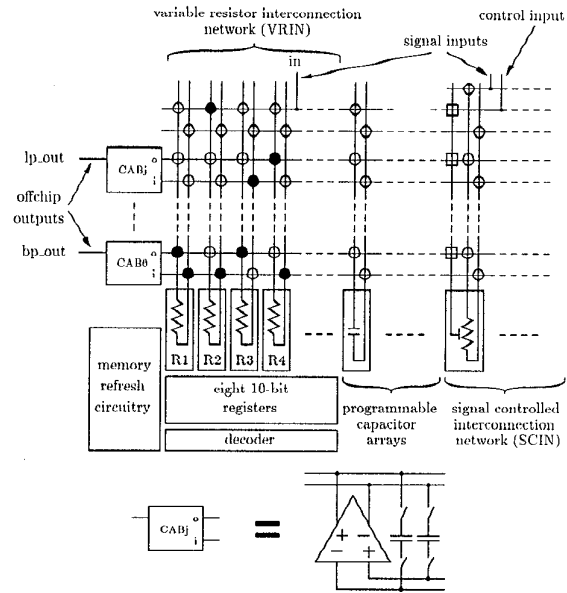


Figure 2: FPAAs based on modified transconductors and embedded filter biquad (• active termination, o = non-active termination and = control terminal connection cell).

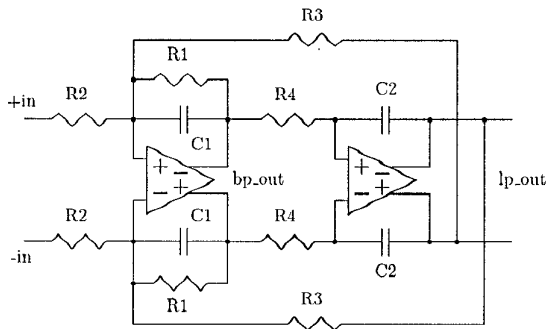


Figure 3: Filter bi-quad schematic.

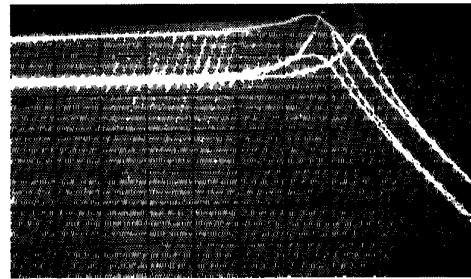


Figure 4: Measured frequency response of biquad low-pass output with different configuration bits that control Q,  $\Omega$ , and DC gain (X-axis: 1 decade/3 divisions starting from 20Hz and Y-axis: 10dB/division).

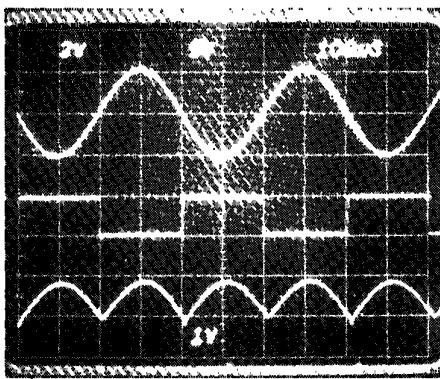


Figure 5: Experimental results of configured full-wave rectifier results (upper, input; middle, comparator output; lower, output).

Acknowledgements

Support by grants from NSERC, Micronet, ITRC and fabrication through CMC are acknowledged.

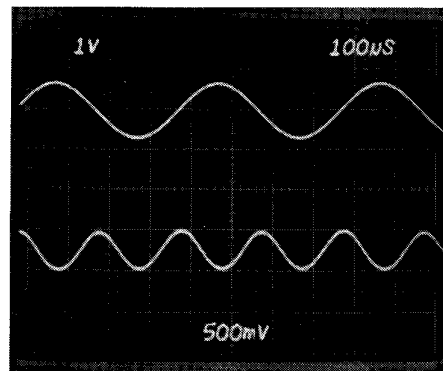


Figure 6: Experimental multiplier circuit results (upper, input; lower, output).

Figure 7: See page 366.

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TP 11.7: A Transconductor-Based Field-Programmable Analog Array

(Continued from page 199)

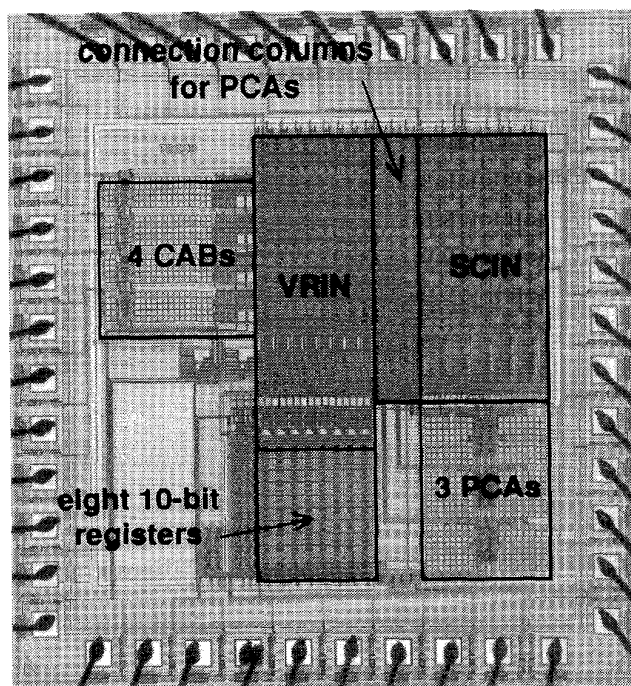


Figure 7: Field-programmable analog array chip micrograph.