

ECE 1387 - CAD for Digital Circuit Synthesis and Layout
Assignment #1 – Crosstalk-Aware FPGA Router

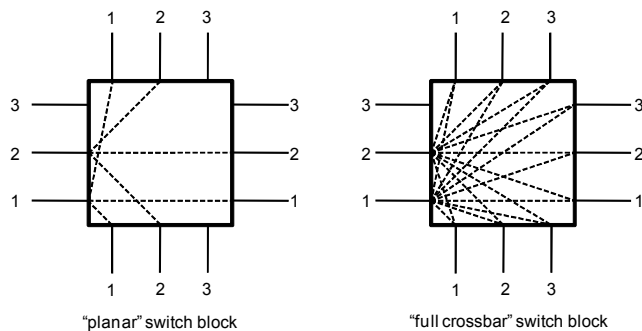
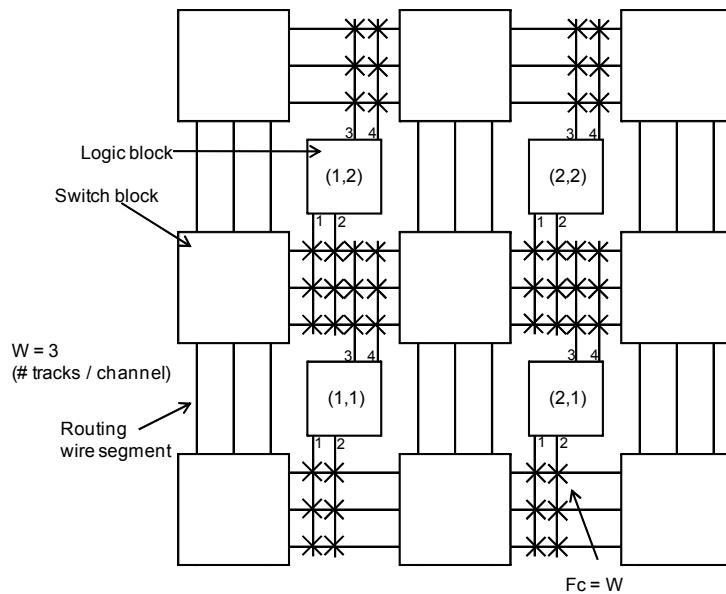
January 2009

J. Anderson

Assignment Date: January 16
Due Date: February 6 (before lecture begins)
Late Penalty: -1 mark per day late, with total marks available = 20

You are to write an implementation of the FPGA maze router described in class, and innovate to handle the negative effects of crosstalk on routing delay. You must have your program display its progress with X11-based graphics. A C-based graphics package is provided on the course web page. You may use either Linux or Solaris.

You should use the FPGA architecture described in class, as illustrated in the figure below. The figure shows the pin numbering scheme, and the x,y position scheme. Two different switch block topologies are shown: “planar” and “full crossbar”. Note that the entire switch block is not shown, just some of the connections. Make sure that you understand how the complete switch blocks look, for any value of W.



Your program should take input from a file that has the following format:

The first line consists of one integer, n, where n is an integer giving the n x n dimension of the chip in logic blocks. The grid cells are numbered from 1 to N in each dimension.

The second line indicates the number of tracks per channel to use, W.

The next set of lines have the form “X1 Y1 P1 X2 Y2 P2 Y|N”. Each of these lines gives a pair of pins to be connected. The first pin is attached to the block at location X1,Y1, and uses pin number P1, where P1 = 1, 2, 3 or 4. The second pin is specified in the same manner by X2, Y2 and P2. The last item on each line is a single character, which is either ‘Y’ or ‘N’, and this indicates whether this is a timing-critical connection – those connections with a ‘Y’ are timing-critical, and this information will be used below. This list is terminated by the line: -1 -1 -1 -1 -1 -1 N.

Example input file:

10	(10 x 10) grid
3	(3 tracks per channel)
1 2 4 4 4 1 Y	Pin 4 on block at (1,2) connects to pin 1 at (4,4)
3 3 4 8 9 3 N	Pin 4 on block at (3,3) connects to pin 3 at (8,9)
-1 -1 -1 -1 -1 -1 N	(end of pin pair list)

Your program must be able to display the routing solution for all of the connections in the test file using the graphics display. For debugging purposes, you may find it helpful to write your program so that it can display the progress of your algorithm as it routes each step for each connection; that is, you may wish to display each step of the router expansion (though this is not mandatory for this assignment). You should test your program on the following test files located on the course web page:

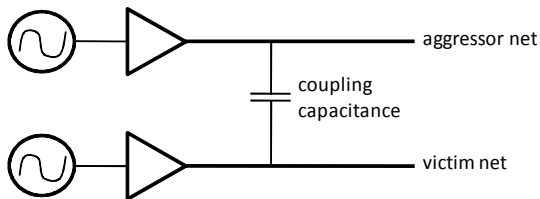
fcct1_09, fcct2_09, fcct3_09 and fcct4_09

Note that in addition to routing each circuit with the value of W given in the input file, you will need to find the smallest value of W for which the test circuits will route successfully.

Note: Use the **planar** switch block for all parts of this assignment, except for bonus Step 7 (below).

What to do and hand in:

1. A listing of your program.
2. The location of the executable file (on EEGC or ECF), with instructions on how to run it. Please set permissions so that I can run it.
3. [10 marks for working router] A paper plot of the results from the four test files (using the value of W given in the test files). The graphics package allows you to do this.
4. [3 marks] The smallest number of tracks/channel (W) that your program could successfully route those circuits in. **That is:** your program should be capable of varying the number of tracks per channel, and you are required to find the smallest number of tracks per channel that your program will successfully route the circuits in. Try different connection ordering schemes to reduce W . Explain any tricks you applied that were successful in reducing W .
5. [4 marks] Crosstalk is a growing problem in deep submicron CMOS design that affects circuit delay, as illustrated in the figure below. When two gates drive adjacent parallel routes, there is capacitive coupling between the two routes. If the aggressor net and victim net transition at the same time, but in opposite directions, then the delay of the victim net becomes longer (relative to the case when the victim net transitions by itself and the aggressor net is silent). Conversely, if the aggressor and victim nets transition at the same time and in the same direction, the delay of the victim net becomes shorter.



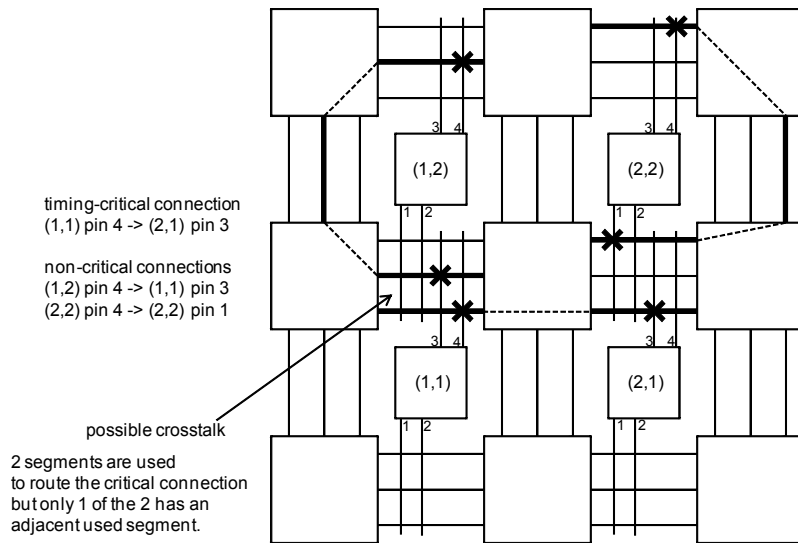
In this part of the assignment, you will modify your router to “isolate” the routing of the timing-critical connections, reducing the number of nearby “aggressor” connections, thereby minimizing crosstalk. Let I be the set of connections that are timing-critical (i.e. those connections marked with a ‘Y’ in the input file). Let S be the set of routing segments used in the routing paths for the connections in set I . Define the *crosstalk cost*, CC , as:

$$CC = \sum_{s \in S} CrossCoupling(s)$$

where $CrossCoupling(s)$ is as follows:

- 0: No adjacent segment to s is used.
- 1: One adjacent segment to s is used.
- 2: Two adjacent segments to s are used.

Here is an example routing of three connections, one of which is critical. The *crosstalk cost* is 1 in this case.



You must devise clever techniques to make your router crosstalk-aware, such that it minimizes the crosstalk cost, CC . Using the above equation, report the crosstalk cost for each of the test circuits. You should report two numbers for each circuit: 1) the crosstalk cost when the circuit was routed without crosstalk optimization (that is, using the router of Step 3; and 2) the crosstalk cost when routed using the techniques you incorporated. Report how much the crosstalk cost was improved for each circuit. **Note:** for this step, you should use the W values given in the test files.

6. [3 marks] Hand in a two-page description of the flow of your software, describing the major routines and data structures, and how they interact. Where you were faced with choices in your implementation of the algorithm, indicate what choices you made, and why. Describe how you made your router crosstalk-aware and the different approaches you investigated and why you selected the one you did.
7. [Bonus for 2 marks]: Change the switch block from the planar to the full crossbar style and repeat Step 4 above. How much does the minimum W decrease for each of the circuits? Comment on why.