

University of Toronto, Department of Electrical and Computer Engineering

ECE 1387 - CAD for Digital Circuit Synthesis and Layout

January 2009

J. Anderson

- Instructor:** Jason Anderson
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Office Hours: After class or by appointment (send e-mail or phone)
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- Pre-requisites:** ECE 1388 (VLSI Design Methodology), or ECE 451 (VLSI Systems), or CSC 2410 (Algorithms in Graph Theory), or Permission of instructor. **Programming skills in C**, including data structures.
- Lecture:** Fridays 4 PM – 6 PM, room BA 4164 (Bahen Building)
- Papers/Readings:** Available in PDF on course website.
- Reference Texts:** **EDA for IC Implementation, Circuit Design, and Process Technology**, L. Scheffer, L. Lavagno, G. Marin (editors), CRC Press, 2006 (not mandatory).
- Evaluation:**
- | | | | |
|-------------|--------------|---------------------|-----|
| Assignments | 55% (3 or 4) | Paper | 25% |
| Exercises | 10% (2 or 3) | Class Participation | 10% |
- Assignments:** Programming implementations of CAD problems such as placement, routing, and technology mapping using optimization strategies such as simulated annealing, dynamic programming, integer linear programming (ILP), and branch and bound, and illustrated using computer graphics.
- Exercises:** Hands-on experience with CAD tools such as ABC (UC Berkeley), VPR (Auto Place & Route) and hMetis (Partitioning).
- The Paper:** A critical assessment of work in a subset of the field (chosen in consultation with the instructor) based on 3 to 4 papers.
- Class Participation:** It is the expectation that you will contribute one good question or idea per class to the general discussion. Hopefully more!

TENTATIVE Lecture and Assignment Schedule

| # | Date Lecture | Lecture Topic | Assignment/ Exercise Handed Out | Assignment/ Exercise Due |
|----|--------------|--|--|--------------------------------|
| 1 | Jan 9 | Introduction, Overview | Paper | |
| 2 | Jan 16 | Detailed Routing | Assignment 1 – FPGA Maze Router | |
| 3 | Jan 23 | Timing-Driven Routing | | |
| 4 | Jan 30 | Placement | | |
| 5 | Feb 6 | Placement (Simulated Annealing) | Exercise 1 – VPR Placement and Routing | Assignment 1 |
| 6 | Feb 13 | Placement (Analytical Techniques) | Assignment 2 – Analytical Placement | Exercise 1 |
| | Feb 20 | NO CLASS – READING WEEK | | |
| 7 | Feb 27 | Timing Analysis and Slack Allocation | | |
| 8 | March 6 | Partitioning (Branch and Bound) | Assignment 3 – Partitioning Using B&B | Assignment 2 |
| 9 | March 13 | Partitioning (FM/Multi-Level: hMetis) | Exercise 2 – Partitioning Using hMetis | |
| 10 | March 20 | Technology Mapping (Dynamic Programming) | Assignment 4 – Technology Mapping Using Dynamic Prog in ABC (UC Berkeley) | Assignment 3 |
| 11 | March 27 | Floorplanning via Sequence Pair OR Physical Optimization via ILP | Exercise 3 – Floorplanning or Int Linear Programming (ILP) | Exercise 2 |
| 12 | April 3 | Special Guest Lecture; TOPIC: TBA | | |
| | April 13 | | | Exercise 3, Assignment 4 |
| | April 17 | | | Paper |

NOTE: You must consult with the instructor on your paper topic by mid-March.