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Education

- **University of Toronto** Toronto, Canada
Doctor of Philosophy (Ph.D.) in Electrical and Computer Engineering Sept. 2001 – June 2005
– Thesis: "Power optimization and prediction techniques for FPGAs".
- **University of Toronto** Toronto, Canada
Master of Applied Science (M.A.Sc.) in Electrical and Computer Engineering Sept. 1995 – Nov. 1997
– Thesis: "Architectures and algorithms for laser-programmed gate arrays with foldable logic blocks".
- **University of Manitoba** Winnipeg, Canada
Bachelor of Science (B.Sc.) in Computer Engineering (with Distinction) Sept. 1991 – May 1995
– Thesis: "Speaker identification using artificial neural networks".

Academic Work Experience

- **University of Toronto** Toronto, Canada
Assistant Professor of Electrical and Computer Engineering August 2008 – present
– Date of appointment: August 18, 2008
- **University of Toronto** Toronto, Canada
Adjunct Professor of Electrical and Computer Engineering July 2005 – July 2008
– Instructor for the graduate course "ECE-1387: CAD for Digital Circuit Synthesis and Layout".
– Adjunct faculty while working full-time in the semiconductor industry at Xilinx, Inc.

Industrial Work Experience

- **Xilinx, Inc.** Dec. 1997 – July 2008: San Jose, CA, USA (5 years); Toronto, Canada (5.5 years)
Positions Held: Principal Engineer and Manager ('07 – '08; Senior Manager ('06 – '07); Senior Staff Software Engineer ('04 – '06); Staff Software Engineer ('00 – '04); Senior Software Engineer ('98 – '00); Software Engineer ('97 – '98)
 - Managed and led a team of six engineers, responsible for the research, design and development of synthesis, placement and routing tools for Xilinx FPGAs.
 - Two years managing all place/route activities at Xilinx, with a team of over 20 engineers.
 - Developer and lead engineer on several major projects, building state-of-the-art FPGA tools used by thousands of Xilinx customers worldwide.
 - Liaised with academia and the research community; responsible for keeping apprised of recent research results and facilitating their transfer into Xilinx.
 - Served on the Patent Committee – a select group of 10-15 technical leaders at Xilinx that reviews all company inventions and selects those which should be patented.
 - Instrumental in project planning/management, product definition, personnel management, team building and interviewing/hiring of new staff.
 - Mentored and trained many junior engineers via formal training sessions and one-on-one interactions. Well-versed in varied supervisory methods and strategies for personnel development.
 - Devised, implemented and evaluated new FPGA place and route algorithms as well as enhancements to existing algorithms that led to significant reductions in tool run-time and improved quality-of-result.
 - Inventor and award recipient of more than 10 trade secrets – patentable inventions Xilinx has chosen to keep confidential.

Research Interests

- FPGA and other programmable hardware architectures, tools, and applications, particularly computing and embedded systems applications with power and area constraints.
- Low-power design at the HDL, gate, circuit and process technology levels.
- Tools and algorithms for the automated synthesis of FPGAs and other ICs.
- VLSI architectures and circuit design.
- Software engineering for large-scale systems.

United States Patents

- PAT1. H. Xu, V. Verma, A. Rahut, **J.H. Anderson**, S. Kalman, "Patterns for routing nets in a programmable logic device," US Patent #7,797,665, Issued September 2010.
- PAT2. **J.H. Anderson**, Q. Wang, "Method for technology mapping considering Boolean flexibility," US Patent #7,725,047, Issued June 2010.
- PAT3. V. Verma, A. Rahut, S.K. Nag, **J.H. Anderson**, R. Jayaraman, "Method and apparatus for facilitating signal routing within a programmable logic device," US Patent #7,725,868, Issued May 2010.
- PAT4. **J.H. Anderson**, M. Chirania, S. Gupta, P. Costello, "Method of reducing power of a circuit," US Patent #7,653,891, Issued January 2010.
- PAT5. T. Jang, K. Chung, **J.H. Anderson**, Q. Wang, S. Gupta, "Method and apparatus for power optimization using don't care conditions of configuration bits in lookup tables," US Patent #7,603,646, Issued October 2009.
- PAT6. Q. Wang, R. Aggarwal and **J.H. Anderson**, "Processing constraints in computer-aided design for integrated circuits," US Patent #7,555,734, Issued June 2009.
- PAT7. J. Saunders, K. Anandh, G. Stenz, S.K. Nag and **J.H. Anderson**, "Unified placer infrastructure," US Patent #7,398,496, Issued July 2008.
- PAT8. V. Verma, A. Rahut, S.K. Nag and **J.H. Anderson**, "Method and apparatus for facilitating signal routing within a programmable logic device," US Patent #7,306,977, Issued December 2007.
- PAT9. **J.H. Anderson**, S.K. Nag G. Stenz and S. Dasasathyan, "Method for application of network flow techniques under constraints," US Patent #7,143,380, Issued November 2006.
- PAT10. **J.H. Anderson**, S. Kalman and V. Verma, "Incremental routing in integrated circuit design," US Patent #7,134,112, Issued November 2006.
- PAT11. **J.H. Anderson**, S. Kalman and V. Verma, "Post-layout optimization in integrated circuit design," US Patent #7,111,268, Issued September 2006.
- PAT12. R. Kong and **J.H. Anderson**, "Method for computing and using future costing data in signal routing," US Patent #7,073,155, Issued July 2006.
- PAT13. **J.H. Anderson** and F.N. Najm, "Leakage power optimization for integrated circuits," US Patent #6,993,737, Issued January 2006.
- PAT14. J. Saunders, K. Anandh, G. Stenz, S.K. Nag and **J.H. Anderson**, "Unified placer infrastructure," US Patent #6,983,439, Issued January 2006.
- PAT15. G.-J. Nam, S. Kalman, **J.H. Anderson**, R. Jayaraman, S.K. Nag and J. Zhuang, "Method and apparatus for testing routability," US Patent #6,877,040, Issued April 2005.
- PAT16. **J.H. Anderson**, "Incremental placement of design objects in an integrated circuit design," US Patent #6,871,336, Issued March 2005.
- PAT17. S. Dasasathyan, G. Stenz, S.K. Nag and **J.H. Anderson**, "Placement of objects with partial shape restriction," US Patent #6,857,115, Issued February 2005.

- PAT18. R. Kong and **J.H. Anderson**, "Method for computing and using future costing data in signal routing," US Patent #6,851,101, Issued February 2005.
- PAT19. **J.H. Anderson**, J. Saunders, M. Chari, S. Nag and R. Jayaraman, "Method and apparatus for placement of input-output design objects into a programmable gate array," US Patent #6,625,795, Issued September 2003.
- PAT20. S. Nag, K. Chaudhary, **J.H. Anderson**, M. Chari and S. Kalman, "Method and apparatus for timing-driven implementation of a circuit design," US Patent #6,484,298, Issued November 2002.
- PAT21. **J.H. Anderson**, J. Saunders, M. Chari, S. Nag and R. Jayaraman, "Placement of input-output design objects into a programmable gate array supporting multiple voltage standards," US Patent #6,289,496, Issued September 2001.
- PAT22. Inventor on additional patents pending.

Publications

Refereed Journal Publications:

- P1. M. Gort, **J.H. Anderson**, "A combined architecture/algorithm approach to reducing FPGA routing time," submitted to *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, October 2011. (13 pages)
- P2. C. Ravishankar, **J.H. Anderson**, A. Kennings, "FPGA power reduction by guarded evaluation considering logic architecture," in revision for *IEEE Transactions on Computer Aided Design for Integrated Circuits and Systems (TCAD)*, October 2011. (14 pages)
- P3. A. Canis, J. Choi, M. Aldham, V. Zhang, A. Kammoona, **J.H. Anderson**, S. Brown, T. Czajkowski, "LegUp: Open source high-level synthesis for FPGA-based processor/accelerator systems," in revision for *ACM Transactions on Embedded Computing Systems (TECS)*, February 2011. (25 pages)
- P4. M. Gort, **J.H. Anderson**, "Accelerating FPGA routing through parallelization and engineering enhancements," *IEEE Transactions on Computer Aided Design for Integrated Circuits and Systems Systems (TCAD)*, Vol. 31, No. 1, pp. 61-74, January 2012.
- P5. **J.H. Anderson**, Q. Wang. C. Ravishankar, "Raising FPGA logic density through synthesis-inspired architecture," accepted to appear in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, December 2010. (14 pages).
- P6. T. Ahmed, P. Kundarewich, **J.H. Anderson**, "Packing techniques for Virtex-5 FPGAs," *ACM Transactions on Reconfigurable Technology and Systems*, Vol. 2, No. 3, September 2009.
- P7. **J.H. Anderson** and F.N. Najm, "Low-power programmable FPGA routing circuitry," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 8, pp. 1048-1060, August 2009.
- P8. **J.H. Anderson** and F.N. Najm, "Active leakage power optimization for FPGAs," *IEEE Transactions on Computer-Aided Design for Integrated Circuits and Systems (TCAD)*, Vol. 25, No. 3, pp. 423-437, March 2006. ****9th-most downloaded IEEE EDA article in 2006 [June 2007 newsletter of the IEEE Council on EDA (CEDA)].**
- P9. **J.H. Anderson** and F.N. Najm, "Power estimation techniques for FPGAs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 10, pp. 1015-1027, October 2004.

Refereed Conference Publications:

- P10. Z. Poulis, Y.-S. Yang, **J.H. Anderson**, A. Veneris, "Leveraging reconfigurability to raise productivity in FPGA functional debug," accepted to appear in the *IEEE/ACM Design Automation and Test Conference (DATE)*, to be held at Dresden, Germany, 2012.
- P11. S. Hadjis, A. Canis, **J.H. Anderson**, J. Choi, K. Nam, S. Brown, T. Czajkowski, "Impact of FPGA architecture on resource sharing in high-level synthesis," accepted to appear in the *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, to be held at Monterey, CA, 2012.

- P12. W. Shum, **J.H. Anderson**, "Analyzing and predicting the impact of CAD algorithm noise on FPGA speed performance and power," accepted to appear in the *ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, to be held at Monterey, CA, 2012.
- P13. J. Rose, J. Luu, K. Kent, C. W. Yu, O. Densmore, J. Goeders, A. Somerville, K. Kent, P. Jamieson, **J.H. Anderson**, "The VTR Project: Architecture and CAD for FPGAs from Verilog to routing," accepted to appear in the *ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, to be held at Monterey, CA, 2012.
- P14. M. Aldham, **J.H. Anderson**, S. Brown, A. Canis, "Low-cost hardware profiling of run-time and energy in FPGA embedded processors," *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pp. 61-68, Santa Monica, CA, 2011. [Acceptance rate: 26%].
- P15. B. Teng, **J.H. Anderson**, "Latch-based performance optimization for FPGAs," *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 58-63, Crete, Greece, 2011. [Acceptance rate: 28%].
- P16. M. Gort, **J.H. Anderson**, "Reducing FPGA router run-time through algorithm and architecture," *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 336-342, Crete, Greece, 2011. (**Best Paper Award**) [Acceptance rate: 28%].
- P17. W. Shum, **J.H. Anderson**, "FPGA glitch power analysis and reduction," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 27-32, Fukuoka, Japan, 2011. [Acceptance rate: 22%].
- P18. A. Canis, J. Choi, M. Aldham, V. Zhang, A. Kammoona, **J.H. Anderson**, S. Brown, T. Czajkowski, "LegUp: High-level synthesis for FPGA-based processor/accelerator systems," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 33-36, Monterey, CA, February, 2011. [Acceptance rate: 45%].
- P19. J. Luu, **J.H. Anderson**, J. Rose, "Architecture description and packing for logic blocks with hierarchy, modes and complex interconnect," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 227-236, Monterey, CA, February, 2011. [Acceptance rate: 26%].
- P20. **J.H. Anderson**, Q. Wang, "Area-efficient FPGA logic elements: architecture and synthesis," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 369-375, Yokohama, Japan, January 2011. (**Nominated for Best Paper**) [Acceptance rate: 31%].
- P21. A. Rakhshanfar, **J.H. Anderson**, "An integer programming placement approach for FPGA clock power reduction," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 831-836, Yokohama, Japan, January 2011. [Acceptance rate: 31%].
- P22. M. Gort, **J.H. Anderson**, "Deterministic multi-core parallel routing for FPGAs," *IEEE International Conference on Field Programmable Technology (FPT)*, pp. 78-86, Beijing, China, December 2010. [Acceptance rate: 20%].
- P23. S. Birk, J.G. Steffan, **J.H. Anderson**, "Parallelizing FPGA placement using transactional memory," *IEEE International Conference on Field Programmable Technology (FPT)*, pp. 61-69, Beijing, China, December 2010. (**Best Paper Award**) [Acceptance rate: 20%].
- P24. **J.H. Anderson**, C. Ravishankar, "FPGA power reduction by guarded evaluation," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 157-166, Monterey, CA 2010. [Acceptance rate: 25%].
- P25. **J.H. Anderson**, "A PUF design for secure FPGA-based embedded systems," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 1-6, Taipei, Taiwan, 2010. [Acceptance rate: 34%].
- P26. **J.H. Anderson**, Q. Wang, "Improving logic density through synthesis-inspired architecture," *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 105-111, Prague, Czech Republic, 2009. [Acceptance rate: 25%].
- P27. S. Huda, M. Mallick, **J.H. Anderson**, "Clock gating architectures for FPGA power reduction," *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 112-118, Prague, Czech Republic, 2009. [Acceptance rate: 25%].

- P28. Q. Wang, S. Gupta, **J.H. Anderson**, "Clock power reduction for Virtex-5 FPGAs," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 13-22, Monterey, CA, 2009. [Acceptance rate: 26%]
- P29. T. Ahmed, P. Kundarewich, **J.H. Anderson**, B. Taylor and R. Aggarwal, "Architecture-specific packing for Virtex-5 FPGAs," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 5-13, Monterey, CA, 2008. [Acceptance rate: 29%]
- P30. S. Gupta, **J.H. Anderson**, L. Farragher, Q. Wang, "CAD techniques for power optimization in Virtex-5 FPGAs," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 85-88, San Jose, CA, 2007. [Acceptance rate: 33%]
- P31. **J.H. Anderson** and F.N. Najm, "Low-power programmable routing circuitry for FPGAs," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 602-609, San Jose, CA, 2004. [Acceptance rate: 24%]
- P32. **J.H. Anderson** and F.N. Najm, "A novel low-power FPGA routing switch," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 719-722, Orlando, FL, 2004. [Acceptance rate: 39%]
- P33. **J.H. Anderson**, S. Nag, K. Chaudhary, S Kalman, C. Madabhushi and P. Cheng, "Run-time-conscious automatic timing-driven FPGA layout synthesis," *International Conference on Field-Programmable Logic and Applications (FPL)*, pp. 168-178, Antwerp, Belgium, 2004. [Acceptance rate: 42%]
- P34. **J.H. Anderson**, F.N. Najm and T. Tuan, "Active leakage power optimization for FPGAs," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 33-41, Monterey, CA, 2004. [Acceptance rate: 27%]
- P35. **J.H. Anderson** and F.N. Najm, "Interconnect capacitance estimation for FPGAs," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 713-718, Yokohama, Japan, 2004.
- P36. **J.H. Anderson** and F.N. Najm, "Switching activity analysis and pre-layout activity prediction for FPGAs," *ACM/IEEE International Workshop on System-Level Interconnect Prediction (SLIP)*, pp. 15-21, Monterey, CA, 2003.
- P37. **J.H. Anderson** and F.N. Najm, "Power-aware technology mapping for LUT-based FPGAs," *IEEE International Conference on Field-Programmable Technology (FPT)*, pp. 211-218, Hong Kong, 2002. [Acceptance rate: 39%]
- P38. **J.H. Anderson**, J. Saunders, S. Nag, C. Madabhushi and R. Jayaraman, "A placement algorithm for FPGA designs with multiple I/O standards," *International Conference on Field-Programmable Logic and Applications (FPL)*, LNCS 1896, Springer-Verlag, pp. 211-220, Villach, Austria, 2000.
- P39. **J.H. Anderson** and S.D. Brown, "Technology mapping for large complex PLDs," *ACM/IEEE Design Automation Conference (DAC)*, pp. 698-703, San Francisco, CA, 1998. [Acceptance rate: 36%]
- P40. **J.H. Anderson** and S.D. Brown, "An LPGA with foldable logic blocks," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 244-252, Monterey, CA, 1998.

Magazine Articles:

- P41. S. Gupta and **J. Anderson**, "Optimizing FPGA power with ISE design tools," *Xcell Journal – The Journal for Programmable Logic Users*, Vol. 60, pp. 16-19, First Quarter 2007.

Software Artifacts Released

- **LegUp: High-level circuit synthesis** 2011
 - LegUp is an open source high-level synthesis tool that *automatically* compiles C program to a hybrid system comprising a processor and custom hardware accelerators. The accelerators work in tandem with the processor to execute the program on an FPGA-based platform with superior performance and energy-efficiency to a software-only solution. An overarching aim of the project is to make FPGA technology accessible to software engineers.
 - The tool (freely available at <http://www.legup.org>) is one of the few open source systems of its kind and it has already been downloaded by over 150 research groups around the world since its initial release in March 2011.

University Courses Taught

Graduate:

- **University of Toronto, Dept. of Electrical and Computer Engineering** Toronto, Canada
ECE-1387: CAD for Digital Circuit Synthesis and Layout July 2005 – present
 - Course deals with algorithms for automatic circuit synthesis for digital integrated circuits, with a concentration on the back-end of the flow: technology mapping, partitioning, placement, routing, timing analysis and physical synthesis.
 - Enrollment was 13 in fall 2005 session; 16 in fall 2006 session; 12 in fall 2007 session; 7 in spring 2009 session; 14 in spring 2010 session; 12 in spring 2011 session; 18 in fall 2011 session.

Undergraduate:

- **University of Toronto, Dept. of Electrical and Computer Engineering** Toronto, Canada
ECE-241: Digital Systems 2009 – present
 - A second-year course on digital design using Verilog and FPGAs.
- **University of Toronto, Dept. of Electrical and Computer Engineering** Toronto, Canada
APS-105: Computer Fundamentals 2008 – present
 - A first-year introductory course on programming and problem solving in C.

Awards and Honours

- **Best Paper Award at the IEEE Int'l Conf. on Field Programmable Logic** 2011
 - For paper: “Reducing router run-time through algorithm and architecture”.
- **ECE Departmental Teaching Award for ECE-241: Digital Systems** 2011
 - Awarded based on ratings in anonymous course evaluations by the undergraduate students.
 - Third teaching award in three successive years of undergraduate teaching.
- **Best Paper Nomination at the IEEE/ACM ASP-DAC Conference** 2011
 - For paper: “Area-efficient FPGA logic elements: architecture and synthesis”.
- **Best Paper Award at the IEEE Int'l Conf. on Field Programmable Technology** 2010
 - For paper: “Parallelizing FPGA placement using transactional memory”.
- **ECE Departmental Teaching Award for APS-105: Computer Fundamentals** 2010
- **ECE Departmental Teaching Award for APS-105: Computer Fundamentals** 2009
- **Nominee for the TV Ontario (TVO) Best Lecturer Competition** 2009
 - A competition held yearly in the Province of Ontario by the public broadcaster TVO and nominated by students.
- **Ontario Graduate Scholarship in Science and Technology (\$15,000)** 2004 – 2005
- **Ontario Graduate Scholarship (\$15,000)** 2003 – 2004
- **NSERC Canada Postgraduate Scholarship (\$19,100/year)** 2001 – 2003
 - Awarded (based on a national competition) by the Natural Sciences and Engineering Research Council (NSERC) of Canada to individuals pursuing doctoral studies in science or engineering.
- **Ross Freeman Award for Technical Innovation (\$5,000 USD)** 2000
 - Highest innovation award given by Xilinx with 4 or 5 nominees each year and the winner chosen based on voting by the Xilinx engineering community.
 - Nominated again for Freeman award in 2001 and 2002 for different projects.
- **Software Engineering Innovation Award** 1999
 - One award given annually by Xilinx, based on peer voting within the software organization.
- **Ontario Graduate Scholarship (\$15,000)** 1996 – 1997

- **IEEE Thesis Award** 1995
– Awarded by University of Manitoba for best undergraduate thesis in Computer Engineering.
- **Sony Science Scholarship in Engineering (\$1,500)** 1994 – 1995
- **Don Craik Memorial Scholarship in Engineering (\$500)** 1992

Graduate Students Currently Supervised

Ph.D. Candidates:

- **Jason Luu (co-supervised by J. Rose)** 2010 – present
Topic: FPGA architecture, CAD and modeling; generic packing algorithms.
- **Marcel Gort** 2009 – present
Topic: Algorithms and architectures for reducing FPGA tool run-time.
- **Andrew Canis (co-supervised by S. Brown)** 2008 – present
Topic: High-level synthesis for FPGAs.
- **Safeen Huda** 2011 – present
Topic: FPGA architecture and circuits.

M.A.Sc. Candidates:

- **James (Jongsok) Choi (co-supervised by S. Brown)** 2009 – present
Topic: SoC and memory architecture for FPGA-based processor/accelerator systems.
- **Steven Gurfinkel (co-supervised by N. Enright Jerger)** 2011 – present
Topic: Heterogeneous CPU/GPU computing architecture.
- **Tahir Diop** 2011 – present
Topic: Heterogeneous computing: compilers and architecture.

M.Eng. Candidates:

- **Edgar Mora-Sanchez** 2011 – present
Topic: Approximate/probabilistic circuits in FPGAs.

Graduate Students Previously Supervised

- **Bill Teng, M.A.Sc.** 2009 – 2011
Topic: Optimizing FPGA performance using latches and clock skew.
Current position: Achronix Semiconductor, Santa Clara, CA, USA.
- **Warren Shum, M.A.Sc.** 2009 – 2011
Thesis: Glitch Reduction and CAD Algorithm Noise in FPGAs.
Current position: Altera Corporation, Toronto, ON, Canada.
- **Mark Aldham, M.A.Sc., Co-supervised by S. Brown.** 2009 – 2011
Thesis: Low-Cost Hardware Profiling of Run-Time and Energy in FPGA Soft Processors.
Current position: Microsoft Corp., Redmond, WA, USA.
- **Jason Luu, M.A.Sc., Co-supervised by J. Rose.** 2009 – 2010
Thesis: A Hierarchical Description Language and Packing Algorithm for Heterogeneous FPGAs.
Current position: Ph.D. candidate, University of Toronto.

Undergraduate Students Supervised

- **Benjamin Hare (Engineering Science thesis)** 2011 – 2012
- **Jack Fu (Engineering Science thesis)** 2011 – 2012
- **Neil Issac and Keyi Shi (design project)** 2011 – 2012
- **Alex Liu (ECE summer researcher)** Summer 2011

• Stefan Hadjis (NSERC summer researcher)	Summer 2011
• Kevin Nam (NSERC summer researcher)	Summer 2011
• Anthony Hau, Gavin Lam, Juan Fuentes (design project)	2010 – 2011
• Ahmed Kammoona (NSERC summer researcher)	Summer 2010
• Victor Zhang (ECE summer researcher)	Summer 2010
• Karen Tam (Engineering Science thesis)	2009 – 2010
• Ali Rakhshanfar (Engineering Science thesis)	2009 – 2010
• Richelle Bernardo and Anahita Panthaky (design project)	2009 – 2010
• James Lee and Se-Hwan Gil (design project)	2009 – 2010
• Chirag Ravishankar (NSERC summer researcher)	Summer 2009
• Safeen Huda and Muntasir Mallick (design project)	2008 – 2009
• Alvin Lui and Stephan Massin (design project)	2008 – 2009
• Safa Mahmood (Engineering Science thesis)	2008 – 2009

Invited Talks and Lectures

- **J.H. Anderson**, “FPGA-based high performance computing,” Fujitsu Laboratories Ltd., Kawasaki, Japan, July 2011.
- **J.H. Anderson**, “LegUp: High-level synthesis – status and research directions,” Ritsumeikan University, Kusatsu, Japan, July 2011.
- **J.H. Anderson**, “LegUp: High-level synthesis – status and research directions,” University of Waterloo, Waterloo, ON, July 2011.
- **J.H. Anderson**, “LegUp: High-level synthesis for FPGA-based processor/accelerator systems,” University of Tokyo, Tokyo, Japan, January 2011.
- **J.H. Anderson**, “Graduate studies and research,” Professional Engineers Ontario Student Conference, Toronto, ON, November 2010.
- **J.H. Anderson**, “Raising FPGA logic density and energy-efficiency,” Tabula Corp, Santa Clara, CA, February 2010.
- **J.H. Anderson**, “Introduction to FPGAs and future research directions,” Fujitsu Research Labs, Kawasaki, Japan, January 2010.

Grants, Contracts and Donations

• NSERC Collaborative Research and Development Grant (lead-PI) – \$127,500 Annual amount: \$42,500.	2012 – 2015
• Altera Industrial Funds (co-PI w. Brown) – \$105,000	2010 – 2013
• Fujitsu Research Labs (co-PI w. Enright Jerger and Sheikholeslami) – \$130,000	2011 – 2012
• Connaught New Researcher (PI) – \$10,000	2011
• NSERC Discovery Grant (PI) – \$230,000 Annual amount: \$46,000.	2009 – 2014
• NSERC Engage Grant (AMD) (co-PI w. Enright Jerger) – \$25,000	2011
• AMD Industrial Funds (co-PI w. Enright Jerger) – \$20,000	2011
• Altera Industrial Funds (co-PI w. Brown) – \$21,500	2009
• NSERC Collaborative Research and Development Grant (lead-PI) – \$33,500	2009 – 2011
• Xilinx Equipment Grant (Virtex-5 FPGA Boards) – value \$8,000	2009
• CFI/MRI Infrastructure Grant (co-PI w. Tate, Enright Jerger) – \$748,000 Grant is approved by CFI; approved by MRI. Yearly release of funds to be determined.	2010 – 2014
• Connaught New Faculty (PI) – \$10,000	2008
• University of Toronto Start-Up (PI) – \$100,000	2008

Scholarly and Professional Service Activities

- **Program Co-Chair, IEEE Int'l Conf. on Field Programmable Technology (FPT)** 2012
- **Technical Editor, IEEE Int'l Solid State Circuits Conference (ISSCC)** 2012
- **Local Arrangements Chair and Webmaster, IEEE Symp. on FCCM (FCCM)** 2012
- **Associate Editor, Integration, The VLSI Journal (Elsevier)** 2011
- **Design Competition Chair, IEEE Int'l Symp. on Field Programmable Technology (FPT)** 2011
- **Publicity Chair, IEEE Symp. on Field Programmable Custom Computing Machines (FCCM)** 2011
- **Workshop Chair, ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2009
- **Technical Program Committee**
 - ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA) 2009 – 2012
 - IEEE Int'l Conference on Field Programmable Custom Computing Machines (FCCM) 2011 – 2012
 - IEEE Int'l Conference on Field Programmable Technology (FPT) 2010 – 2012
 - IEEE Int'l Conference on Field-Programmable Logic and Applications (FPL) 2005 – 2011
 - Int'l Symposium on Applied Reconfigurable Computing (ARC) 2012
 - IEEE Int'l Conference on VLSI (VLSI-SoC) 2011
 - IEEE Int'l Conference on Computer-Aided Design (ICCAD) 2007 – 2008
 - IEEE Int'l Symposium on Circuits and Systems (ISCAS) Review Committee 2010 – 2011
 - IEEE Reconfigurable Architectures Workshop (RAW) 2009 – 2010
- **Session Chair, IEEE Int'l Conference on Field Programmable Logic (FPL)** 2009,2011
- **Session Chair, IEEE Int'l Conference on Field-Prog. Custom Computing Machines (FCCM)** 2011
- **Session Chair, IEEE Int'l Conference on Computer-Aided Design (ICCAD)** 2007

Professional Memberships and Licenses

- **Member of IEEE**
- **Member of ACM**
- **Licensed Professional Engineer (P.Eng.) in Ontario**

Interests, Activities and Personal Information

- **Interests:** Travel, wine, international films, public radio, jogging, reading, learning about different ethnic foods and cultures.
- **Music:** Grade 9 Royal Conservatory of Music piano certification, music history and harmony.
- **Nationality:** Canadian.
- **Personal:** Born in Winnipeg, Canada. Traveled extensively in Canada and USA. Also traveled in Europe and Asia. Lived and worked in the San Francisco Bay Area (California, USA) for 5 years.