Stereo-Vision circuit description, Aug 2002,
Ahmad Darabiha

This design contains four top level circuits: sv_chip0.vhd, sv_chip1.vhd, sv_chip2.vhd and sv_chip3.vhd each of them built by one Virtex2000E fpga chip. This design is hierarchical and the sub-circuits can be used as smaller benchmarks.

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summary of the design for sv_chip0.vhd of stereo vision system.
A. Darabiha, Aug, 2002.

synthesized by Synplicity version 7.0.0
placed and routed by Xilinx par v4.1.03i

Target device Xilinx V2000E

Number of Slices: 16,892 out of 19,200 87%

Number of Slice Flip Flops: 32,424 out of 38,400 84%

Total Number 4 input LUTs: 25,382 out of 38,400 66%

Number of Block RAMs: 42 out of 160 26%

Total equivalent gate count for design: 3,761,738

here is the hierarchy of the circuit:
(.edn files are Xilinx format for EDIF 2 0 0 netlist file. They are generated from Xilinx Core Generator and are instantiated in the circuit and declared as balck boxes for synplicity)

- sv_chip0.vhd
  - |- combine_res.vhd
  - |- v_fltr_496.vhd
  - | |- my_fifo_496.edn
  - |
  - |- v_fltr_316.vhd
  - | |- my_fifo_316.edn
  - |
  - |- lp_fltr_v1.vhd
  - | |-my_fifo_359.edn
  - |
  - |- lp_fltr_v2.vhd
  - | |- my_fifo_179.edn
  - |

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|- lp_fltr_v4.vhd
|       |- my_fifo_89.edn
|
|- scaler.vhd
|       |- scl_h_fltr.vhd
|       |       |- sh_reg_1.vhd
|       |
|       |- scl_v_fltr.vhd
|               |- my_fifo_496.edn
|
|- wrapper_qs_intr_5_20.vhd
|       |- quadintr_5_20.vhd
|       |- my_ram.edn
|
|- wrapper_qs_intr_10_20.vhd
|       |- quadintr_10_20.vhd
|       |- my_ram.edn
|
|- find_max.vhd
|- lp_fltr.vhd
|- my_fifo_1.edn
|- my_fifo_2.edn
|- port_bus_1to0_1.vhd
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summary of the design for sv_chip1.vhd of stereo vision system.
A. Darabiha, Aug, 2002.

synthesized by Synplicity version 7.0.0
placed and routed by Xilinx par v4.1.03i

Target device Xilinx V2000E

Number of Slices: 19,198 out of 19,200 99%

Number of Slice Flip Flops: 30,961 out of 38,400 80%

Total Number 4 input LUTs: 16,709 out of 38,400 43%

Number of Block RAMs: 0 out of 160 0%

Total equivalent gate count for design: 475,100

here is the hierarchy of the circuit:
(.edn files are Xilinx format for EDIF 2 0 0 netlist file. They are generated from Xilinx Core Generator and are instantiated in the circuit and declared as balck boxes for synplicity)

- sv_chip1.vhd
  - |- port_bus_2to1_1.vhd
  - |- wrapper_norm_corr_20.vhd
  - | |- wrapper_core_20.vhd
  - | | |- sh_reg.vhd
  - | | |- corr.vhd
  - | | | |- my_mult_8.edn
  - | |- wrapper_norm.vhd
  - | | |- my_div_16.edn
  - |
  - |- wrapper_norm_corr_10.vhd
  - | |- wrapper_corr_10.vhd
  - | | |- sh_reg.vhd
  - | | |- corr.vhd
  - | | | |- my_mult_8.edn
  - | |- wrapper_norm.vhd
  - | | |- my_div_16.edn
  - |
  - |- wrapper_norm_corr_5_seq.vhd
  - | |- wrapper_corr_5_seq.vhd
  - | | |- sh_reg.vhd
  - | | |- corr_seq.vhd
  - | | | |- my_mult_8_slow.edn
  - | |- wrapper_norm_seq.vhd
  - | | |- my_div_16_slow.edn
  - |
  - |- port_bus_1to0.vhd

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summary of the design for sv_chip2.vhd of stereo vision system.
A. Darabiha, Aug, 2002.

synthesized by Synplicity version 7.0.0
placed and routed by Xilinx par v4.1.03i

Target device Xilinx V2000E

Number of Slices:	19,198 out of 19,200	99%

Number of Slice Flip Flops: 18,020 out of 38,400 46%

Total Number 4 input LUTs: 23,151 out of 38,400 60%

Number of Block RAMs: 150 out of 160 93%

Total equivalent gate count for design: 3,865,725

here is the hierarchy of the circuit:
(.edn files are Xilinx format for EDIF 2 0 0 netlist file. They are generated from Xilinx Core Generator and are instantiated in the circuit and declared as balck boxes for synplicity)

- sv_chip2.vhd
  - h_fltr.vhd
    - my_fir_f1.edn
    - my_fir_f2.edn
    - my_fir_f3.edn
    - my_fir_h1.edn
    - my_fir_h2.edn
    - my_fir_h3.edn
    - my_fir_h4.edn
    - steer_fltr.vhd
  - v_fltr
    - fltr_compute_f1.vhd
      - mult_const_f1_2.edn
      - mult_const_f1_3.edn
      - mult_const_f1_4.edn
      - mult_const_f1_5.edn
    - fltr_compute_f2.vhd
      - mult_const_f2_2.edn
      - mult_const_f2_3.edn
      - mult_const_f2_4.edn
      - mult_const_f2_5.edn
    - fltr_compute_f3.vhd
      - mult_const_f3_2.edn
      - mult_const_f3_3.edn
      - mult_const_f3_4.edn
      - mult_const_f3_5.edn
      - mult_const_f3_6.edn

```
|       |       |- mult_const_f3_7.edn
|       |       |- mult_const_f3_8.edn
|       |
|       |- fltr_compute_h1.vhd
|       |       |- mult_const_h1_2.edn
|       |       |- mult_const_h1_3.edn
|       |       |- mult_const_h1_4.edn
|       |       |- mult_const_h1_5.edn
|       |       |- mult_const_h1_6.edn
|       |       |- mult_const_h1_7.edn
|       |       |- mult_const_h1_8.edn
|       |
|       |- fltr_compute_h2.vhd
|       |       |- mult_const_h2_2.edn
|       |       |- mult_const_h2_3.edn
|       |       |- mult_const_h2_4.edn
|       |       |- mult_const_h2_5.edn
|       |
|       |- fltr_compute_h3.vhd
|       |       |- mult_const_h3_2.edn
|       |       |- mult_const_h3_3.edn
|       |       |- mult_const_h3_4.edn
|       |       |- mult_const_h3_5.edn
|       |       |- mult_const_h3_6.edn
|       |       |- mult_const_h3_7.edn
|       |       |- mult_const_h3_8.edn
|       |
|       |- fltr_compute_h4.vhd
|       |       |- mult_const_h4_2.edn
|       |       |- mult_const_h4_3.edn
|       |       |- mult_const_h4_4.edn
|       |       |- mult_const_h4_5.edn
|       |
|       |- fifo.vhd
|
|- port_bus_2to1.vhd
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summary of the design for sv_chip3.vhd of stereo vision system.
A. Darabiha, Aug, 2002.

synthesized by Synplicity version 7.0.0
placed and routed by Xilinx par v4.1.03i

Target device Xilinx V2000E

Number of Slices: 109 out of 19,200 1%

Number of Slice Flip Flops: 71 out of 38,400 1%

Total Number 4 input LUTs: 169 out of 38,400 1%

Number of Block RAMs: 0 out of 160 0%

Total equivalent gate count for design: 2,148

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