University of Toronto, Faculty of Applied Science and Engineering
Department of Electrical and Computer Engineering

ECE 1387F- CAD for Digital Circuit Synthesis and LayoutHandout #2

September 1999 J. Rose

Reading List for Paper and Course

In general, the places to look are for CAD papers are:

- IEEE Transactions on Computer Aided Design of Circuits and Systems.
- The Internation Conference on Computer-Aided Design (ICCAD).
- The Design Automation Conference (DAC). You can find the last three years of DAC proceedings on line at http://www.sigda.acm.org/Dac/index.htm
- The European Design Automation Conference (EDAC).
- The International Conference on Computer Design (ICCD).

Below is a partial list of papers organized by the specific CAD area.

Also, if you go to the www.ieee.org, and are a member of the IEEE, there are lots of searchable databases. The UofT also has a searchable database.

1.0 Partitioning

1. Charles J. Alpert, Jen-Hsin Huang, Andrew B. Kahng, “Multilevel Circuit Partitioning”, Proc DAC 97, pp 530.
2. J. Cong, H.P. Li, S.K. Lim, T. Shibuya, D. Xu, “Large Scale Circuit Partitioning With Loose/Stable Net Removal And Signal Flow Based Clustering,” , Proc ICCAD 97, Nov 1997, pp. 441.
3. H. Yang, D.F. Wong, “Efficient Netowrk Flow Based Min-Cut Balanced Partitioning,” Proc. ICCAD ‘94, pp. 50-55.
4. J. Cong, L. Hagen, A. Kahng, ‘‘Net Partitions Yield Better Module Partitions,’’ Proc 29th Design Automation Conference, pp. 47-52, June 1992.
5. B.W. Kernighan and S. Lin, “An Efficient Heuristic Procedure for Partitioning Graphs” Bell System Technical Journal, Vol. 49, No. 2, pp.291-307, Feb. 1970.
6. C.M. Fiduccia and R.M. Mattheyses, “A Linear-Time Heuristic for Improving Network Partitions”, 19th ACM/IEEE Design Automation Conference, pp. 175-181, pp. 1982.

7. S. Kirkpatrick, C.D. Gelatt, Jr., M.P. Vecchi, “Optimization by Simulated Annealing”, Science, Vol. 220, No. 4598, pp. 671-680, May 1983.

2.0 Placement

1. A. Sangiovanni-Vincentelli, “Automatic Layout of Integrated Circuits”, in Design systems for VLSI Circuits: Logic Synthesis and Silicon Compilation, G. De Micheli, A. Sangiovanni-Vincentelli and P. Antognetti, Eds., Martinus Nijhoff Publishers, pp. 113-196, 1987.

2. Hans Eisenmann, Frank M. Johannes, “Generic Global Placement and Floorplanning” Proc. 1998 DAC, pp. 269.

3. C.J. Alpert, T. Chan, D.J.-H. Huang, I. Markov, K. Yan, Quadratic Placement Revisited Proc. DAC ‘97, pp 75.

4. S.R. Arikati, R. Varadarajan, “A Signature Based Approach to Regularity Extraction”, Proc ICCAD ‘97 pp. 542,

5. M. Hanan, J.M. Kurtzberg, “Placement Techniques”, in Design Automation of Digital Systems, Vol. 1, M. Breuer, Ed., Englewood Cliffs, NJ: Prentice Hall, Chapter 5, 1972.

6. M.A. Breuer, “Min-Cut Placement”, Design Automation & Fault-Tolerant Computing, vol. 1, no. 4, pp. 343-362, Oct. 1977.

7. A. E. Dunlop and B. W. Kernighan, “A Placement Procedure for Layout of VLSI Circuits”, IEEE Trans. CAD of ICs and Systems, vol. CAD-4, no. 1, pp. 92-98, Jan. 1985.

8. J. P. Blanks, “Near-Optimal Quadratic-Based Placement for a Class of IC Layout Problems”, IEEE Circuits and Devices Magazine, pp. 31-37, Sept. 1985.

9. L. Sha, R. Dutton, “An Analytical Algorithm for Placement of Arbitrarily Sized Rectangular Blocks,” Proc. 1985 Design Automation Conference, pp. 602-607.

10. D.W. Jepsen and C.D. Gelatt, Jr., “Macro Placement by Monte Carlo Annealing”, Proc. 1983 IEEE Int’l Conf. on Computer Design, pp 495-498, Nov. 1983.

11. D. Wong and C. Liu, “A New Algorithm for Floor-plan Design”, Proc. 23rd ACM/ IEEE Design Automation Conference, pp. 101-107, June 1986.

12. N. Togawa, M. Sato, T. Ohtsuki, “Maple: A simulataneous Technology Mapping, Placement and Global Routing Algorithm for Field-Programmable Gate Arrays,” Proc. ICCAD ‘94, pp. 156-163.

13. C. Cheng, “RISA: Accurate and Efficient Placement and Routability Modeling,” Proc. ICCAD ‘94, pp 690-696.

3.0 Routing

1. J. Soukup, “Circuit Layout”, Proceedings of the IEEE, vol. 69, no. 10, pp. 1281-1304, Oct. 1981.

2. Charles J. Alpert, Anirudh Devgan,” Wire Segmenting for Improved Buffer Insertion”, Proc. DAC ‘97, pp 588.

3. T. Ohtsuki, “Maze-Running and Line Search Algorithms”, in Layout Design and Verification, Advances in CAD, Vol. 4, T. Ohtsuki, Ed., Elsevier Science Publishing Co., pp. 99-132, 1986.

4. D. Hightower, “The Lee Router Revisited”, Proc. IEEE Int’l Conf on Computer Design, pp. 136-139, Oct 1983.

5. E. S. Kuh and M. Marek-Sadowska, “Global Routing”, in Layout Design and Verification, Advances in CAD, Vol. 4, T. Ohtsuki, Ed., Elsevier Science Publishing Co., pp. 169-198, 1986.

6. J. Soukup and J.C. Royle, “On Hierarchical Routing”, Journal of Digital Systems, vol. V, no. 3, pp. 265-289, 1981.

7. S. Brown, J.S. Rose, Z. Vranesic, “A Detailed Router for Field Programmable Gate Arrays” IEEE Transactions on Computer-Aided Design of Circuits and Systems, Vol. 11, No. 5, May 1992, pp. 620-628.

8. M. Burstein, “Channel Routing”, in Layout Design and Verification, Advances in CAD, Vol. 4, T. Ohtsuki, Ed., Elsevier Science Publishing Co., pp. 133-168, 1986.

9. A. Hashimoto and J. Stevens, “Wire Routing by Optimizing Channel Assignment within Large Apertures”, Proc. 8th SHARE/ACM/IEEE Design Automation Workshop, pp. 155-179, 1971.

10. D. Deutch, “A Dogleg Channel Router”, Proc. 13th ACM/IEEE Design Automation Conference, pp. 425-433, 1976.

11. T. Yoshimura and E. Kuh, “Efficient Algorithms for Channel Routing”, IEEE Trans, CAD of ICS and Systems, vol. CAD-1, pp. 25-34, Jan. 1982.

12. R. Rivest and C. Fiduccia, “A Greedy Channel Router”, Proc. 19th ACM/IEEE Design Automation Conference, pp. 418-424, 1982.

13. M. Burstein and R. Pelavin, “Hierarchical Wire Routing”, IEEE Trans, CAD of ICS and Systems, vol. CAD-2, pp. 223-234, Oct. 1983.

4.0 Wirability Theory

1. W.R. Heller, C. George Hsi, W.F. Mikhail, “Wirability - Designing Wiring Space for Chips and Chip Packages,” IEEE Design & Test of Computers, vol. 1, no. 3, pp. 43-

51, Aug. 1984.

2. Heller, W.R., W.F. Mikhail, W.E. Donath, “Prediction of Wiring Space Requirements for LSI”, Jour. Design Automation and Fault Tolerant Computing, vol. 2, no. 2, pp. 117-144, May 1978.

3. W.E. Donath, “Placement and Average Interconnection Lengths of Computer Logic”, IEEE Trans. Circuits and Systems, vol CAS-26, pp. 272-277, April 1979.

4. M. Feuer, “Connectivity of Random Logic”, IEEE Trans Computers, vol. C-31, no. 1, pp. 29-33, Jan. 1982.

5. A. El Gamal, ‘‘Two-Dimensional Stochastic Model for Interconnections in Master Slice Integrated Circuits,’’ IEEE Transactions on Circuits and Systems Vol. CAS-28, No. 2, February 1981, pp. 127-138.

6. S. Sastry, A. Parker, “Stochastic Models for Wireability Analysis of Gate Arrays,” IEEE Trans. Computer-Aided Design, Vol. CAD-5 No. 1, January 1986, pp. 52-65.

5.0 Module Generators

1. M. Buric, “Design of Module Generators and Silicon Compilers”, in Design systems for VLSI Circuits: Logic Synthesis and Silicon Compilation, G. De Micheli, A. Sangiovanni-Vincentelli and P. Antognetti, Eds., Martinus Nijhoff Publishers, pp. 403-438, 1987.

2. R. Lipton et al, “ALI: A Procedural Language to Describe VLSI Layouts”, Proc, 19th ACM/IEEE Design Automation Conf., 1982.

3. R. Mayo and J. Ousterhout, “Pictures with parentheses: combining graphics and procedures in a VLSI layout tool,” Proc. 20th Design Automation Conf., June 1983.

4. D. Eddington et al., “CMOS Cell Compilers for Custom IC Design”, Proc. Custom IC Conf., pp. 512-517, 1984.

5. R. Mayo, “Mocha Chip: A System for the Graphical Design of VLSI Module Generators,” Proc. IEEE Int’l Conf. on CAD, pp. 74-77, Nov. 1986.

6.0 Logic Optimization

1. R. Brayton “Algorithms for Multi-Level Logic Synthesis and Optimization,” in Design systems for VLSI Circuits: Logic Synthesis and Silicon Compilation, G. De Micheli, A. Sangiovanni-Vincentelli and P. Antognetti, Eds., Martinus Nijhoff Publishers, pp. 197-248, 1987. or (shorter, but harder to read): R. Brayton, R. Rudell, A. Sangiovanni-Vincentelli, A. Wang, “MIS: A Multiple-Level Logic Optimization System,” IEEE Trans. Computer-Aided Design, Vol. CAD-6 No. 6, November 1986, pp. 1062-1081.

2. R.E. Bryant, “Graph-Based Algorithms for Boolean Function Manipulation,” IEEE

Trans. on Computers, Vol. C-35 No. 8, August 1986, pp. 677-691.

3. R.K. Brayton, et. al. Logic Minimization Algorithm for VLSI Synthesis, Kluwer Academic Publishers, Boston, 1984.

4. K.A. Bartlett, et. al “Multilevel Logic Minimization Using Implicit Don’t Cares,” IEEE Trans. Computer-Aided Design, Vol. CAD-7 No. 6, June 1988, pp. 723-740.

5. K. Bartlett et. al, “Synthesis and Logic Optimization under Timing Constraints,” IEEE Trans. Computer-Aided Design, Vol. CAD-5 No. 4, October 1986, pp. 582-596.

6. D.E. Wallace, M.S. Chandrasekhar, “High-Level Delay Estimation for Technology-Independent Logic Equations,” Proc. 1990 International Conference on Computer-Aided Design (ICCAD), pp. 188-191, November 1990.

7. A. Shen, A. Ghosh, S. Devadas, K. Keutzer, “On Average Power Dissipation and Random Patter Testability of CMOS Combinational Logic Networks,” Proc. ICCAD ‘92, pp. 402-407.

8. D. Brand, A. Drumm, SKundu, P.Narain, “Incremental Synthesis,” Proc. ICCAD ‘94, pp. 14-17.

9. S. Iman, M. Pedram, “Multi-Level Network Optimization for Low Power,” Proc. ICCAD ‘94, pp. 372-377.

7.0 Technology Mapping

1. K. Keutzer, ‘‘DAGON: Technology Binding and Local Optimization by DAG Matching,’’ Proc. 24th Design Automation Conference, June 1987, pp. 341-347.

2. E.Detjens et. al, ‘‘Technology Mapping in MIS’’, Proc. ICCAD 87, Nov 1987, pp. 116-119.

3. R.J Francis, J. Rose, Z. Vranesic, “Chortle-crf: Fast Technology Mapping for Lookup Table-Based FPGAs,” 28th ACM/IEEE Design Automation Conference, June 1991, pp. 227-233.

4. R. Lisanke, F. Brglez, G. Kedem, ‘‘McMAP: A Fast Technology Mapping Procedure for Multi-Level Logic Synthesis,’’ Proc. ICCD, pp. 252-256, October 1988.

8.0 Sequential Logic Synthesis

1. Naresh Maheshwari, Sachin S. Sapatnekar, “An Improved Algorithm For Minimum-Area Retiming”, Proc DAC ‘97 pp 2.

2. S. Devadas et. al., “MUSTANG: State Assignment of Finite State Machines Targeting Multilevel Lobic Implementations,” IEEE Trans. Computer-Aided Design, Vol. CAD-7, No.12, December 1988, pp. 1290-1300.

3. G. DeMicheli, “Synthesis of Control Systems,” in Design systems for VLSI Circuits: Logic Synthesis and Silicon Compilation, G. De Micheli, A. Sangiovanni-Vincentelli and P. Antognetti, Eds., Martinus Nijhoff Publishers, pp. 327-364, 1987.

4. Try all of IEEE Trans. Computer-Aided Design, Vol CAD-10, No. 1, January 1991, including the following two:.

5. K. Bartlett, G. Borriello, S. Raju, “Timing Optimization of Multiphase Sequential Logic”, IEEE Trans. Computer-Aided Design, Vol CAD-10, No. 1, January 1991, pp. 51-62.

6. S. Malik et. al, “Retiming and Resynthesis: Optimizing Sequential Networks with Combinational Techniques,” IEEE Trans. Computer-Aided Design, Vol CAD-10, No. 1, January 1991, pp. 74-84.

7. N. SHenoy, R. Rudell, “Efficient Implementation of Re-timing”, Proc. ICCAD ‘94, pp. 226-233.

8. J. Grodstein et. al, “Optimal Latch Mapping and Retiming Within a Tree,” Proc. ICCAD ‘94, pp. 242-246.

9.0 High-Level Synthesis

1. M. McFarland, A. Parker, R. Camposano, “Tutorial on High-Level Synthesis,” Proc. 25th ACM/IEEE Design Automation Conference, pp. 330-336, 1988. (contains many references).

2. C-J. Tseng, D.P. Siewiorek, “Automated Synthesis of Data Paths in Digital Systems,” IEEE Trans. Computer-Aided Design, Vol. CAD-5, No.3, July 1986, pp. 379-395.

3. P.G. Paulin, J.P. Knight, “Force-Directed Scheduling for the Behavioral Synthesis of ASICs,” IEEE Trans. Computer-Aided Design, Vol. CAD-8 No. 6, June 1989, pp. 661-679.

4. P.G. Paulin, J.P. Knight, “Scheduling and Binding Algorithms for High-Level Synthesis” Proc. 26th ACM/IEEE Design Automation Conference, 1989, pp. 1-6.

5. G. DeMicheli, D. Ku, “HERCULES - A System for High-Level Synthesis,” Proc. 25th ACM/IEEE Design Automation Conference, 1988, pp. 483-488.

6. H. Trickey, “Flamel: A High Level Hardware Compiler,” IEEE Trans. Computer-Aided Design, Vol. CAD-6 No. 2, March 1987, pp. 259-269.

7. For High-Level Synthesis, see also the special issue of IEEE, Design & Test, Vol 7, No. 5, October 1990.