Digital Logic Scope Tutorial for the BA31XX Labs.

November 12, 2006

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Note to readers

This provides a brief tutorial of the logic scope found in the BA31XX digital logic labs. The intended audience are students who have never used or have had limited use the logic scope. This document gives a very narrow perspective of the logic scope and is focused specifically to get ECE241 or ECE342 students through their labs and encourage them to use it for debugging. Full more advanced features, please refer to the user manual or check the reference section for other resources.

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Introduction to the Logic Scope

The logic scope is a powerful tool to help engineers identify and rectify problems within their digital design. There are two types of logic scopes found in each BA31XX lab. This includes the Hewlett Packard logic scope and Agilent logic scope. Each model will have an identifier on the front face panel of the device. The user interfaces are shown in Figure 1 and Figure 2. For the purposes of the labs, both are equivalent in functionality.

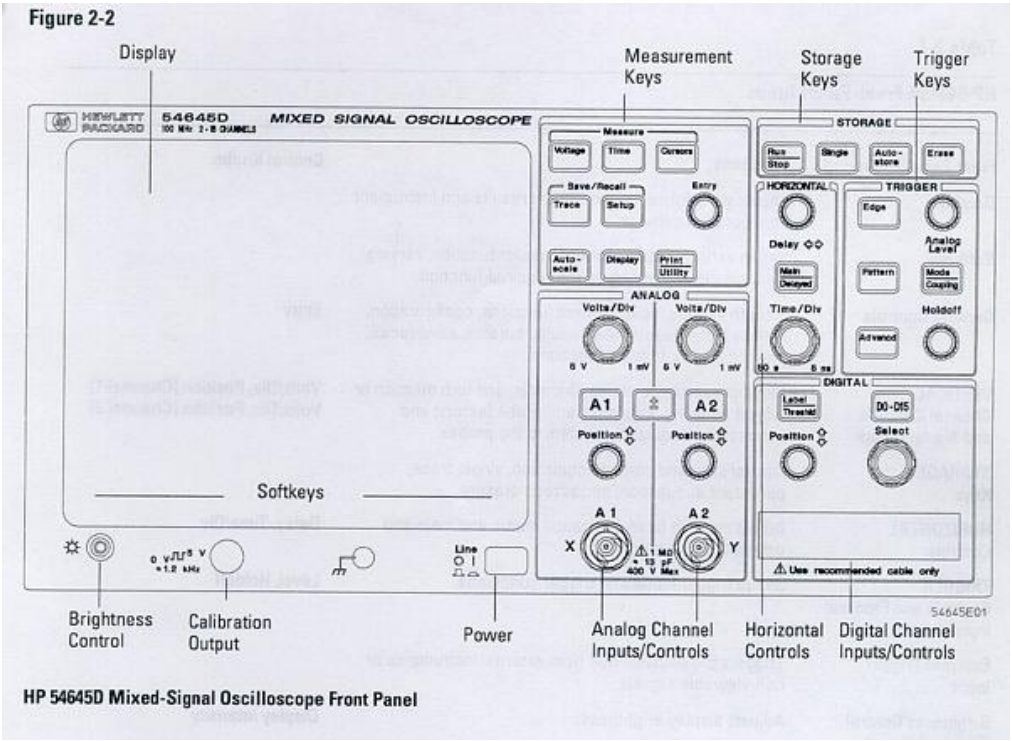


Figure 1 Illustration of the Hewlett Packard logic scope user interface.

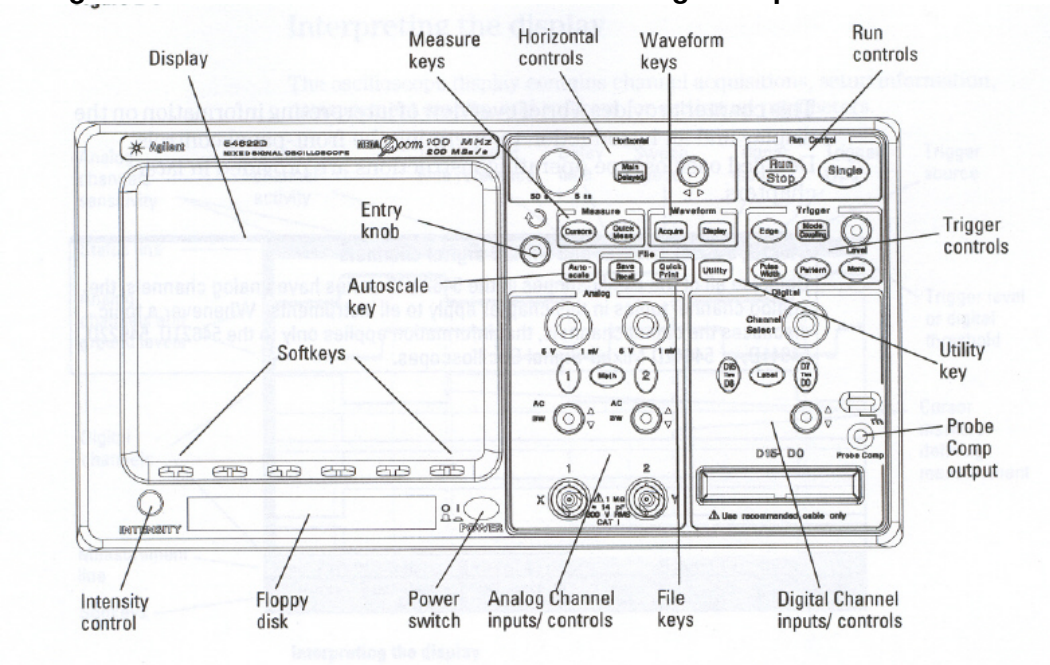


Figure 2 Illustration of the Agilent logic scope user interface.

For the purposes of the digital labs, you will only worry about the digital interface, labeled “Digital Channel – input/controls” and the trigger interface labeled “Trigger controls/keys” as shown in Figure 1 and Figure 2.

The first thing you’ll need to do is to connect your digital logic probes to the scope and turn the machine on. To connect the digital logic probes, take the probes out of the pack located on the top of the logic scopes and connect them to the digital channel inputs. This is illustrated in for the Hewlett Packard model, the Agilent model will look very similar.

Figure 3 Illustration of the logic scope digital probe attachment.

To turn on your scope, simply depress the “power” button.

Viewing a Signal

To view a signal, there are three main steps that you must take.

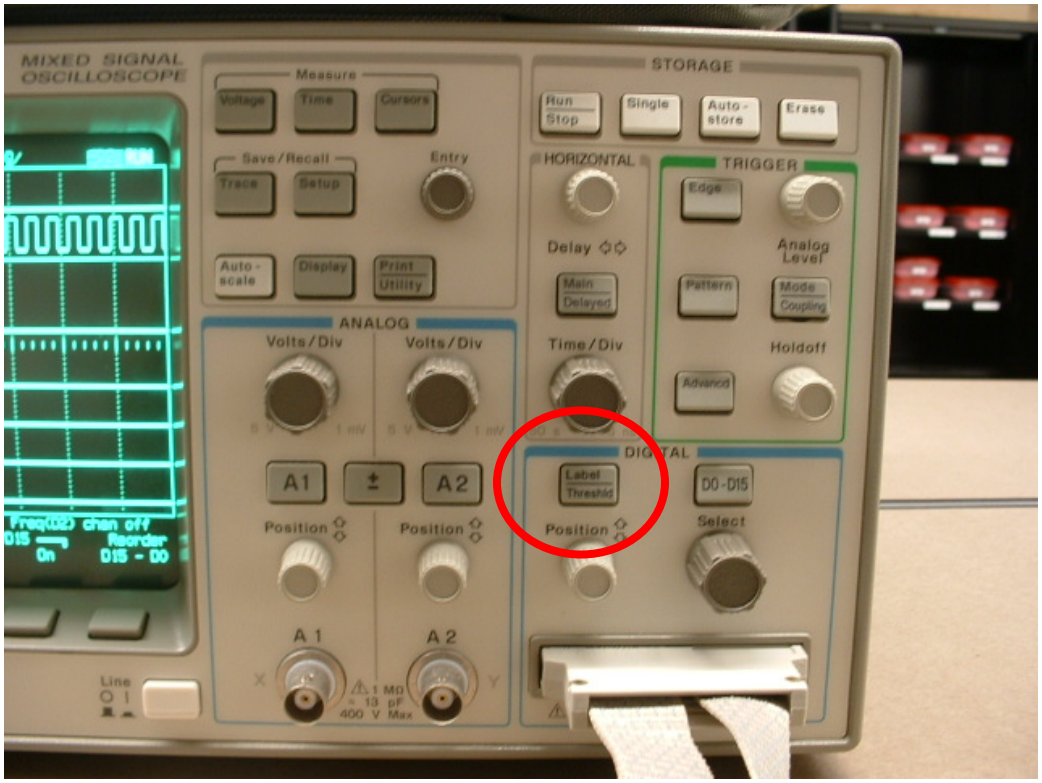
- Turn on your signals on the logic scope.
- Output the signal you want to view onto an output pin on the board.
- Attach a probe to the output pin you assigned your signal to.

View signals on logic scope

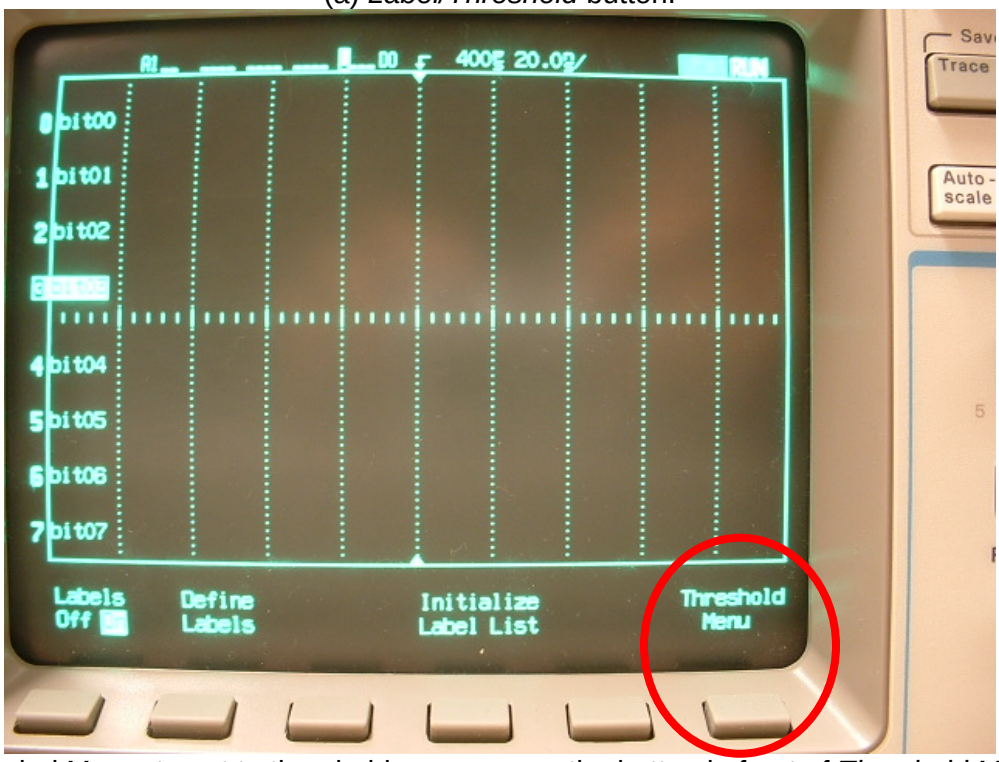
If your screen is blank, you will need to turn on your signals. Viewing signals on each model of the logic scope requires different steps, so please refer to the steps of your current model.

Hewlett Packard Model

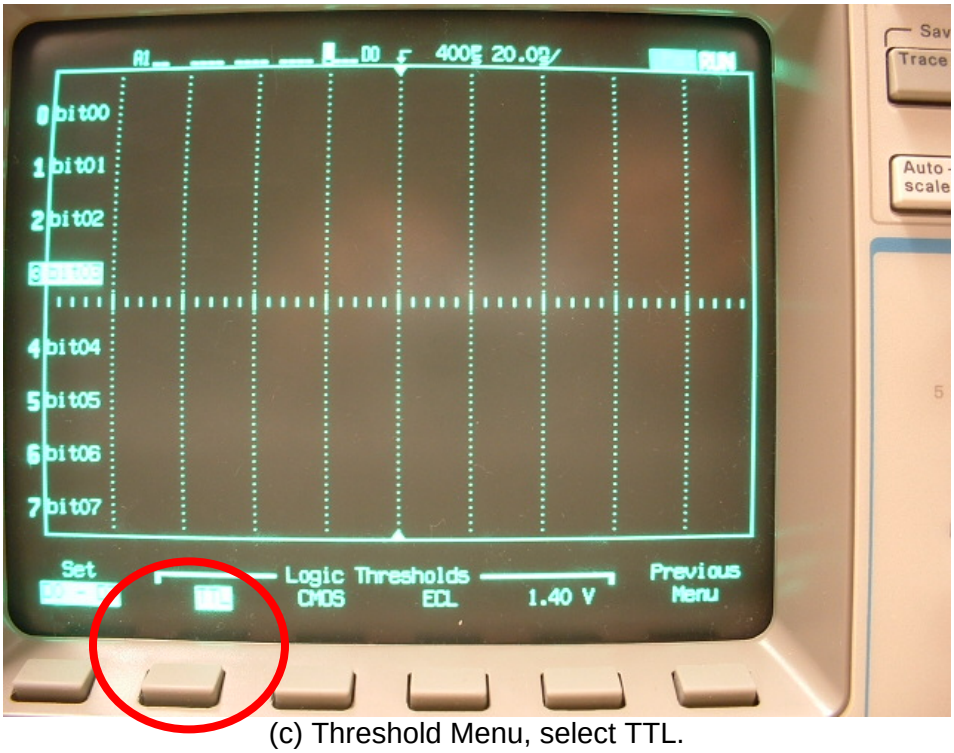
Before you can view signals on your logic scope, you should ensure that you threshold is set to TTL. The threshold mode defines the voltage ranges that represent a logical ‘1’ and logical ‘0’. To check your threshold, press the “Label/Threshold” button highlighted in Figure 4a. This will bring up a new menu on the logic screen as illustrated in Figure 4b. Press the button in front of “Threshold Menu” highlighted in Figure 4b. This will bring up a secondary menu as shown in Figure 4c. Once at the threshold menu, select the button in front of “TTL”. By default, most scopes will be already set to TTL, but some users change this from time to time.



(a) *Label/Threshold* button.



(b) Label Menu, to get to threshold menu, press the button in front of *Threshold Menu*.



(c) Threshold Menu, select TTL.

Figure 4 Location of threshold button and menu. (a) Highlight of the label/threshold button. (b) Label Menu (b) Threshold Menu.

After you ensured that your threshold is set to TTL, you can start viewing your logic signals. To turn on your signals on the logic scope, press the D0-D15 button as highlighted in Figure 5.

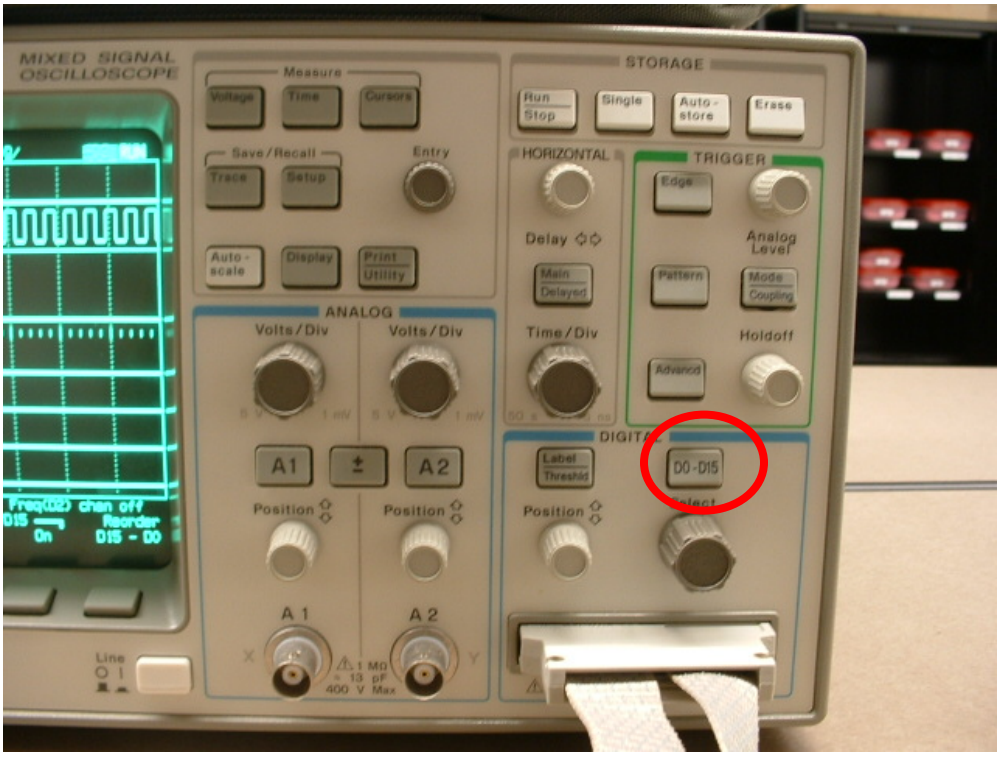
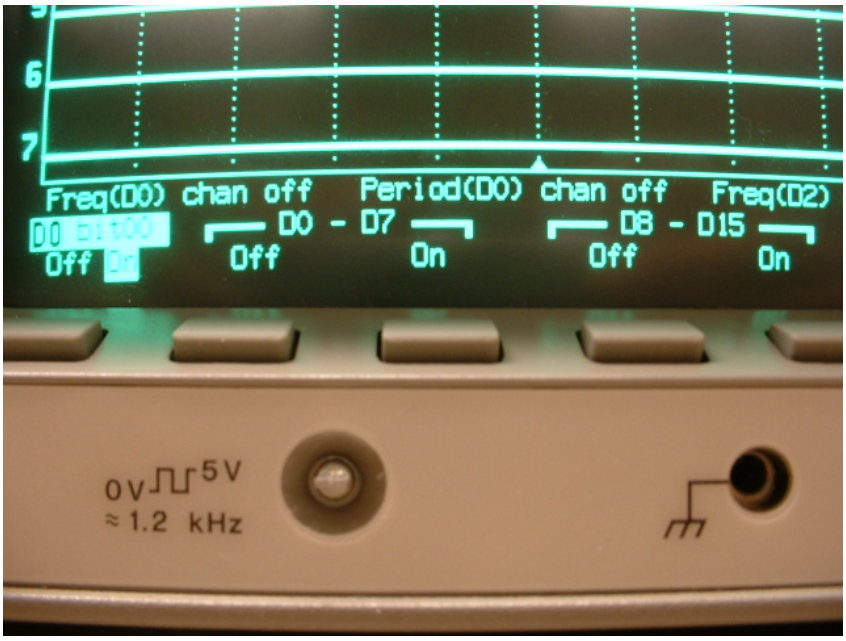
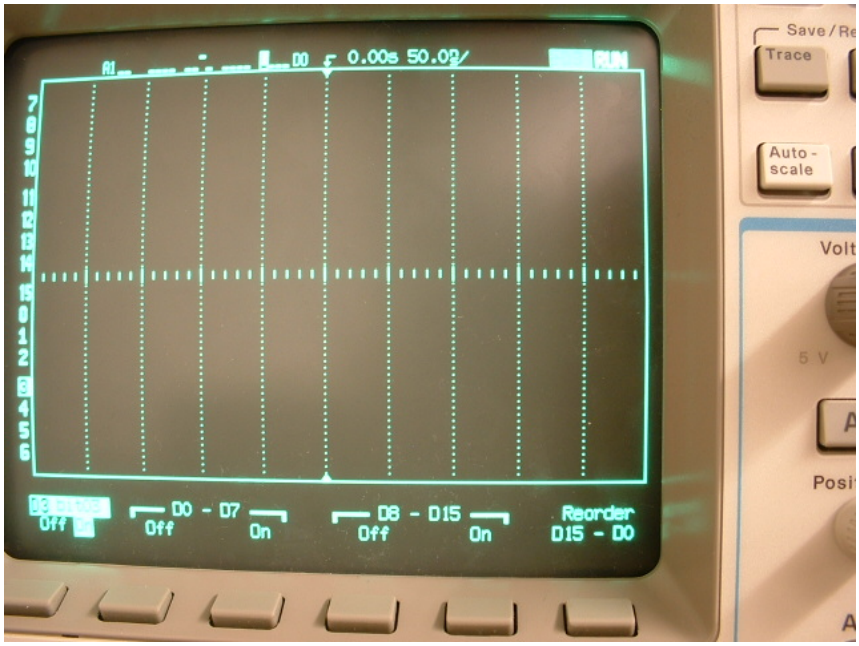


Figure 5 Illustration of D0-D15 button the Hewlett Packard logic scope.

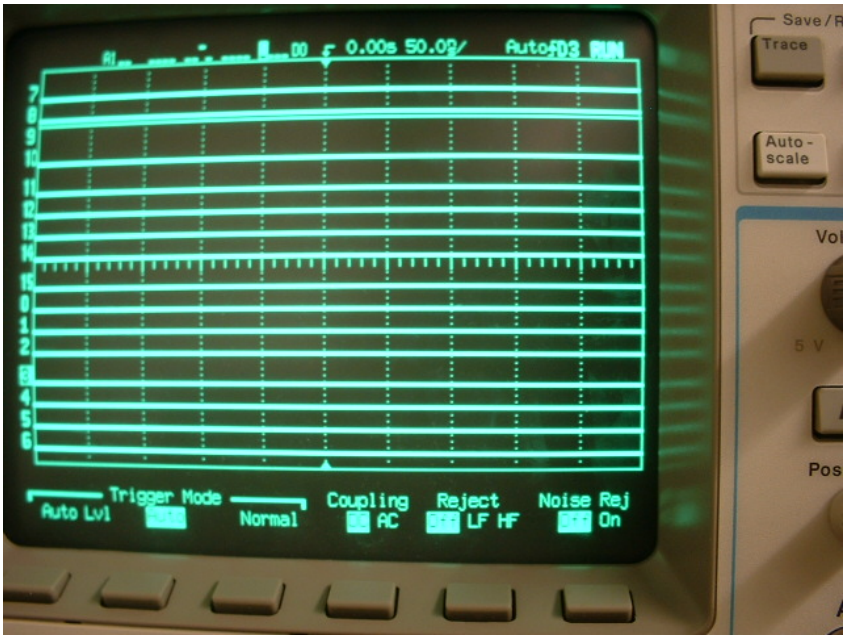
A submenu will appear on the screen afterwards, as shown in Figure 6a. Press the buttons in front of “on” to turn on the associated signals. This should turn on the signals as shown in Figure 6c. It may be possible that your signals will not appear, as shown in Figure 6b. In this case, you will need to change the trigger mode to “auto”. To do this, press the “mode coupling” button as shown in Figure 7a. A menu will pop up on the main screen as shown in Figure 7b. Here, press the button in front of “auto”.



(a)

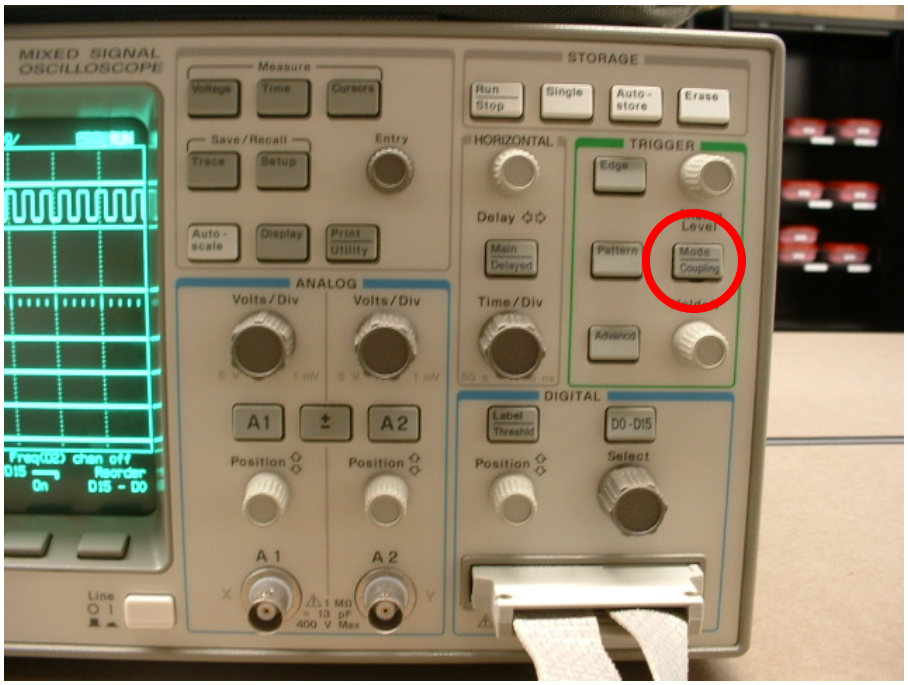


(b)

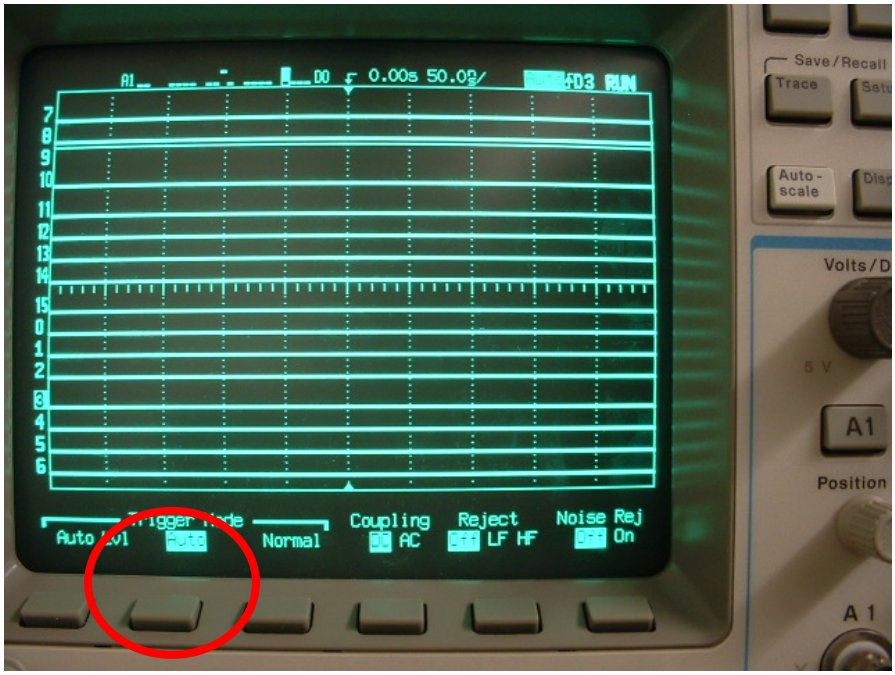


(c)

Figure 6 Illustration of turning on signals on the digital scope. (a) Digital pins menu (b) Empty screen with no signals showing (c) Signals showing.



(a) Location of mode coupling button.

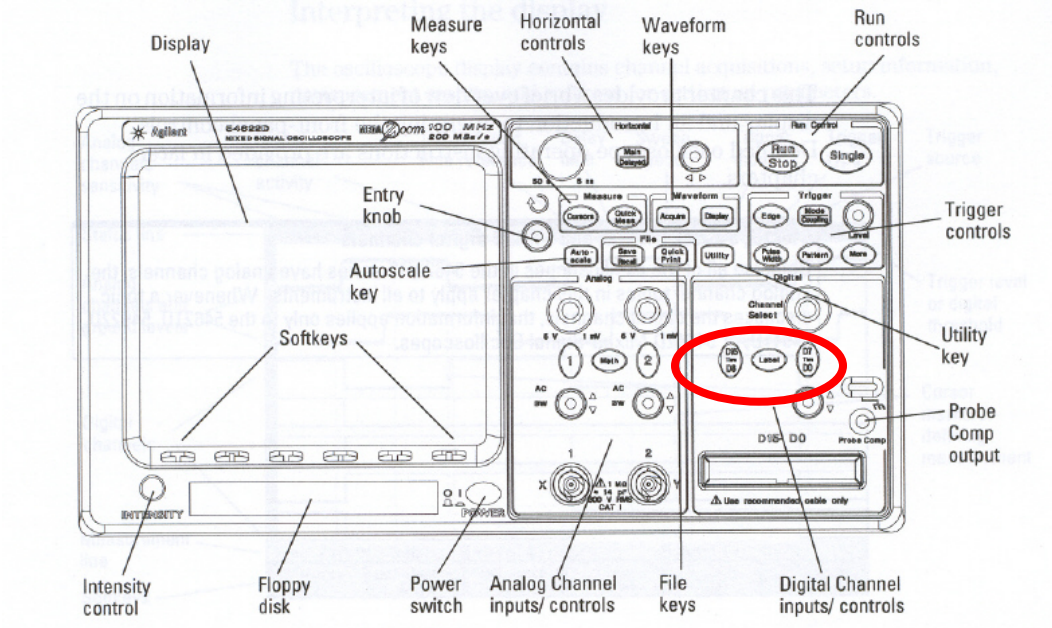


(b) Trigger mode menu.

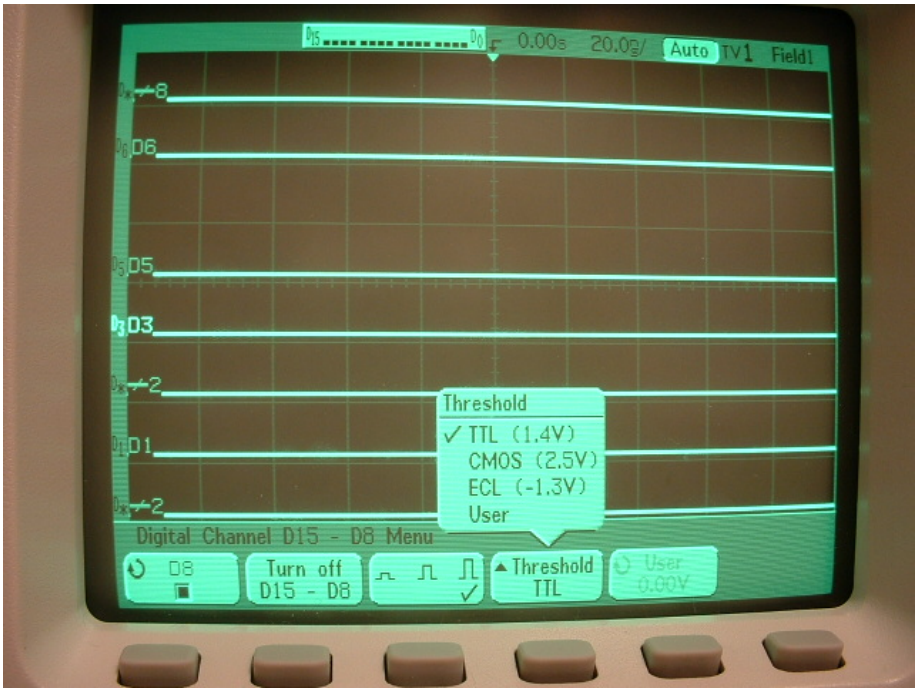
Figure 7 Illustration of the trigger mode menu. (a) Location of mode couple buttons (b) Trigger mode menu

Agilent Model

Before you can view signals on your logic scope, you should ensure that you threshold is set to TTL. The threshold mode defines the voltage ranges that represent a logical '1' and logical '0'. To check your threshold, press the "D7 thru D0" or "D15 thru D8" button highlighted in Figure 7a. This will bring up a new menu on the logic screen as illustrated in Figure 7b. Press the button in front of "Threshold" highlighted in Figure 7b until TTL is selected. By default, most scopes will be already set to TTL, but some users change this from time to time.



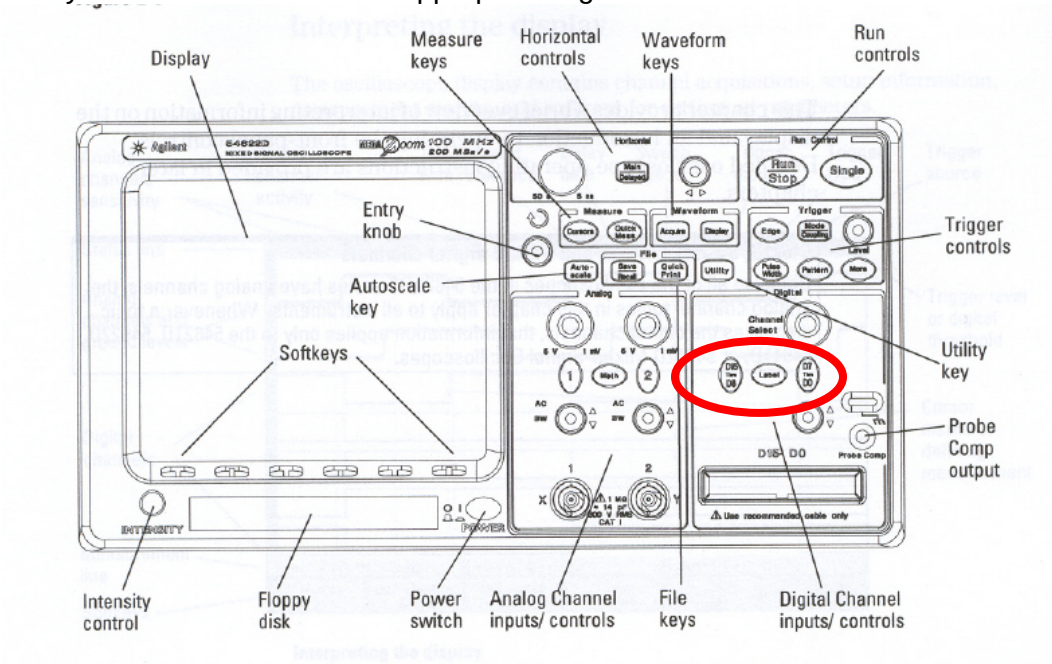
(a) Highlight of data line buttons.



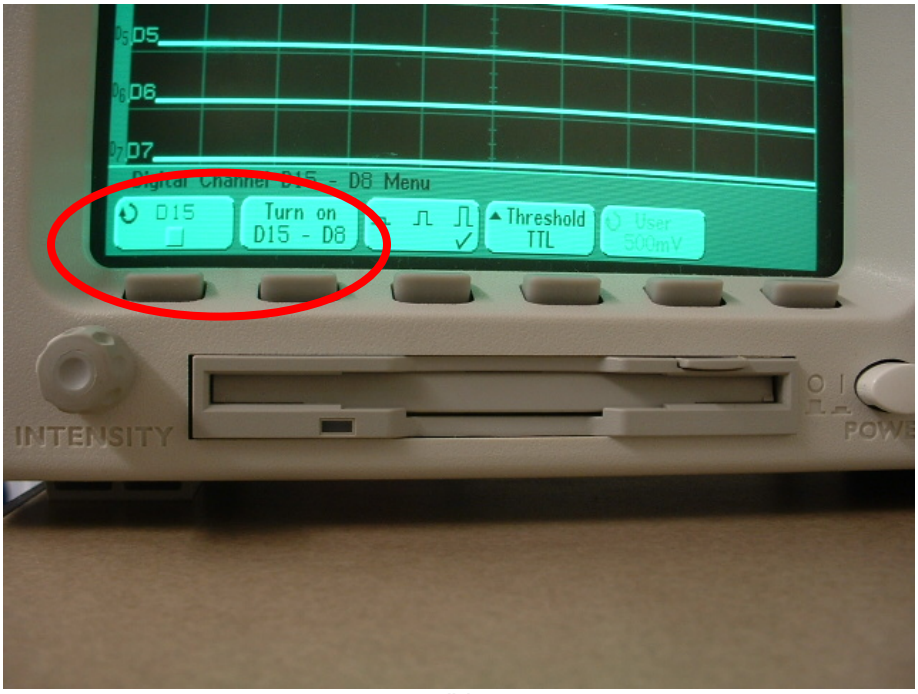
(b) Threshold menu

Figure 8 Changing your threshold mode on the logic scope. (a) Highlight of data line buttons. (b) Setting the threshold.

Once the threshold is set to TTL, you can turn on your signals. To turn on your signals, press the D0-D7 or D8-D15 button, as highlighted in Figure 9a. This will bring up a menu as shown in Figure 9b which will allow you to turn on and off the appropriate signals.



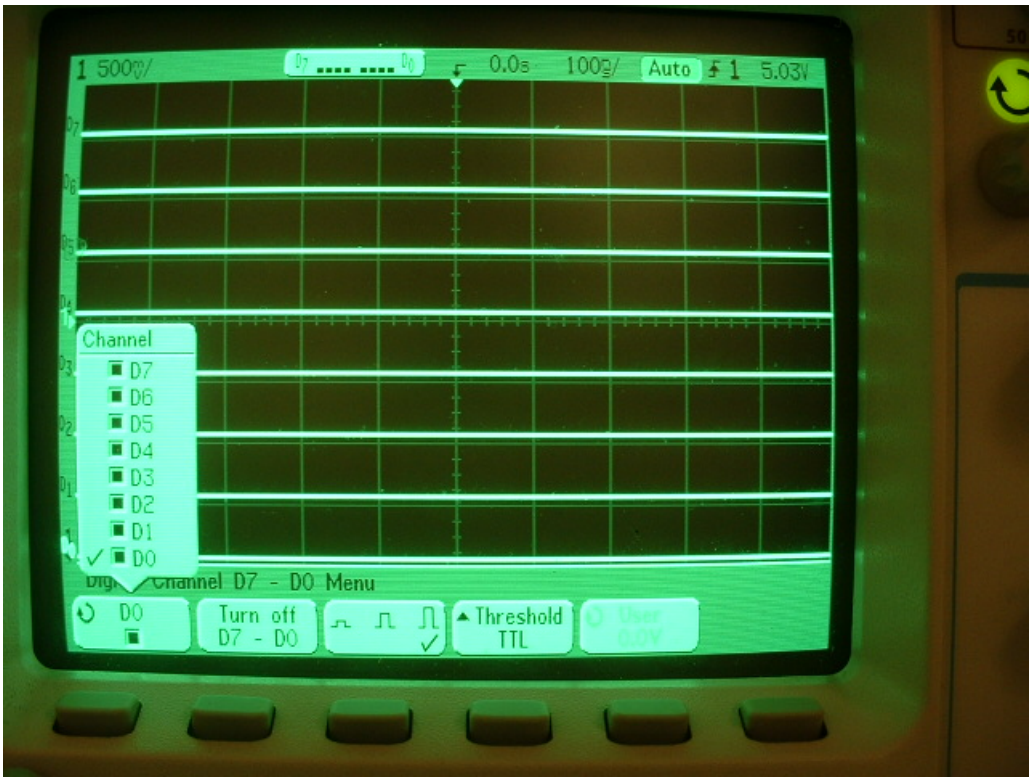
(a)



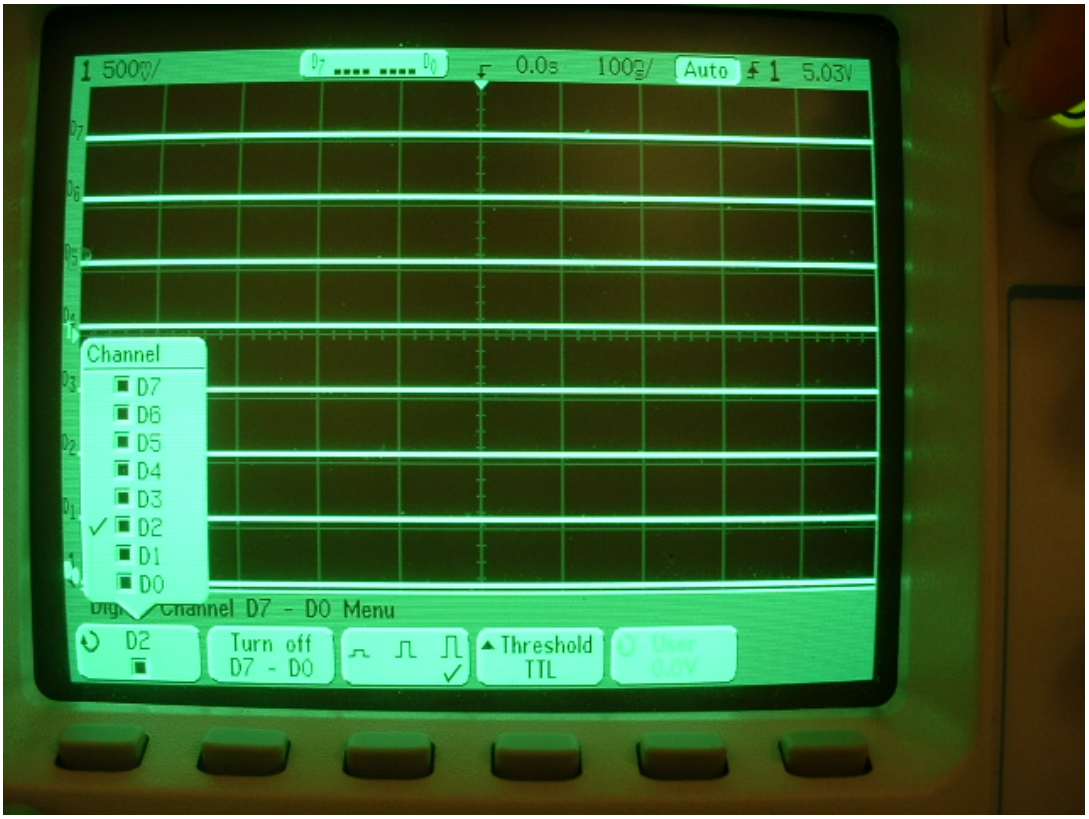
(b)

Figure 9 Illustration of D0-D7 and D8-D15 buttons. (a) button locations (b) illustration of menu

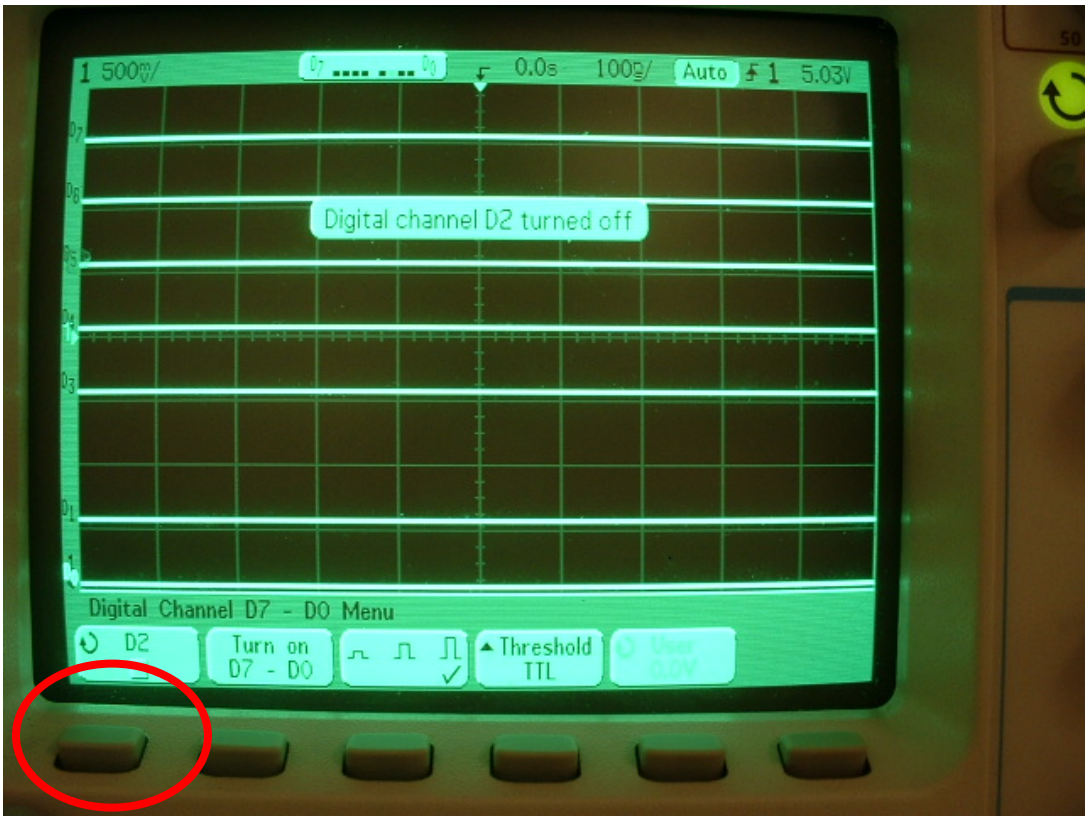
You can also turn off individual signals by turning the entry knob displayed in Figure 9a. For example, Figure 10 illustrates the steps taken to turn off signal D2.



(a) Selecting D0 with the entry knob.



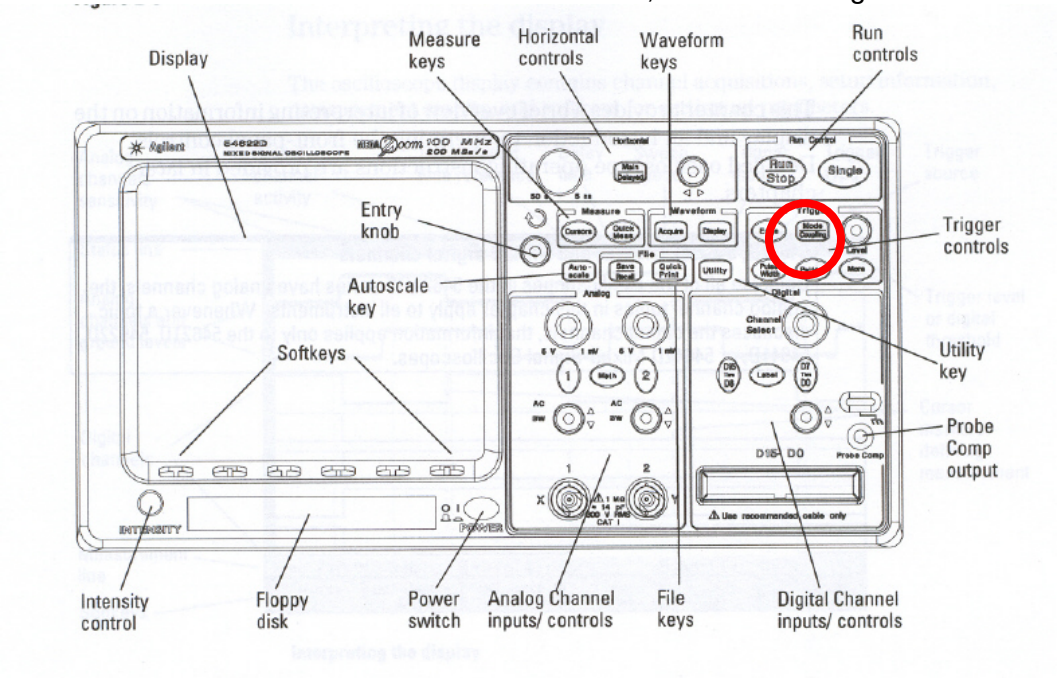
(b) Selecting D2 using the entry knob.



(c) Turning off signal D2 by pressing the highlighted button.

Figure 10 Illustration of turning off a signal on the Agilent model. (a) Selecting D0. (b) Selecting D2 with the entry knob. (c) Turning off D2.

If your signals do not show up, you may need to set your trigger mode using the mode coupling button shown in Figure 11a. After you press mode coupling, a menu will pop up on the screen. Simply press the button in front of the "Mode" until "Mode Auto" is selected, as shown in Figure 11b.



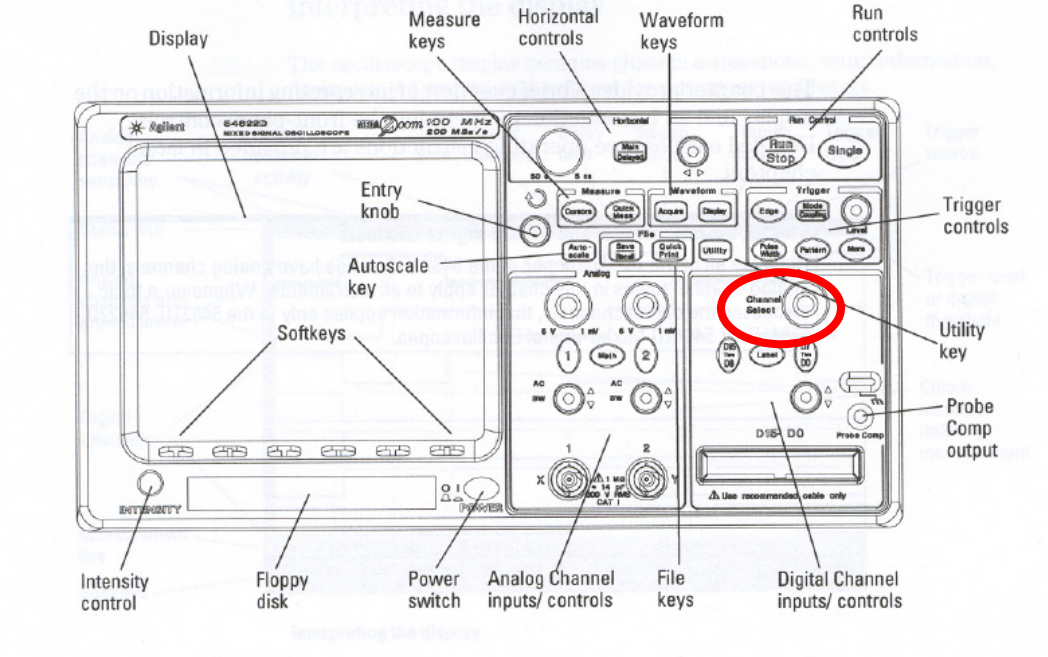
(a)

(b)

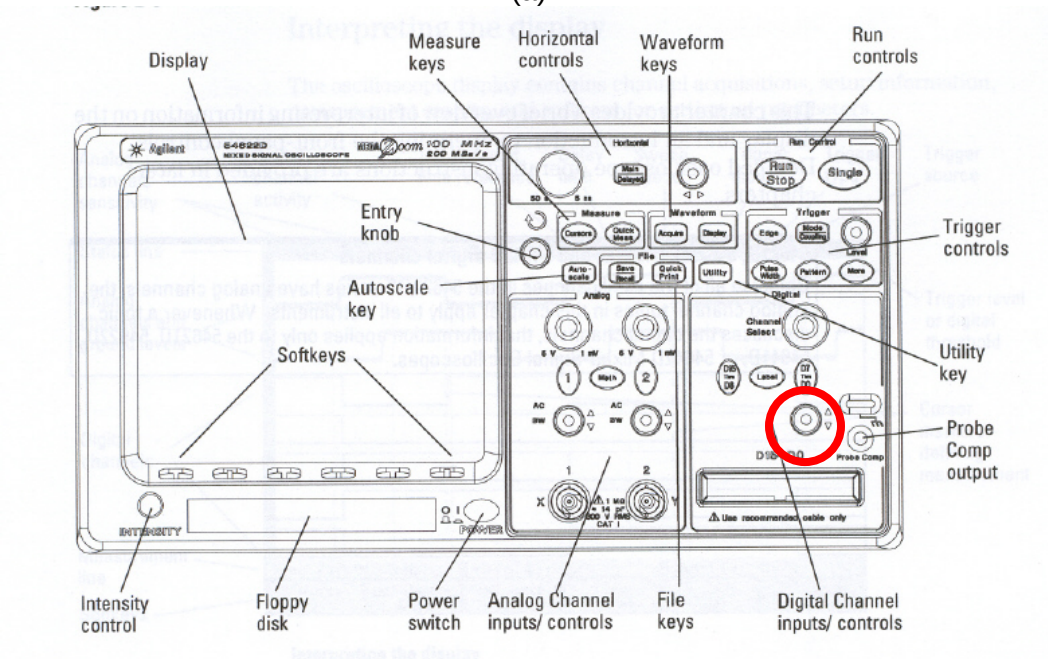
Figure 11 Setting your trigger mode to "Mode Auto".

Optional Features:

The channel select knob highlighted in Figure 12a allows you to select a specific data line or “channel”. Once selected you can use the knob highlighted in Figure 12b to move it around and overlap with other channels. This allows you to condense your picture if you only want to view a few channels at a time.



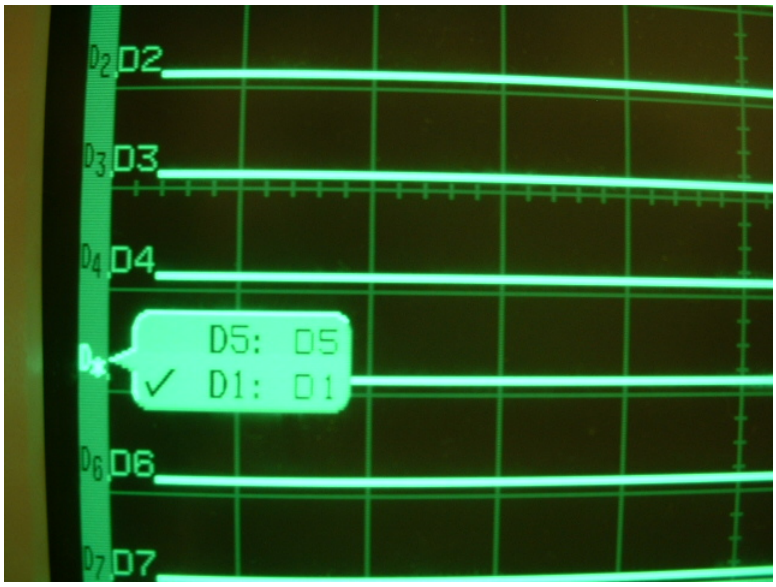
(a)



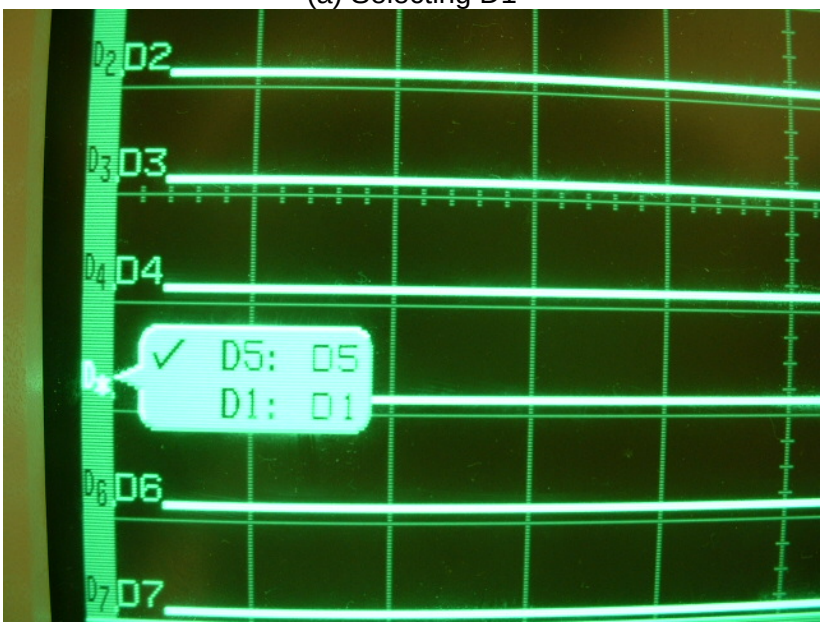
(b)

Figure 12 Optional Channel Select and channel move features. (a) Channel select knob (b) Channel move knob

To select a channel on a shared line, you will have to scroll through them using the channel select knob. For example, Figure 13 illustrates a channel line shared by D1 and D5. You can select between D1 and D5 using the Channel Select knob.



(a) Selecting D1



(b) Selecting D5

Figure 13 Illustration of selecting channels on a shared line.

Output your signal to an output pin

In order to view your signals using the logic scope, you will need to output the signal to one of the output pins on the JP1 port shown in Figure 14. Note that pin 1 starts at the top right corner, and the pin number increment going from right to left followed by top to bottom as shown in Figure 15. We will illustrate this process through an example, both for the schematic entry case using a BDF file, and a Verilog module case.

The steps for the Hewlett Packard and Agilent model are the same, so follow the following sections for both models.

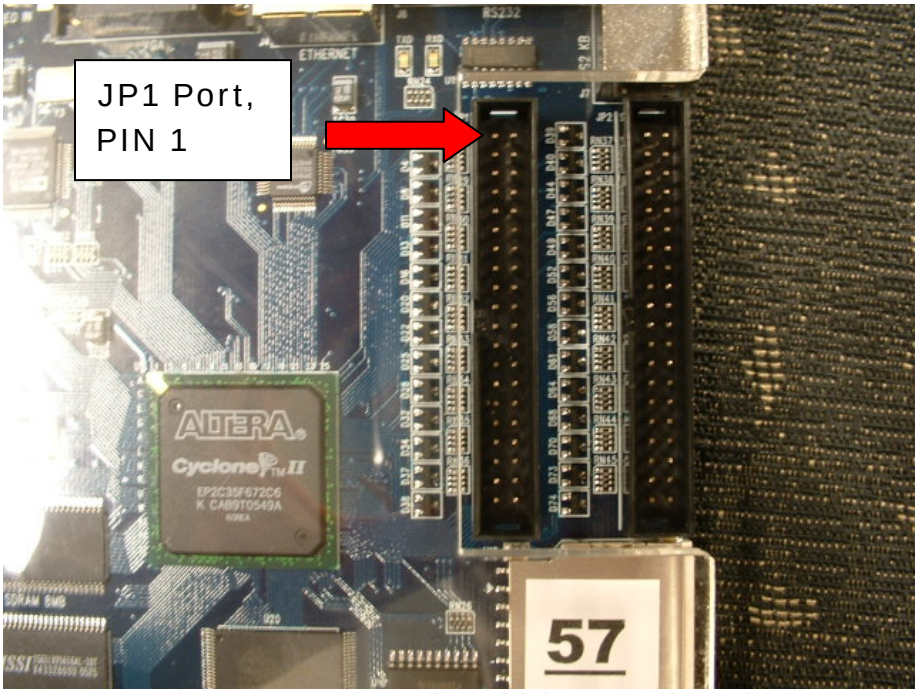


Figure 14 JP1 port (left side) on DE2 board.

Figure 15 Pin numbers for the JP1 port.

Schematic BDF

Consider the design shown in Figure 16. This is a basic design consisting of 6 inputs (clock, data_ready, datain[3..0]), 8 outputs (data_request, a-g), and 5 internal signals (enable, reged[3..0]).

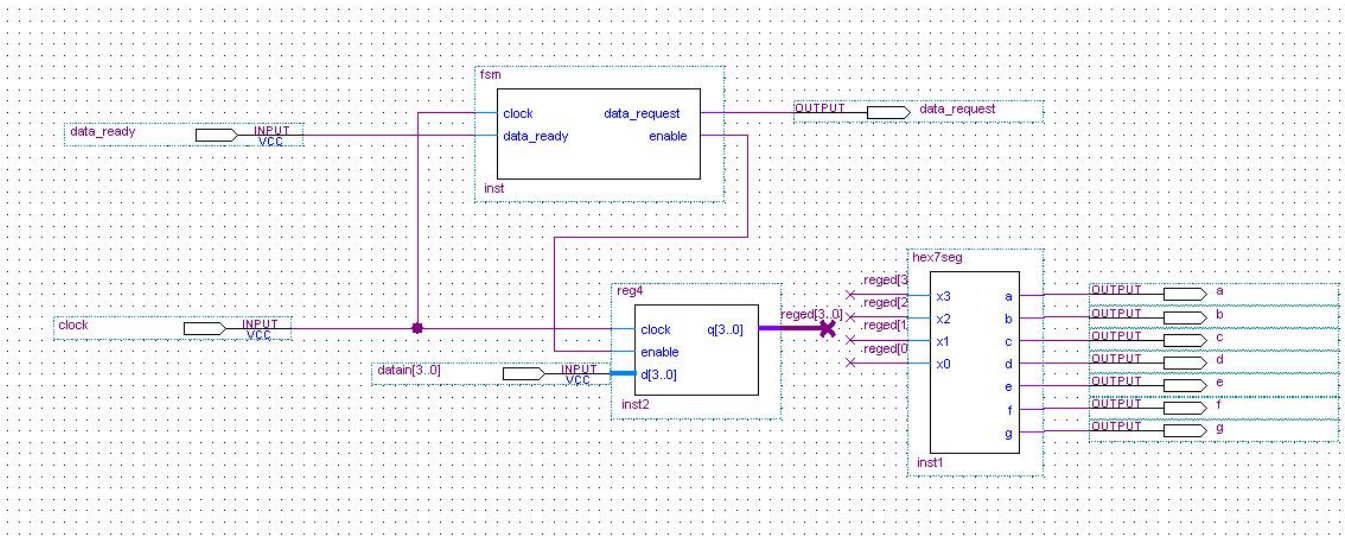


Figure 16 Example design in schematic format (BDF).

To view the clock, we will need to create an output pin, and connect the clock signal to the output pin as shown in Figure 17. Here, we created an output pin called “clock_view” and connected it to the input “clock”.

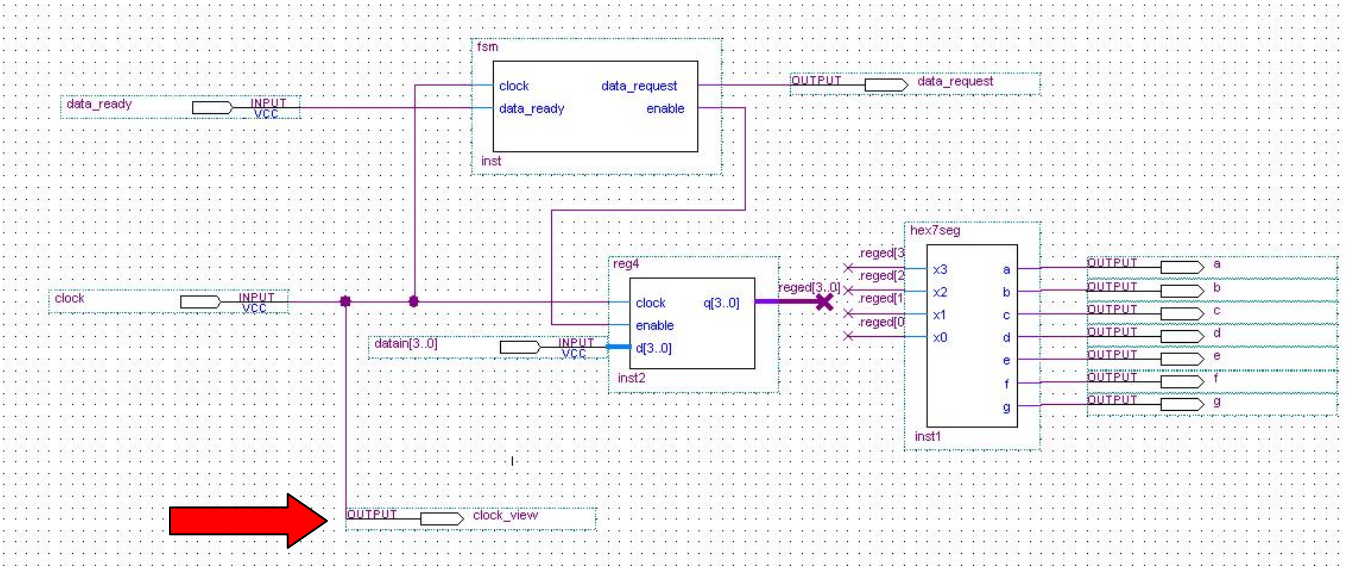


Figure 17. Output the clock input signal.

Following this, we will assign the output pin to one of the pins on the JP1 port through the pin assignment editor. For example, if we want to assign “clock_view” to PIN 1 of the JP1 port, we will assign it PIN_D25. The ***Appendix*** lists all the pin names for the JP1 port.

If you want to view internal signals and other inputs, you can simply create more output pins as illustrated in Figure 18.

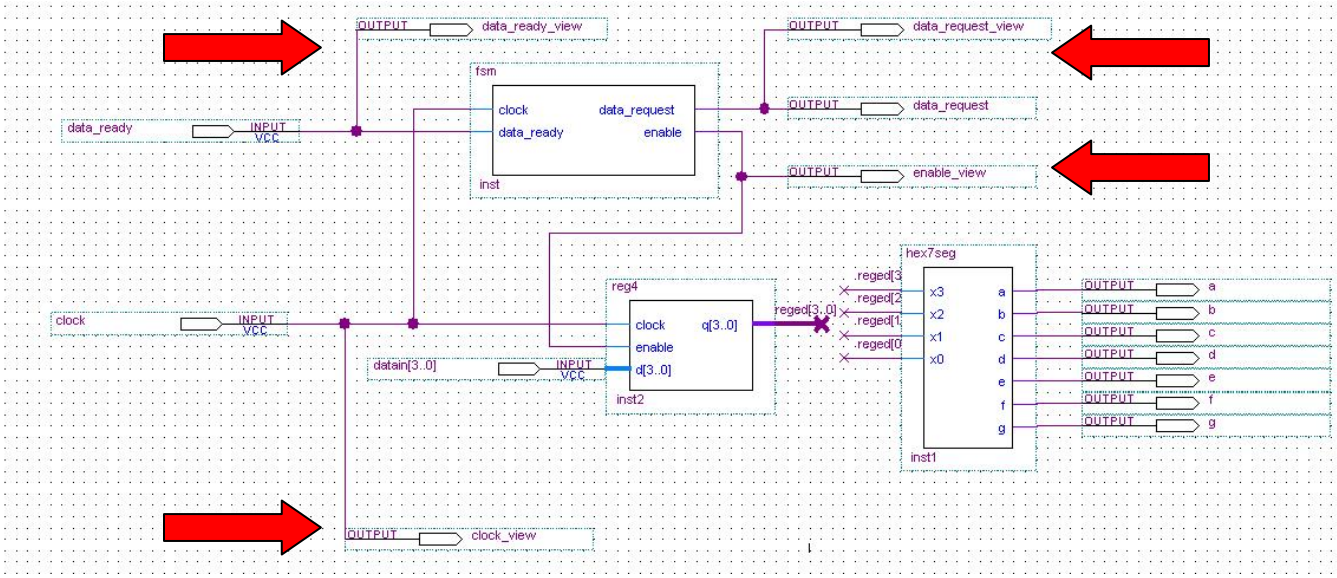


Figure 18 Illustration of viewing several signals on the schematic.

Verilog

To output the pins in a Verilog design, you will need to create an output wire in your port list, then assign the signal of interest to the new output wire. For example, consider the module shown in Figure 19. To view the clock, you will need to create a new output wire called "**`clock_view`**" and assign the clock input signal to "**`clock_view`**" as highlighted in Figure 20.

```
module top(clock, data_ready, data_request, a, b, c, d, e, f, g, data)

  input clock;
  input data_ready;
  output data_request;
  output a, b, c, d, e, f, g;
  input [3:0] data;

  wire internal_enable;
  wire [3:0] internal_regout;

  fsm inst( .data_ready(data_ready),
            .clock(clock),
            .enable(internal_enable),
            .data_request(data_request) );


  reg4 inst2( .clock(clock),
              .enable(internal_enable),
              .d(data),
              .q(internal_regout) );

  hex7seg inst1( .x3(internal_regout[3]),
                 .x2(internal_regout[2]),
                 .x1(internal_regout[1]),
                 .x0(internal_regout[0]),
                 .a(a), .b(b), .c(c), .d(d), .e(e), .f(f), .g(g) );

endmodule
```

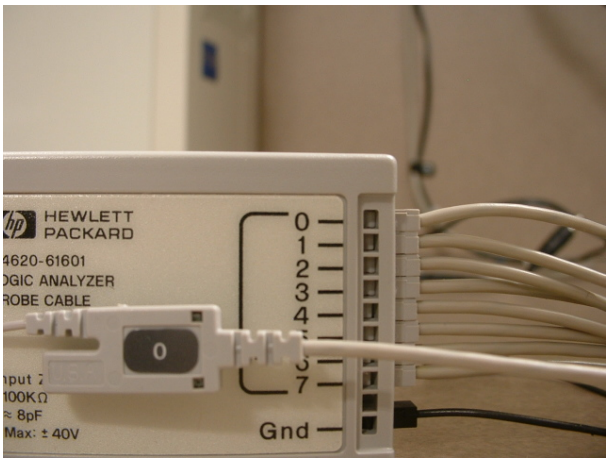
Figure 19. Verilog module, equivalent to the schematic shown in Figure 16.

```
module top(clock, data_ready, data_request, a, b, c, d, e, f, g, data, clock_view)
  input clock;
  input data_ready;
  output data_request;
  output clock_view;
  output a, b, c, d, e, f, g;
  input [3:0] data;

  wire internal_enable;
  wire [3:0] internal_regout;

 assign clock_view = clock;

  fsm inst( .data_ready(data_ready),
            .clock(clock),
            .enable(internal_enable),
            .data_request(data_request) );

  reg4 inst2( .clock(clock),
              .enable(internal_enable),
              .d(data),
              .q(internal_regout) );

  hex7seg inst1( .x3(internal_regout[3]),
                 .x2(internal_regout[2]),
                 .x1(internal_regout[1]),
                 .x0(internal_regout[0]),
                 .a(a), .b(b), .c(c), .d(d), .e(e), .f(f), .g(g) );

endmodule
```

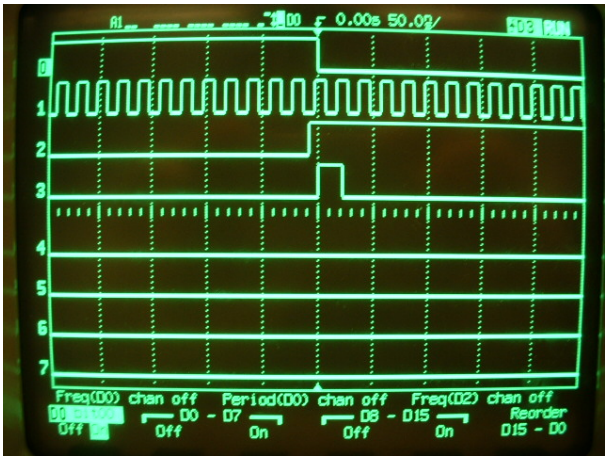
Figure 20. Verilog module to view "clock" with "clock_view", equivalent to the schematic shown in Figure 17.

Connect your probes

The last thing you will need to do is physically attach your probes to the appropriate output pins. Each probe is identified by a number labeled at the end of the probe, as illustrated in Figure 21a. This corresponds to a signal as shown in Figure 21b.



(a) Probe label for probe 0.



(b) Highlighting signal 0.

Figure 21 Illustration of probe labels (a) and their correspondence to the screen (b).

After you identified which probes you want to use, you need to attach the probe heads to your output pins as illustrated in Figure 22.

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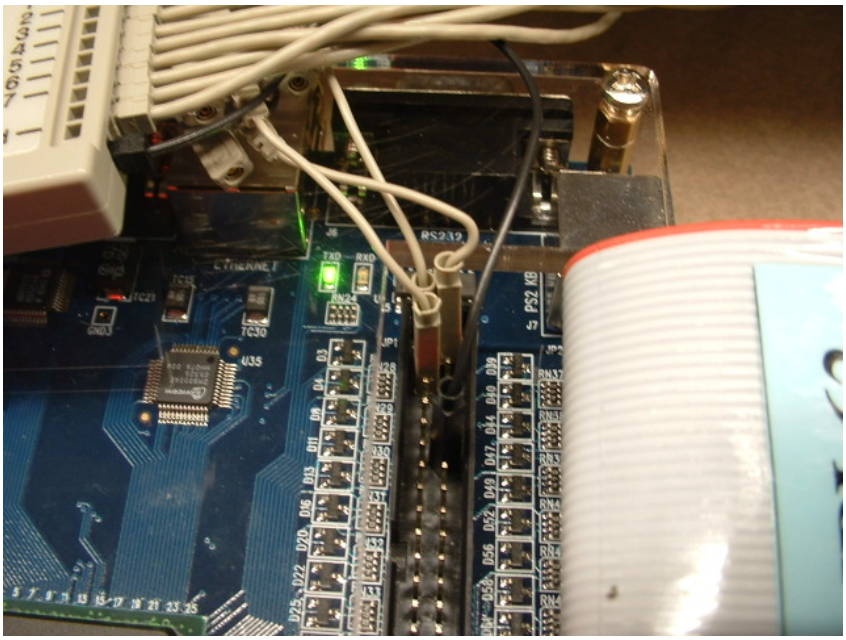
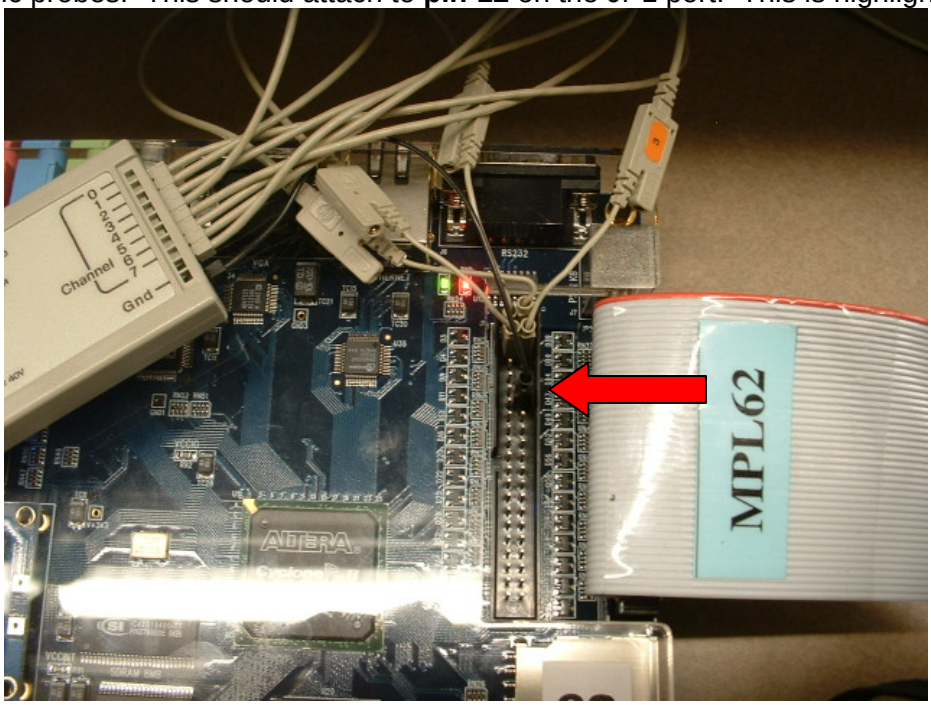


Figure 22. Connecting your logic probes to the JP1 port.

You will need to attach your ground to the ground pin on the JP1 port. The ground wire is the black wire on your logic probes. This should attach to **pin 12** on the JP1 port. This is highlighted in Figure 23.



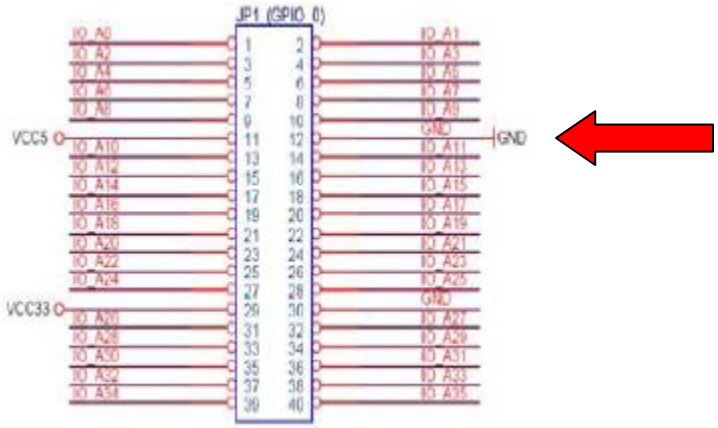


Figure 23 Illustration of logic probe attachment, with ground highlighted.

Setting up a Trigger Event

Often it is necessary to capture a specific pattern on the logic scope and freeze that moment in time on the logic scope. This is an important during debugging to check the behaviour of your signals during specific instances in time. Freezing the display at specific events is possible using your logic scope through trigger events.

To setup a trigger event you will need to:

- Specify the correct mode for the logic scope.
- Set your trigger source.
- Specify the input pattern the trigger will look for.

Please refer to your model to setup the trigger event.

Hewlett Packard

Setup Trigger Mode

To get into trigger mode, press the “mode coupling” button in the trigger menu as shown in Figure 24.

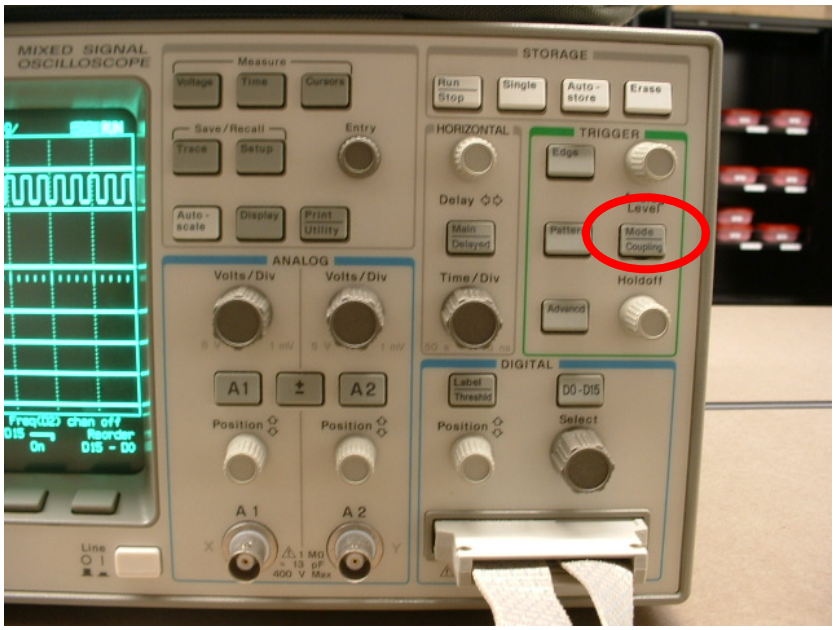


Figure 24 Hewlett Packard Mode Coupling Button.

This will pop up a display on the screen as shown in Figure 25.

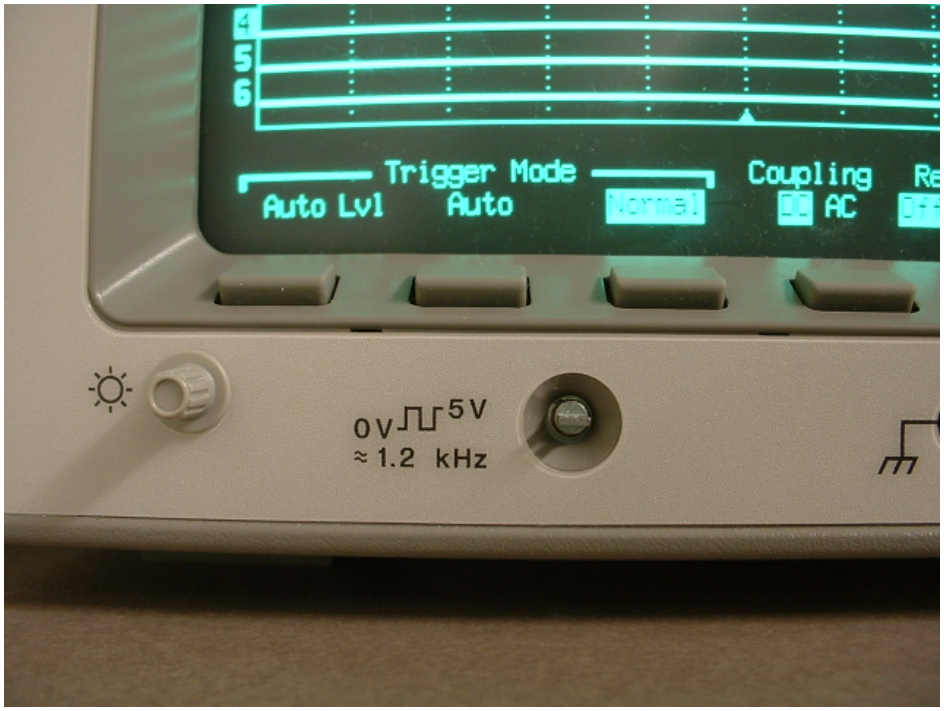


Figure 25 Mode coupling menu on Hewlett Packard.

Once the mode coupling menu is displayed, select the “Normal” option.

Setup Trigger Source

The trigger source is the signal that will be monitored for the trigger event. To setup the trigger source, press the edge button highlighted in Figure 26. This will display a trigger source menu as shown in Figure 27.

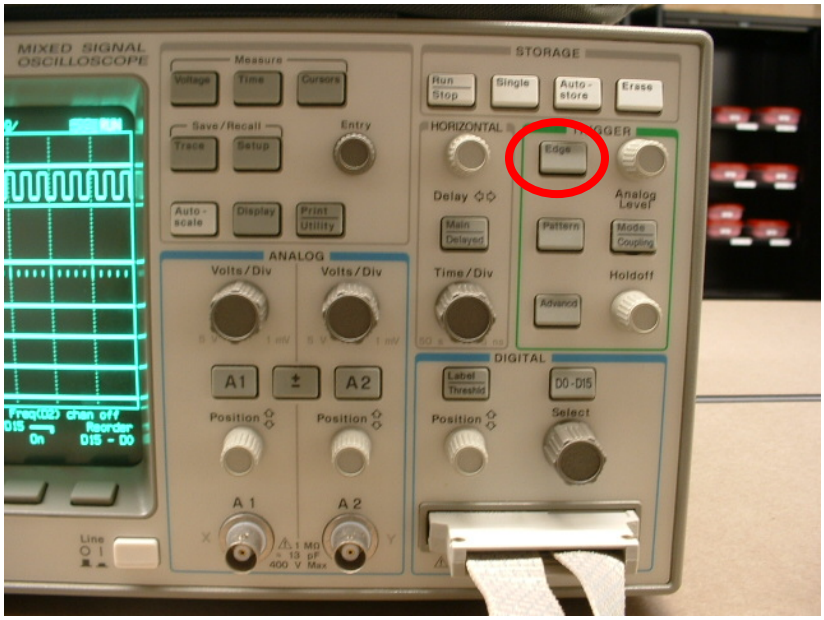
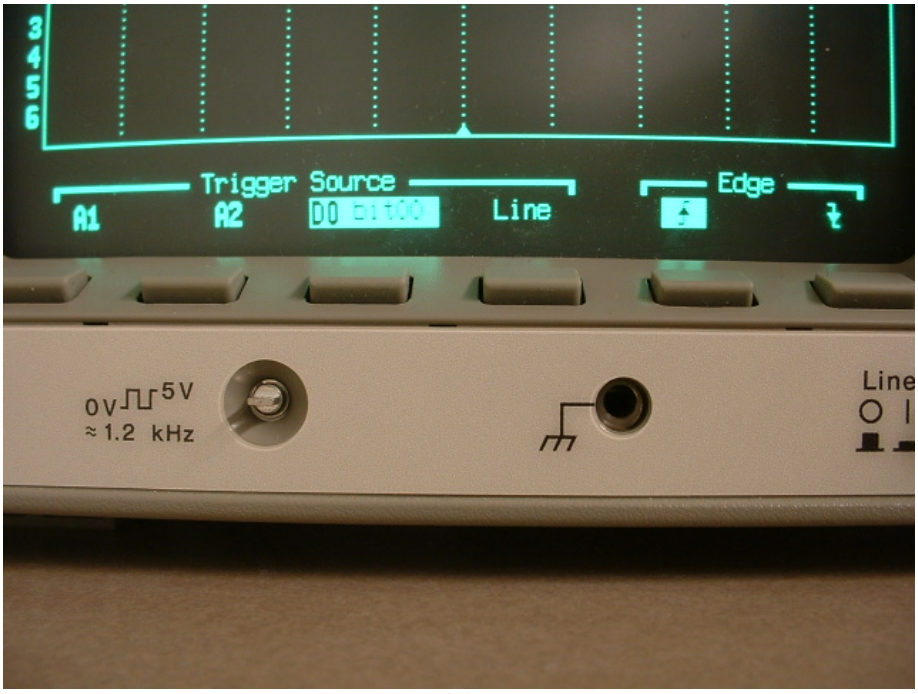
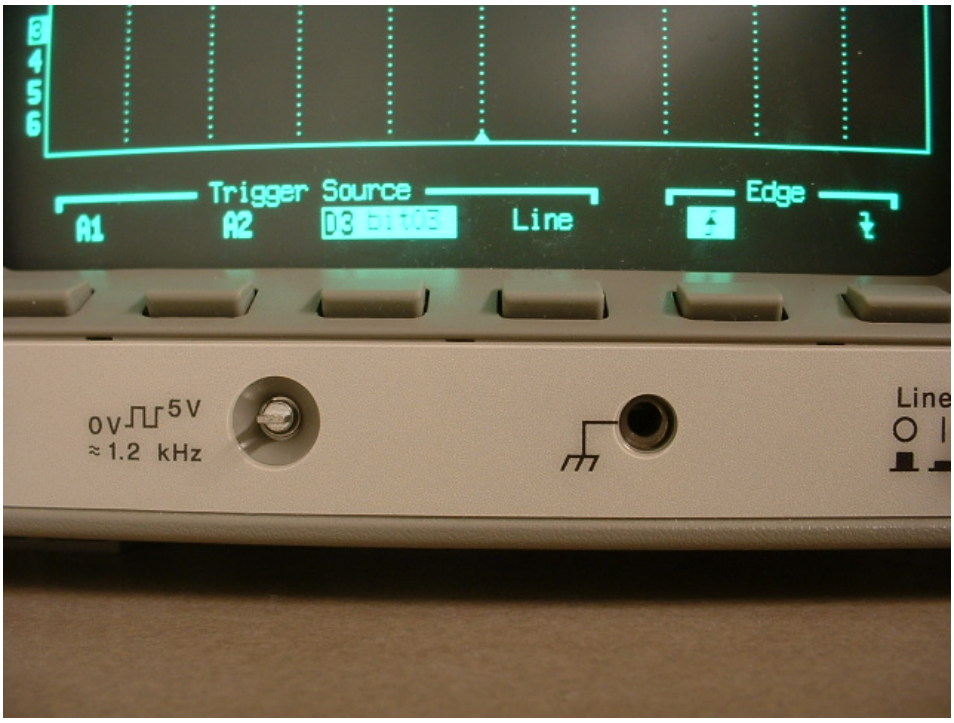


Figure 26 The location of the edge button on the Hewlett Packard model.



(a)



(b)

Figure 27 Illustration of selecting your source on the trigger menu. (a) D0 trigger source. (b) D3 trigger source.

In the trigger menu, since we are dealing with the digital logic probes, select the DXX as the source where XX will match the number on your digital probe. Scroll through the DXX values to pick the source you would like to trigger on. For example, in Figure 27a the current trigger source is D0. If you would like to trigger on probe D3, press the button in front of D0 until D3 appears as shown in Figure 27b.

Setup Trigger Pattern

The trigger pattern is the pattern that will be monitored on the trigger source to cause the logic scope to freeze its display. For our purposes, we will only be triggering on the rising or falling edge of a signal. To select what edge you would like to trigger on, press the “edge” button to display the trigger menu and select the rising or falling edge symbol on the edge menu. For example, in Figure 28, the rising edge is selected.

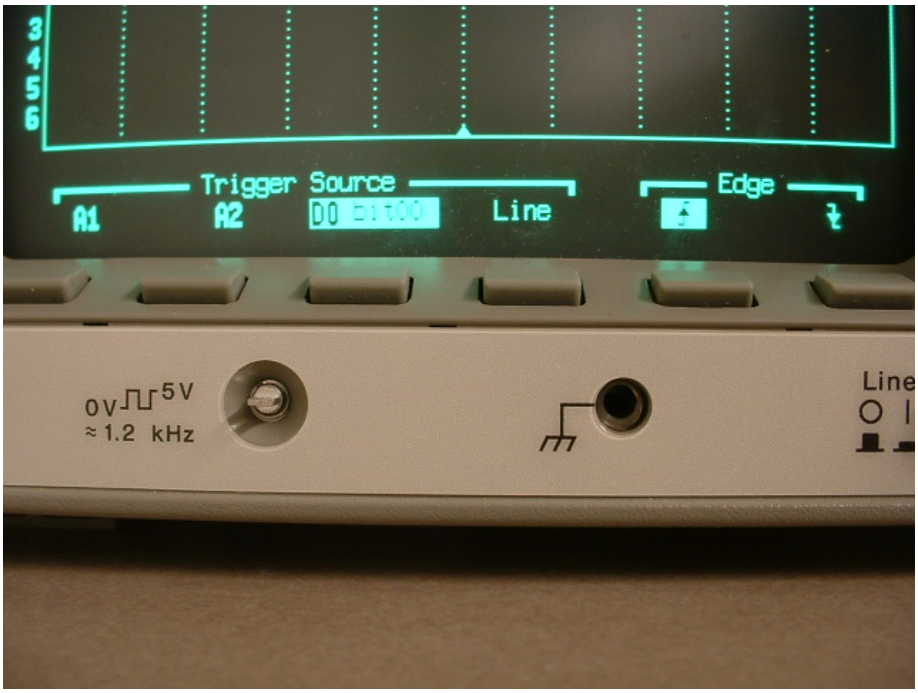
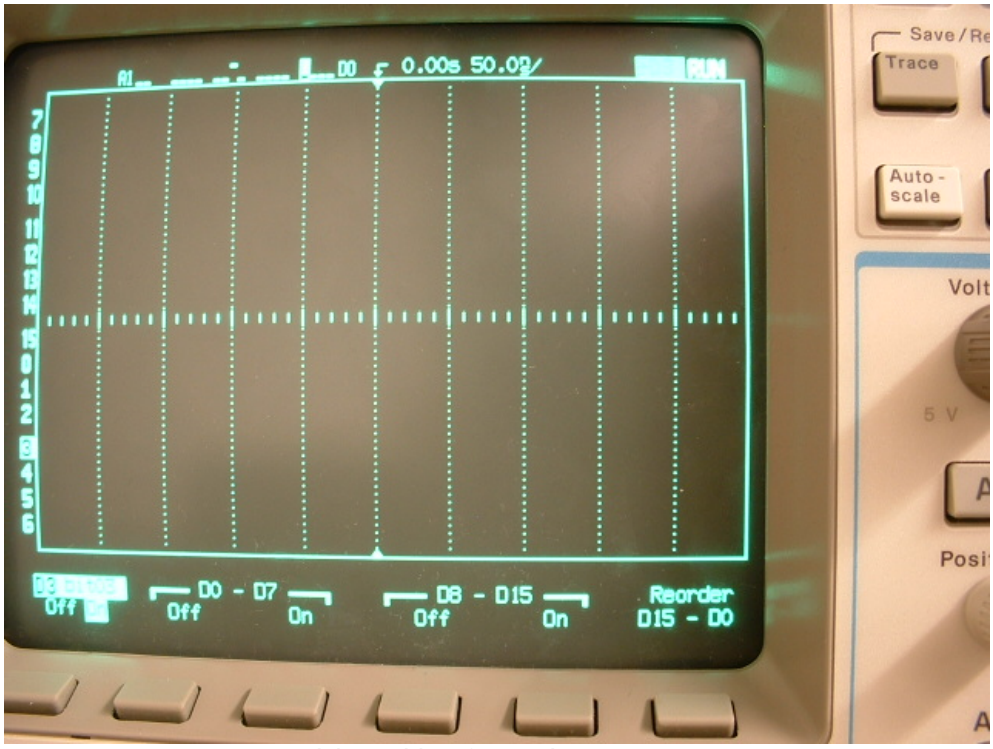
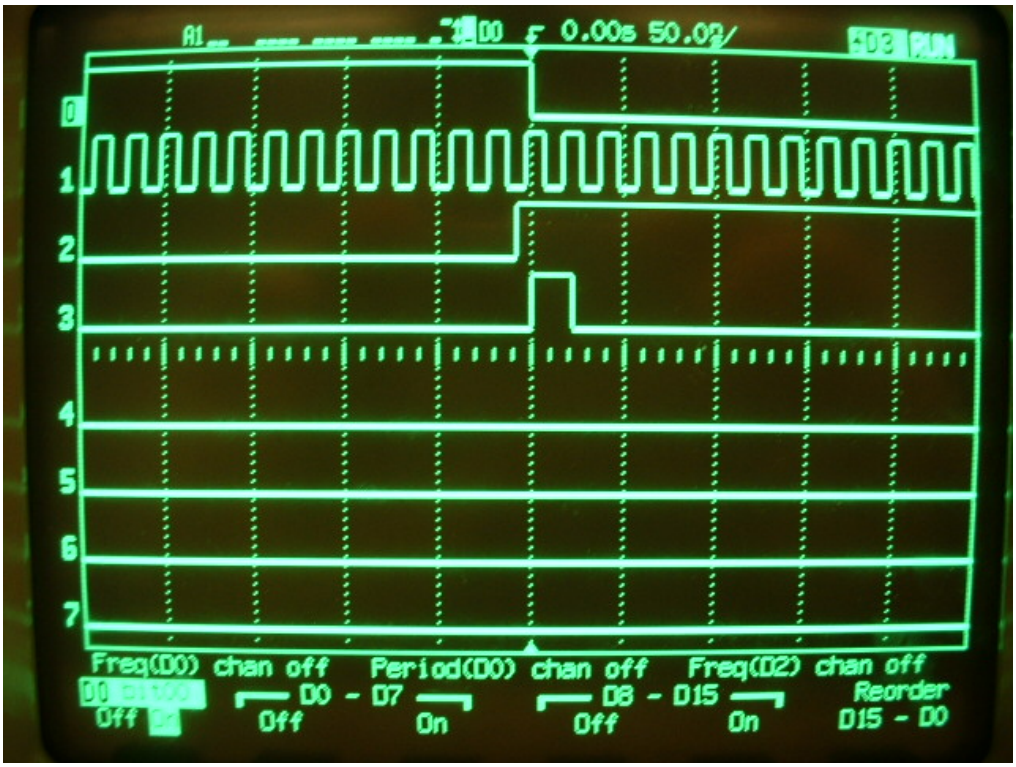


Figure 28 Illustration of rising edge trigger pattern.

After all the parameters have been set in the logic scope, the logic scope will not display anything until the trigger event occurs. Once it occurs, it will display its signals at the moment the event occurred. For example, in Figure 29 the trigger source was on D2 on its rising edge.



(a) Waiting for and event on D2.



(b) Rising edge event on D2 occurred and screen is captured.

Figure 29 Illustration of trigger events. (a) Waiting for a rising edge to occur on probe D2. (b) Rising edge detected which freezes all signal activity on the screen during the event.

Agilent

Setup Trigger Mode

Allow for a trigger event, you must set the trigger mode to “Normal”. First press the “mode coupling” button as highlighted in Figure 30.

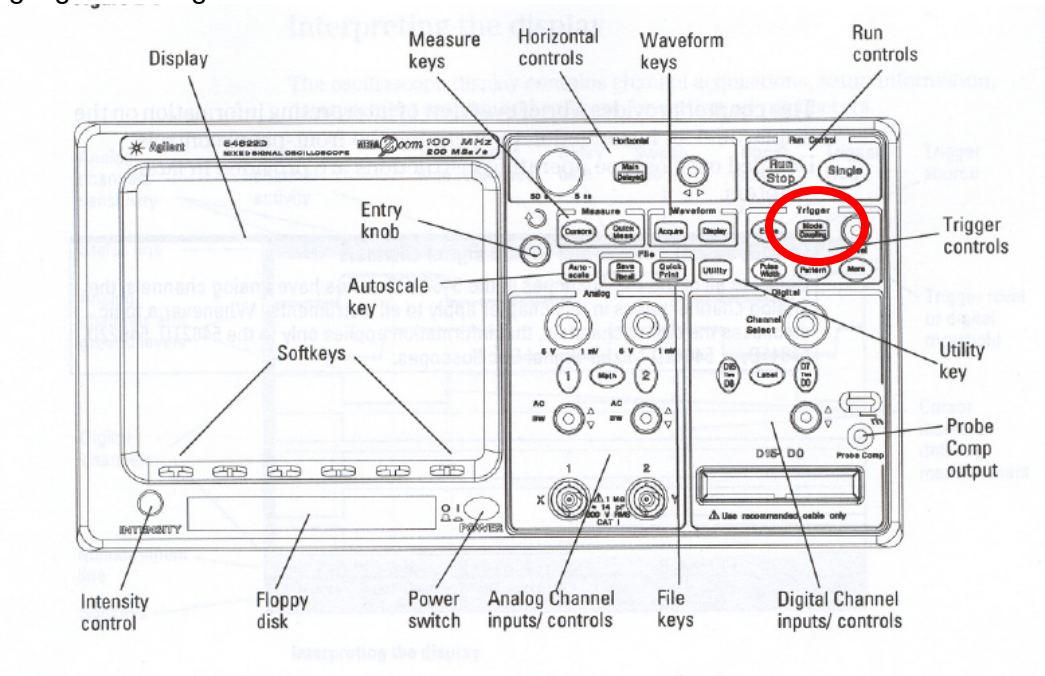


Figure 30 Location of "Mode Coupling" button

This will pop a trigger menu on the screen. Press the button in front of Mode until “Mode Normal” is shown as shown in Figure 31.

Figure 31 Setting the Agilent scope to "Normal" mode

Setup Trigger Source

The trigger source is the signal that will be monitored for the trigger event. To setup the trigger source, press the edge button. This will display a trigger source menu as shown in Figure 33 (D7 is shown as the trigger source). To select your trigger source, use the entry knob shown in Figure 32 to scroll through the sources.

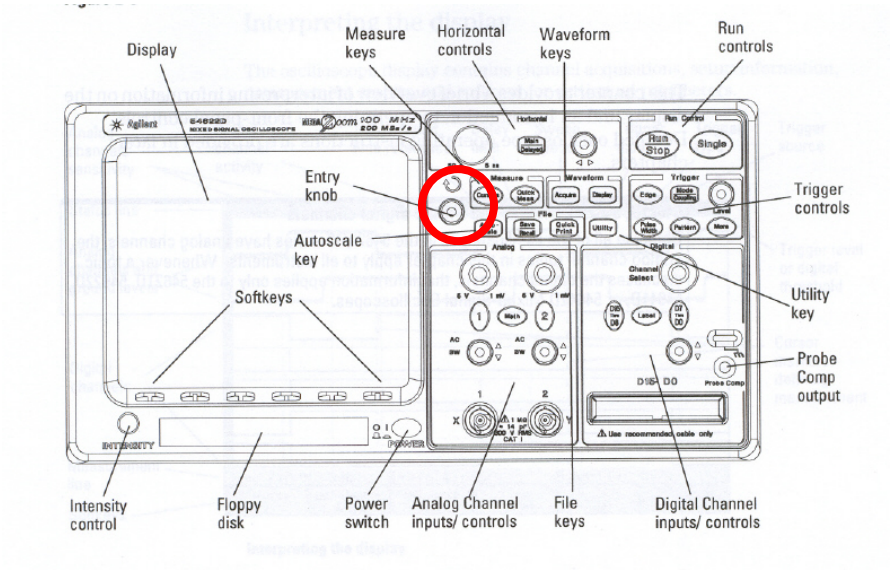


Figure 32 Highlight of the entry knob in the Agilent scope.

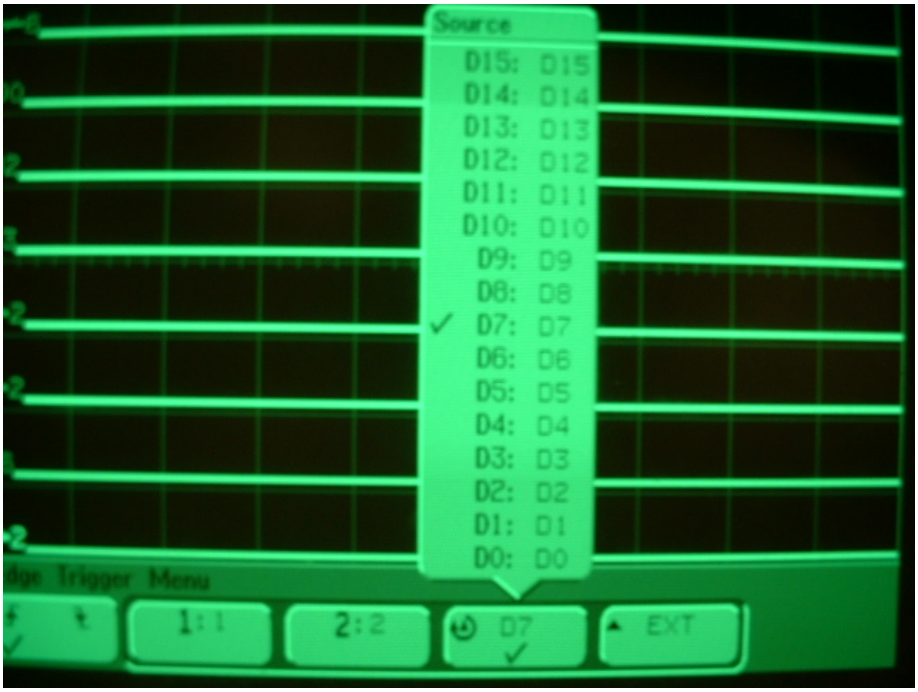


Figure 33 Selecting your trigger source on the Agilent scope in the trigger menu.

Setup Trigger Pattern

The trigger pattern is the pattern that will be monitored on the trigger source to cause the logic scope to freeze its display. For our purposes, we will only be triggering on the rising or falling edge of a signal. To select what edge you would like to trigger on, press the “edge” button to display the trigger menu

and select the rising or falling edge symbol on the edge menu. For example, in Figure 34 the falling edge is selected.

Figure 34 Falling edge selected as trigger pattern.

After all the parameters have been set in the logic scope, the logic scope will freeze its display when the trigger event occurs. Once it occurs, it will display its signals at the moment the event occurred. For example, in Figure 35 the trigger source was on D2 on its rising edge.

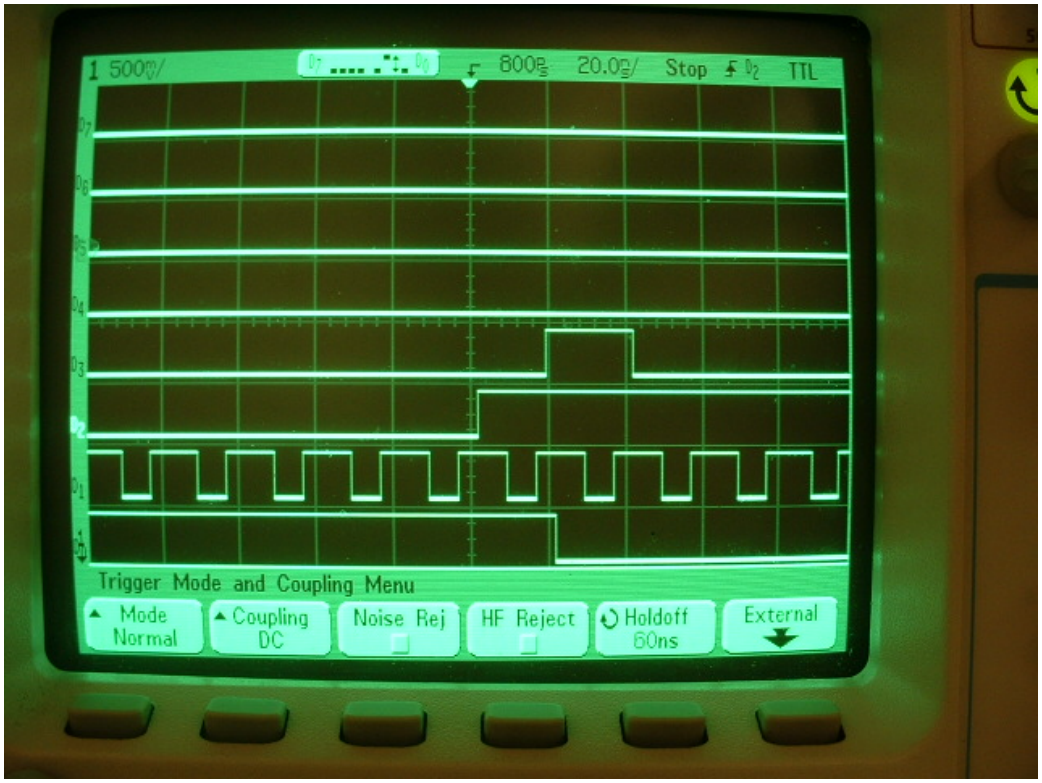


Figure 35 Trigger example with D2 as the trigger source with a rising edge pattern.

Appendix

Pin Assignment File

The location of the pin assignment file can be found here.
http://www.altera.com/education/univ/materials/boards/DE2_pin_assignments.csv

If that link is dead, go to the Altera website at www.altera.com and search for “DE2”.

Node that in the pin assignment file (DE2_pin_assignments.csv), the JP1 port are referenced as GPIO_0 and the JP2 port is referenced as GPIO_1 (i.e. JP1 = GPIO_0 and JP2 = GPIO_1). Furthermore, the CSV file starts at index 0, instead of index 1 (i.e. JP1 PIN 1 = GPIO_0[0], JP1 PIN 2 = GPIO_0[1], … , JP1 PIN ‘N’ = GPIO_0[N-1]).

JP1 and JP2 Pins to Quartus II Pin Names

PORT JP1, PIN Number	Quartus II Pin Assignment
1	PIN_D25
2	PIN_J22
3	PIN_E26
4	PIN_E25
5	PIN_F24
6	PIN_F23
7	PIN_J21
8	PIN_J20
9	PIN_F25
10	PIN_F26
11	PIN_N18
12	PIN_P18
13	PIN_G23
14	PIN_G24
15	PIN_K22
16	PIN_G25
17	PIN_H23
18	PIN_H24
19	PIN_J23
20	PIN_J24
21	PIN_H25
22	PIN_H26
23	PIN_H19
24	PIN_K18
25	PIN_K19
26	PIN_K21
27	PIN_K23
28	PIN_K24
29	PIN_L21
30	PIN_L20

31	PIN_J25
32	PIN_J26
33	PIN_L23
34	PIN_L24
35	PIN_L25
36	PIN_L19

PORT JP2, PIN Number	Quartus II Pin Assignment
1	PIN_K25
2	PIN_K26
3	PIN_M22
4	PIN_M23
5	PIN_M19
6	PIN_M20
7	PIN_N20
8	PIN_M21
9	PIN_M24
10	PIN_M25
11	PIN_N24
12	PIN_P24
13	PIN_R25
14	PIN_R24
15	PIN_R20
16	PIN_T22
17	PIN_T23
18	PIN_T24
19	PIN_T25
20	PIN_T18
21	PIN_T21
22	PIN_T20
23	PIN_U26
24	PIN_U25
25	PIN_U23
26	PIN_U24
27	PIN_R19
28	PIN_T19
29	PIN_U20
30	PIN_U21
31	PIN_V26
32	PIN_V25
33	PIN_V24
34	PIN_V23
35	PIN_W25
36	PIN_W23

References

References of various logic scopes:
http://www.eecg.utoronto.ca/~aulich/analyzer.html

Hewlett Packard Reference:
http://www.eecg.utoronto.ca/~aulich/logicmix.html

Agilent Reference:
http://www.eecg.utoronto.ca/~aulich/logicmix2.html