University of Toronto
Faculty of Applied Science and Engineering
Edward S. Rogers Sr. Department of Electrical and Computer Engineering

Final Examination
ECE 241F - Digital Systems

Examiners: S. Brown, J. Rose, K. Truong and B. Wang
December 12, 2005

Duration: 2.5 Hours

SOLUTIONS

- Exam Type D, these specific aids allowed:
  i. Original Versions (no photocopies) of the course text, **Fundamentals of Digital Logic with Verilog Design,** by Brown & Vranesic, ISBN 0-07-282315-1.
  ii. One 8.5 x 11" two-sided aid sheet.

- The amount of marks available for each question is given in square brackets [].
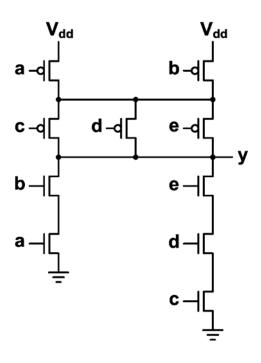

LAST NAME: _____

FIRST NAME: _____

STUDENT NUMBER: _____

Lecture Section: Section 01 (Rose)   [   ]
                    Section 02 (Wang)   [   ]
                    Section 03 (Brown)   [   ]
                    Section 04 (Truong) [   ]

Question	1	2	3	4	5	6	7	8	9	Total
Maximum Mark	6	5	4	8	10	8	12	8	9	70
Mark Obtained										

[6] Q1.   This question concerns transistor-level circuit design of digital logic gates.

(a) Write the logic function for **y**, the output of the circuit below, in terms of **a**, **b**, **c**, **d** and **e**.
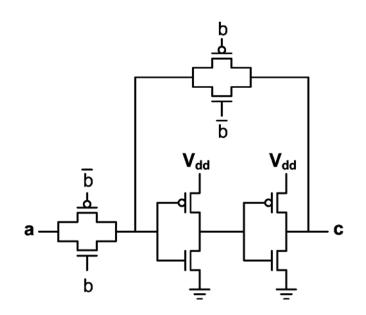

ANSWER:

Solution:
 y=(ab+cde)'

Marking scheme:
3 marks for correct in any form.
1 mark for some basically sensible attempt
0 marks for blank

Q1, continued .

(b)   Describe the operation of the circuit below in the simplest way.

   ANSWER:

   Solution:
   It is a D latch – b is the clock and a is the D input.
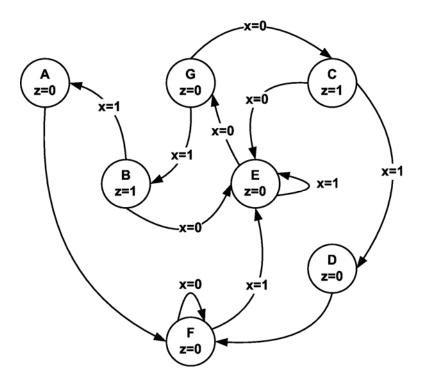
   Marking scheme:

   3 marks for identifying that it is a D latch.
   2 for identifying D latch without saying a = D input and b is the clock.
   1 mark for a correct description of the operation of the circuit without saying it is a D latch.
   0 marks for incorrect description

[5] Q2.   Finite State Machine State minimization. Consider the following state diagram for a state machine that has **x** as its input and **z** as its output:

(a) Give state transition table corresponding to this state diagram.

Present state	Next state		Output (z)
	x=0	x=1	
A	C	F	0
B	E	A	1
C	E	D	1
D	F	E	0
E	G	E	0
F	F	E	0
G	E	B	0

Solution:

Present state	Next state		Output (z)
	x=0	**x=1**	
A	F	F	0
B	E	A	1
C	E	D	1
D	F	F	0
E	G	E	0
F	F	E	0
G	C	B	0

Marking scheme for (2a):
-0.5 for each incorrect state to the minimum of 0.

Last Name_____   Student Number _____

Q2, continued.

(b) Determine the minimum number of states in this state machine.

(i) The minimum number of states = _____

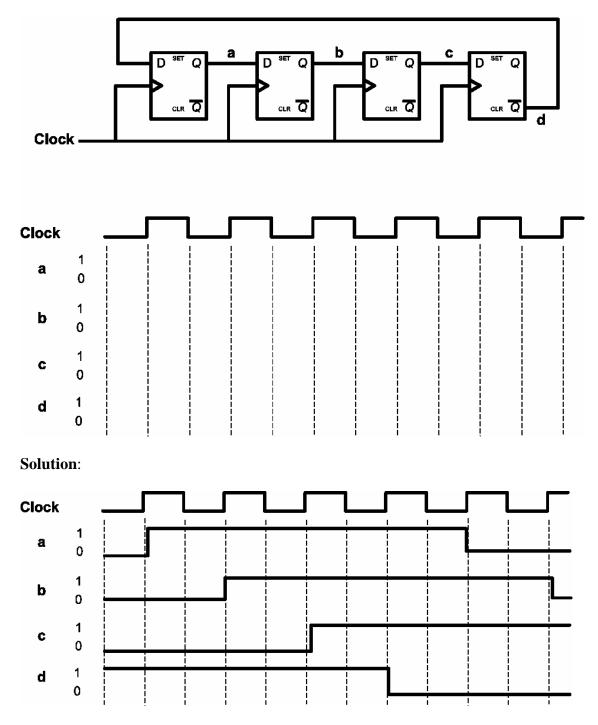(ii) The states that are equivalent in the original state machine are:

Solution:
(ABCDEFG)
(ADEFG)(BC)
(ADEF)(G)(BC)
(ADF)(E)(G)(BC)
(AD)(F)(E)(G)(BC)

(i)   Minimum Number of States = 5;
(ii)   States A and D are equivalent, as are B and C.
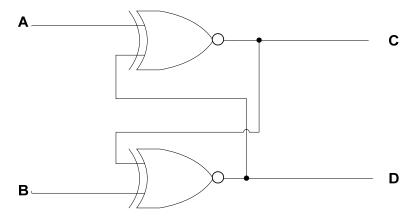
Marking scheme:
3 marks for determining that AD and BC are equivalent states.
1-2 marks for varying degrees of correctness.
0 marks for nonsense.

[4] Q3. Complete the timing diagram for the circuit below for the outputs **a**, **b**, **c** and **d**. Assume that all the D-flip flops are initially cleared to 0. Assume that all delays are zero (i.e. functional simulation).
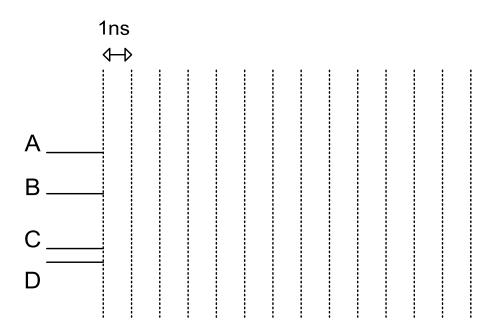

Solution:

Marking scheme:

1 mark for each correct output.

[8] Q4.   Consider the following cross-coupled **exclusive NOR** circuit with inputs A and B and outputs C and D:

Describe the behavior of the circuit when A = 1 and B = 0 using words *and* by completing the timing diagram below. For the timing diagram assume that the propagation delay of the Exclusive OR gates are 1 ns, and that the initial values for the circuit nodes are: A=0, B=0, C=0 and D=1. Your answer <u>must</u> consist of a very short written description of the behavior of the circuit and the timing diagram.
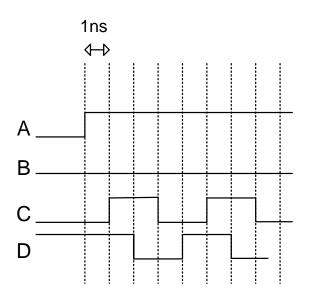
Timing Diagram:

Written Description of Behavior:

Solution: C and D oscillate, with a period of 4 ns.
[8 marks – **2** for oscillation, **2** for period, **4** for correct timing diagram below (-1 for each mistake)]
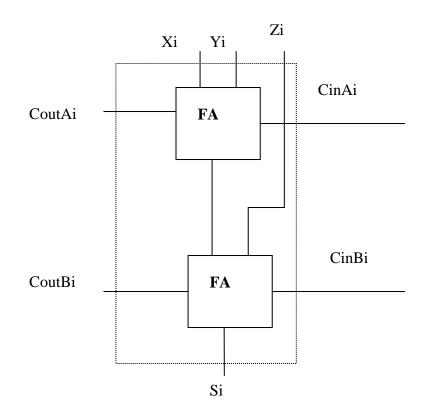
Timing Diagram

[10] Q5.   This question is about building a digital circuit that will add <u>three</u> 4-bit numbers, X, Y and Z. The individual bits of these three numbers will be represented as X_i, Y_i, and Z_i. To illustrate this clearly, the addition of three 4-bit numbers would be written on papers as follows:

			X_3	X_2	X_1	X_0
		$+$	Y_3	Y_2	Y_1	Y_0
		$+$	Z_3	Z_2	Z_1	Z_0
S_5	S_4	S_3	S_2	S_1	S_0

Recall the design of a Full Adder (FA) building block described in class (and on page 239 of the text) which is used as a building block to create an adder that adds <u>two</u> N-bit numbers. You will design the complete circuit in two steps, part (a) and (b) below.

(a)   Using <u>only</u> FA building blocks give the design of a new building block that performs the function needed to implement the box surrounding x_2, y_2, z_2, and s_2, (shown above). You will call this building block **TNFA** and use it in part (b) below. It computes the sum bit S_i, corresponding to the three inputs X_i, Y_i, and Z_i <u>and any other inputs and outputs that are necessary</u> in the context of the full adder.

Solution: (4 marks – 1 corresponding to the X_i,Y_i,Z_i and then 1 each of the CinAi, CinBi, CoutAi and CoutBi)
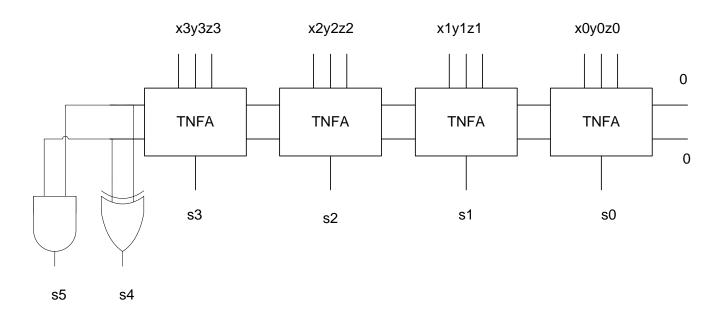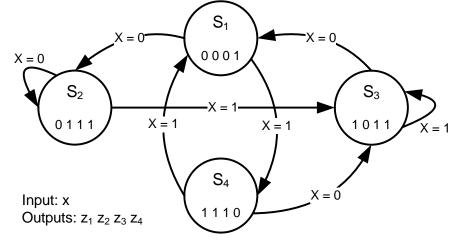
Q5, continued

      (b) Using the building block of part (a), the TNFA, and any other logic gates you deem necessary give the design of the three 4-bit number adder (which produces a 6-bit sum, $s_5 \ldots s_0$). Your answer should show <u>all</u> the inputs (i.e. all X_i, Y_i and Z_i, $i=0\ldots3$ and any carry inputs) and outputs necessary to make the complete adder function correctly.

Solution:

As below. 6 marks Total: 3 marks for the four TNFAs and 1 each for the s4 and s5 gates, 1 for carry ins on right hand side.

[8] Q6. For the finite state machine state diagram given below:

Input: x
Outputs: z_1 z_2 z_3 z_4

(a) Fill in the blanks in the following state assignment (encoding) table. Assume D flip-flops are used to implement this FSM. Q_1 and Q_0 are the outputs of the flip-flops, and therefore, represent the current state. D_1 and D_0 are the inputs of the flip-flops, and therefore, represent the next state.

Current State		Next State				Outputs			
		x = 0		x = 1					
Q_1	Q_0	D_1	D_0	D_1	D_0	z_1	z_2	z_3	z_4
(S_1) 0	0								
(S_2) 0	1								
(S_3) 1	0								
(S_4) 1	1								

Solution: 2 marks for correct answer - -1/2 for each error until max of 2

Current State		Next State				Outputs			
		x = 0		x = 1					
Q_1	Q_0	D_1	D_0	D_1	D_0	z_1	z_2	z_3	z_4
(S_1) 0	0	0	1	1	1	0	0	0	1
(S_2) 0	1	0	1	1	0	0	1	1	1
(S_3) 1	0	0	0	1	0	1	0	1	1
(S_4) 1	1	1	0	0	0	1	1	1	0

Q6, continued.

(b) Write the logic expressions in the simplest (optimized) sum-of-product (SOP) form for all the next-state variables (D_1 and D_0) and the outputs (z_1, z_2, z_3 and z_4).

Answer:

$D_1 =$

$D_0 =$
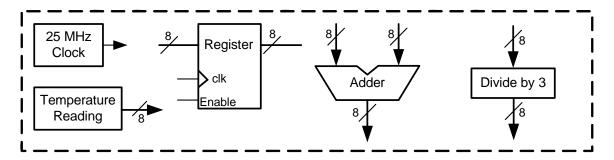
$z_1 =$

$z_2 =$

$z_3 =$

$z_4 =$

Working Space:

Solution:

$$D_1 = Q_1 Q_0 \bar{x} + \bar{Q}_0 x + Q_1 x$$

$$D_0 = \bar{Q}_1 \bar{x} + \bar{Q}_1 \bar{Q}_0$$

$$z_1 = Q_1$$

$$z_2 = Q_0$$

$$z_3 = Q_1 + Q_0$$

$$z_4 = \bar{Q}_1 + \bar{Q}_0$$

6 Total Marks:
1 mark for correct D_1
1 mark for correct D_0
1 mark for each of the correct z_1, z_2, z_3 and z_4,

[12] Q7. Your boss, Mr. Touf, asks you to design a "temperature averaging" system. The system captures a binary number corresponding to a temperature reading every hour. Two hours after the system is turned on, it will have captured three temperature readings. Then, it will calculate and display the first average temperature (T_{Avg}) of those three readings as a binary number. Subsequently, it will display the T_{Avg} of the three most recent temperature readings.

For example (Note: numbers would appear as binary in the system but are shown in decimal here):

Time elapsed	0 h	1 h	2 h	3 h	4 h	5 h	6 h
temperature reading	22	23	24	19	17	21	22
T_{Avg}	0	0	23	22	20	19	20

The company has the following digital hardware units available for this design project:
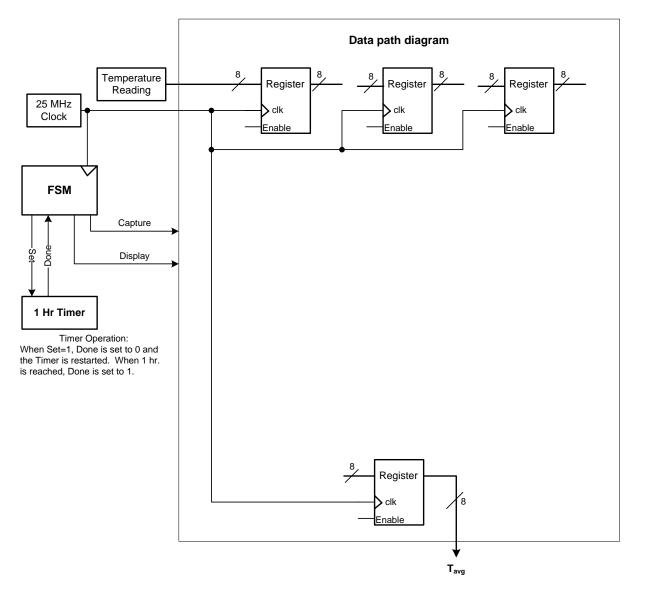

A junior engineer has already worked on this project and left you with an incomplete design. Your task is twofold: **a)** to complete the Data path diagram; and **b)** to draw a state diagram for the FSM, which will send out the appropriate signals to control the operation of the system represented by your completed Data path diagram.   Assume that the temperature reading input signal is synchronized to the Clock.
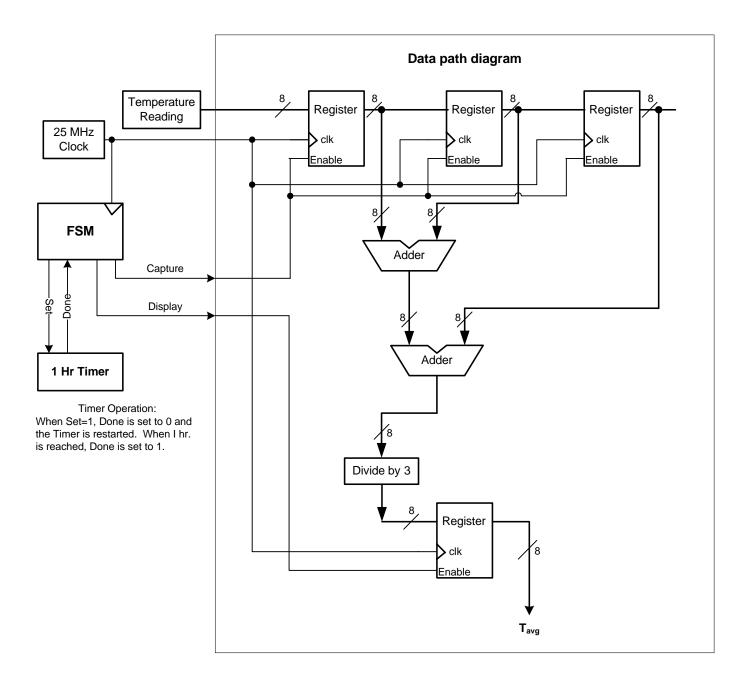
You will need the following specifications of the FSM: the "Capture" signal tells the system to take a new Temperature Reading; and the "Display" signal tells the system to display a new T_{Avg} .

Q7, continued.

      (a) Complete the Data path diagram (given below), using only the digital hardware units given above in the dashed box.

Data path diagram

Temperature Reading

25 MHz Clock

FSM

Set   Done

Capture

Display

1 Hr Timer

Timer Operation:
When Set=1, Done is set to 0 and the Timer is restarted. When 1 hr. is reached, Done is set to 1.

Register — clk — Enable

Register — clk — Enable

Register — clk — Enable

Register — clk — Enable

T_{avg}

Solution: 8 marks

Data path diagram

Temperature Reading

25 MHz Clock

FSM

Set   Done

1 Hr Timer

Capture

Display

Register   clk   Enable

Register   clk   Enable

Register   clk   Enable

8   8   8   8

Adder

8   8

Adder

8   8

8

Divide by 3

8

Register   clk   Enable

8

Tavg

Timer Operation:
When Set=1, Done is set to 0 and
the Timer is restarted. When I hr.
is reached, Done is set to 1.

Total: 5
1 marks for each of the two Adders (2)
1 mark for the Divider (1)
1 marks for the Capture signal (1)
1 mark for the Display signal (1)
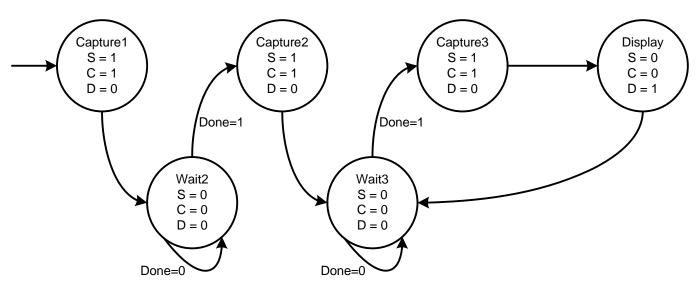
Q7, continued.
      (b) Give the state diagram for the FSM:

Solution: 7 marks total

Inputs: Done
Outputs: Set(S) Capture(C) Display(D)
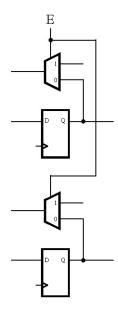
Capture1
S = 1
C = 1
D = 0

Capture2
S = 1
C = 1
D = 0

Capture3
S = 1
C = 1
D = 0

Display
S = 0
C = 0
D = 1

Done=1

Done=1

Wait2
S = 0
C = 0
D = 0

Wait3
S = 0
C = 0
D = 0

Done=0

Done=0

1 mark for each correct state
1 mark for all correct state transitions

[8] Q8.   Consider the Verilog code shown below, which describes a counter similar to ones described in Section 7.13 of the textbook.

```
module thing (R, M, Clock, L, E, Q);
        input [1:0] R, M;
        input Clock, L, E;
        output [1:0] Q;
        reg [1:0] Q;

        always @ (posedge Clock)
        begin
          if (L == 1)
            Q <= R;
          else if (E == 1)
            if (Q == M)
              Q <= 0;
            else
              Q <= Q + 1;
        end
endmodule
```
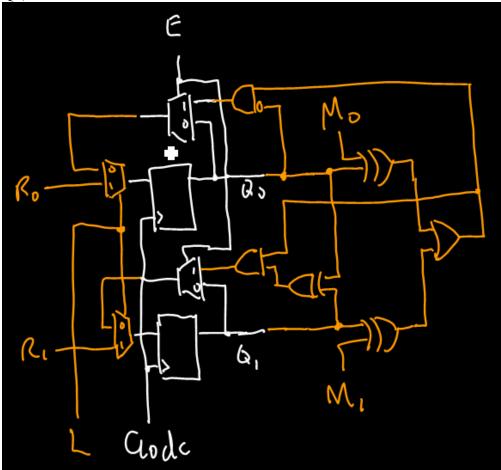
An incomplete circuit diagram that corresponds to this code is shown below. You are to complete the circuit diagram. Make the circuit as simple as you can.
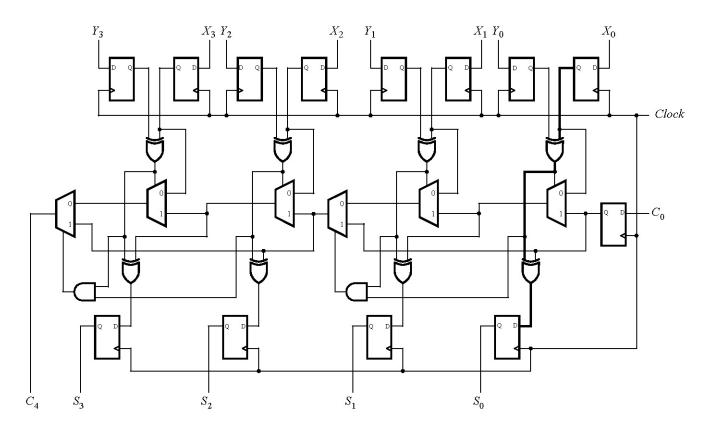
Q8, continued

Worth 8

Multiplexers for load on left: 2
Correct clear/reset when M=Q: 3
Exor gate for making it a counter: 3

[9] Q9. The circuit shown below produces the sum S = X + Y, with the carry-out C_4. Assume the following delays: t_{su} = 0.5 ns, t_{rd} = 0.3 ns (t_{rd} is also called $t_{clock-to-Q}$), t_h = 0.25 ns, exclusive-OR delay = 1.6 ns, AND delay = 1.55 ns, and multiplexer delay = 1.65 ns. Answer parts a) to c).

a) For this part, consider *only* the path through the circuit from the X_0 flip-flop to the S_0 flip-flop (this path is highlighted with a thick line in the figure). Considering only this path through the circuit, and ignoring the rest of the circuit, what is the maximum frequency of the *Clock* input for which the circuit would work reliably? Derive your answer in the space below (show your work).

ANSWER:

Solution:

Delay = $t_{rd} + t_{xor} + t_{xor} + t_{su}$
       = 0.3 + 1.6 + 1.6 + 0.5 = 4 ns
Fequency = 250 MHz

b) For this part, you are to consider the whole circuit shown in the figure. If the data inputs are $X_3 X_2 X_1 X_0 = 1111$ and $Y_3 Y_2 Y_1 Y_0 = 1111$, how much propagation time in total is needed from when a positive clock edge occurs to when the carry-out C_4 is produced? Derive your answer in the space below (show your work). Hint: think about which multiplexers produce the carry-out.

ANSWER:

Solution:

$Delay = t_{rd} + t_{xor} + t_{mux} + t_{mux}$

$= 0.3 + 1.6 + 1.65 + 1.65 = 5.2 \text{ ns}$

c) Again consider the whole circuit shown in the figure. If the data inputs are $X_3 X_2 X_1 X_0 = 0111$ and $Y_3 Y_2 Y_1 Y_0 = 1011$, how much propagation time in total is needed from when a positive clock edge occurs to when the carry-out C_4 is produced? Derive your answer in the space below (show your work). Hint: think about which multiplexers produce the carry-out.

ANSWER:

Solution:

$Delay = t_{rd} + t_{xor} + t_{mux} + t_{mux} + t_{mux}$

$= 0.3 + 1.6 + 1.65 + 1.65 + 1.65 = 6.85 \text{ ns}$

Solution marking scheme:
Part (a): 4 for correct frequency (3 if only correct delay is given)
(b): 2
(c): 2